Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

freescale™ semiconductor

QMCSUPPLEMENT/AD
8/97

QMC Supplement to
MC68360 and MPC860 User's Manuals

Home Page:
www.freescale.com
email:
support@freescale.com
USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com
Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com
Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com
Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com
For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

freescale™
semiconductor

CONTENTS

CONTENTS

CONTENTS

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS

TABLES

TABLES

About This Book

This document is a supplement to the *MC68360 Quad Integrated Communications Controller User's Manual* (MC68360UM/AD) and the *MPC860 PowerQUICC User's Manual* (MPC860UM/AD). It replaces the MC68MH360 Reference Manual (MC68MH360RM/AD).

To locate any published errata or updates for this document, refer to the website at http://www.mot.com/netcomm.

Audience

This manual is intended for system software and hardware developers. It is assumed that the reader understands basic concepts of time-division-multiplexed processors and how the MPC860 CPM operates.

Organization

Following is a summary and a brief description of the major sections of this manual:

- Chapter 1, "Overview," gives an introduction to the QMC (QUICC multichannel controller) protocol including some example applications.
- Chapter 2, "QMC Memory Organization," describes the operation specific to the QMC protocol.
- Chapter 3, "QMC Commands," discusses the transmit and receive commands.
- Chapter 4, "QMC Exceptions," describes QMC interrupt handling.
- Chapter 5, "Buffer Descriptors," describes the contents of the receive and transmit buffer descriptors for the QMC protocol and discusses the placement of QMC and non-QMC buffer descriptors in internal and external memory.
- Chapter 6, "QMC Initialization," discusses the essential steps to initialize QMC after a hard reset.
- Chapter 7, "Features Deleted in MC68MH360," lists the features deleted from the MH360.
- Chapter 8, "Performance," provides a performance table for common configurations supported by the 860MH and/or MH360; covers general guidelines and examples for determining the serial bit rate and CPM loading on a given system; and discusses system bus utilization and arbitration.

- Chapter 9, “Multi-Subchannel (MSC) Microcode,” provides the MSC microcode features and operation, and discusses how to program the MSC protocol.
- Appendix A, “68360 Bit Numbering,”shows the bit numbering used for the 68360.
- Appendix B, “Frequently-Asked Questions,” provides a list of common questions and solutions for the MH360 and 860MH.
- Appendix C, “Connecting S/T or U Interfaces to QUICC32,” shows how multiple MC145574 (S/T interface) or MC145572 (U interface) can be connected to a QUICC32. It describes the level-1 connections and explains the data flow through the devices.
- This manual also includes an index.

Additional Reading

This section provides a brief list of additional reading that supplements the information in this manual.

The following materials are available from the Motorola Literature Distribution Centers listed on the back cover of this manual; the document order numbers are included in parentheses for ease in ordering:

- *MPC860 PowerQUICC User’s Manual* (MPC860UM/AD)
- *MC68360 Quad Integrated Communications Controller User’s Manual*, Rev. 1 *(M68360UM/AD)*
- *M68000 Family Programmer’s Reference Manual*, Rev. 1 (M68000PM/AD)

Conventions

This document uses the following notational conventions:

ACTIVE_HIGH	Names for signals that are active high are shown in uppercase text without an overbar. Active-high signals are referred to as asserted when they are high and negated when they are low.
$\overline{\text{ACTIVE\_LOW}}$	A bar over a signal name indicates that the signal is active low. Active-low signals are referred to as asserted (active) when they are low and negated when they are high.
0x0F	Hexadecimal numbers
0b0011	Binary numbers
REG[FIELD]	Abbreviations or acronyms for registers are shown in uppercase text. Specific bit fields or ranges are shown in brackets.
Bold font (field name)	Entries in boldface must be initialized by the user.

Acronyms and Abbreviations

Table i contains acronyms and abbreviations that are used in this document.

Table i. Acronyms and Abbreviated Terms

Term	Meaning
BD	Buffer descriptor
bps	Bits per second
BRI	Basic rate interface
BRG	Baud rate generator
CPM	Communications processor module
CR	Command register
DCL	Data clock signal
FSC	Frame sync signal
GSM	Global system for mobile communications
GOV	Global receiver overrun (global error)
GUN	Global transmitting underrun (global error)
HDLC	High-level data link control
I^2C	Interprocessor-integrated controller channel
MSC	Multi-subchannel microcode
NMSI	Nonmultiplexed serial interface
QMC	QUICC multichannel controller
QUICC	QUad integrated communication controller
RCCR	RISC controller configuration register
RxBD	Receive buffer descriptor
SCC	Serial communication controller
SCCE	SCC event register
SI	Serial interface routing
SS-7	Signaling system 7
TDM	Time-division multiplexing
TSA	Time slot assigner
TSO	Time slot zero
TxBD	Transmit buffer descriptor

Chapter 1
Overview

This chapter gives an overview of the QMC protocol including some example applications.

1.1 The QMC (QUICC Multichannel Controller)

The QMC protocol emulates up to 64 logical channels within one SCC (serial communication controller) using the same time-division-multiplexed (TDM) physical interface. This multichannel protocol is implemented using the CPM ROM space and additional hardware; it is not a downloadable microcode.

The standard QUICC family members (MC68360[1], MPC860[2], etc.) work in TDM applications but can only support one logical channel per SCC. The parts currently supporting the QMC protocol are a superset to the following devices:

- MC68MH360 is a superset of the MC68EN360[3]
- MPC860MH is a superset of the MPC860EN
- MPC860DH is a superset of the MPC860DE

The QMC parts are pin-compatible with their respective family members. With minor adjustments, they can be used in identical applications such as primary rate ISDN support.

1.2 Introduction

Ideal for E1/T1 applications, the QMC protocol can multiplex any 64-channel combination of subgroups to one TDM interface.

Each of the channels can be separately programmed either to perform HDLC formatting/deformatting or to act as a transparent channel.

Both of the SI serial interfaces (for example, TDM_a or TDM_b) can be dedicated to the QMC protocol. The SI transfers the whole frame to an SCC[4]. Using the CPM RISC, the SCC

[1]MC68360 is trademarked as the QUICC.
[2]MPC860 is trademarked as the PowerQUICC.
[3]On the MC68MH360, protocol support for Centronics and BISYNC have been removed to create space for the QMC microcode.
[4]This is the normal operating mode; however, it is possible to split the TDM stream over several SCCs.

works transparently, not participating in any QMC protocol functions. The SCC only performs the parallel-to-serial conversion and adds elasticity through its FIFO memory. The CPM, with its special enhanced microcode and additional dedicated hardware for framing and masking support, does all of the protocol processing for each of the 64 channels. Note that it is executed without intervention from the on-board CPU. Figure 1-1 illustrates the QMC's multichannel capability. Note that each SCC can support up to 64 channels from the TDM; however, there are limitations depending on the device used. This is summarized in Section 1.3, "QMC Features."

Each SCC can work in QMC mode, either alone or together in any combination. The larger FIFO of SCC1 yields the best performance and is therefore recommended for QMC operation. One TDM connection can be routed to one or more SCCs operating in QMC mode, with each SCC operating on different time slots. It is possible to use both TDMs for QMC with combined routing to one SCC or to separate SCCs. When using two TDMs connected to one SCC, restrictions such as using common clocks and sync inputs apply; it is also important to avoid collisions by separating the serial interface (SI) routing.

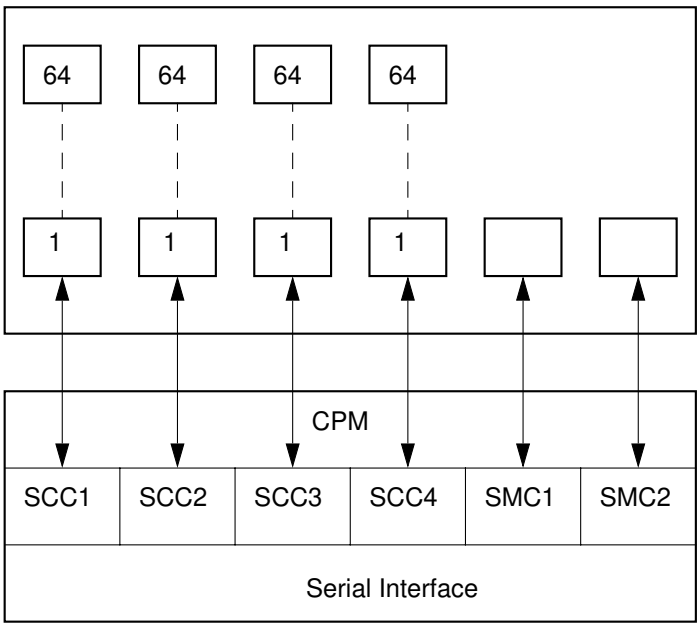

Figure 1-1. QMC Channel Addressing Capability

1.3 QMC Features

- MC68MH360-specific features
  - Up to 32 independent communication channels
  - Arbitrary mapping of any of 0–31 channels to any of 0–31 TDM time slot
  - Can support arbitrary mapping of any of 0–31 channels to any of 0–63 TDM time slots in case of common Rx and Tx mapping
  - Up to three additional HDLC 64-Kbps channels at 25-MHz system clock
  - Simultaneous Ethernet support at 33-MHz system clock
  - Up to 64 DMA channels with linear buffer array
- MPC860MH/DH-specific features
  - Up to 64 independent communication channels
  - Arbitrary mapping of any of 0–63 channels to any of 0–63 TDM time slots
  - Supports arbitrary mapping of any of 0–63 channels to any of 0–127 TDM time slots in case of common Rx and Tx mapping
  - Two simultaneous 32-channel E1 links at 50-MHz system clock
  - Up to 128 DMA channels with linear buffer array
- Common features
  - Independent mapping for receive/transmit
  - Supports either transparent or HDLC protocols for each channel
  - Interrupt circular buffer with programmable size and overflow identification
  - Global loop mode
  - Individual channel loop mode through the SI
  - Programmable frame length (via SI)
- Serial interface
  - Serial-multiplexed (full duplex) input/output 2048-, 1544-, or 1536-Kbps PCM highways
  - Compatible with T1/DS1 24-channel and CEPT E1 32-channel PCM highway, ISDN basic rate, ISDN primary rate and user-defined
  - Subchanneling on each time slot
  - Allows independent transmit and receive routing, frame syncs, and clocking
  - Concatenation of any, not necessarily consecutive, time slots to channels independently for receive/transmit
  - Supports H0, H11, and H12 ISDN channels
  - Allows dynamic allocation of channels

- System interface
  - On-chip bus arbitration for serial DMAs with no performance penalty
  - Efficient bus usage (no bus usage for nonactive channels and active channels that have nothing to transmit)
  - Efficient control of the interrupts to the CPU
  - Supports external buffer descriptors table
  - Uses on-chip enlarged dual-ported RAM for parameter storage

1.4 The Time Slot Assigner and the QMC

The time slot assigner (TSA) in the MH devices is no different from the other versions. This section discusses the new possibilities when using the TSA in combination with the QMC.

The QMC protocol can be executed in nonmultiplexed serial interface (NMSI) mode, but the usual operating mode takes advantage of the programmable time slot assigner,.

A frame synchronization pulse alerts the time slot assigner to start counting clock pulses. The user programs what bits are routed to the different internal serial channels. The TSA is an intelligent multiplexer that restarts its sequence on every frame synchronization pulse.

External strobe signals allow other devices that do not have built-in time slot assigner functions to participate in the TDM interface. This is very useful when interfacing to the MC68302 or other telecommunication devices like codecs.

The time slot assigner is not limited to standard TDM lines. It is a flexible, programmable device that allows the user to route any combination of bits and bytes to any channel. For example, the user can transmit 3 bits from SCC2, skip 12 bytes, and then transmit another 17 bits from SCC1. This routing must be programmed into the TSA memory. The complexity of the routing is limited only by the number of program entries in the TSA.

Ideal for TDM bridging applications, the MC68MH360 and MPC860MH have two independent time slot assigners and physical interfaces. A complete set of independent receive and transmit clock signals, as well as independent synchronization signals, are available for each TDM.

1.5 The Serial Interface (SI)

Functions such as frame synchronization, loopback, echo, and inverted signals are performed in the serial interface and cannot be achieved in NMSI mode. It is recommended to use the serial interface even if only one SCC is used for the TDM bus.

1.5.1 Synchronization

Independent receive and transmit clocks and frame synchronization signals control the data transfer. In NMSI operation, synchronization occurs only once to initiate a transfer using the CD (receive) and CTS (transmit) signals in pulse mode. If any noise corrupts either signal, the QMC will be out of synchronization until the whole protocol is restarted.

In contrast, the more robust SI performs a synchronization on each frame, limiting the damage from noise error on the clock or synchronization lines. Noisy channels can be restarted individually without interrupting other channels. For more details about possible errors in the TDM interface, see Section 1.8, “SI RAM Errors.”

1.5.2 Loopback Mode

The loopback from a transmitter to a receiver is implemented on a per channel basis for every logical channel. A common transmit and receive clock as well as a common frame synchronization pulse must be provided for loopback mode to work. The loopback is done on a fixed time slot, meaning that if one logical channel transmits on time slot 17, the loopback occurs through time slot 17 also, whether it is same logical channel or not that receives the incoming data. The reason for this restriction is that no buffering is performed after a channel is processed by the transmitter, or before it reaches the receiver.

Previously reserved, bit 15 of each entry in the SI-RAM is now the loopback bit controlling the loopback for the corresponding time slot. It is important to have each individual time slot as an entry in the SI-RAM for proper loopback on each individual channel.

1.5.3 Echo Mode

The SI can be programmed to echo incoming data. In this mode, the complete TDM link is retransmitted from the incoming L1RXDx to the L1TXDx pin on a bit-by-bit basis. The receiver section of the selected SCC can operate normally and also receive the incoming bit stream. This is also known as global echo mode on the whole link. Individual time slot echo is not possible with QMC without software intervention.

1.5.4 Inverted Signals

For each SCC, the DPLL can be used to invert the bitstream of the transmitter before the signal reaches the pin. This is not a bit-order inversion, but a logical level inversion. The DPLL can also invert the incoming data before it is forwarded to the receiver section. A logical inversion on a per channel basis is not possible in the QMC without external hardware. To invert a specific channel, the SI can be programmed to send a strobe signal at the channel’s corresponding time slot, assuming the SCC is operating in QMC mode. This strobe can then be connected to an external XOR gate to perform the inversion.

1.6 QMC Serial Routing and Example Applications

The QMC protocol provides multiple logical channels from a single SCC. The SCC channel dedicated to operate the QMC protocol should have all the relevant bits or time slots routed to it. Individual logical channels are selected by a combination of signals routed through the TDM and tables within the QMC protocol. Contrasting a non-QMC example application with QMC implementations highlights benefits of the multichannel protocol.

Figure 1-2 shows an Ethernet-to-BRI bridge using an MC68EN360, a non-QMC device. The configuration shows the Ethernet routed via an NMSI interface to SCC1. The ISDN BRI is routed via the TSA over an IDL2[1] interface to SCC2–SCC4 for the 2 B + D (B1, B2, and D) channels. The first byte of the frame (B1) is routed to SCC2, the second byte (B2) to SCC3, and then the next two bits (the D channel) to SCC4. In this example, SMC2 is used to connect to a PC over RS232. The internal routing is illustrated in Figure 1-3. Note that three SCCs are required to implement the ISDN BRI. This uses all the MC68EN360's serial channels without efficient use of the CPM bandwidth.

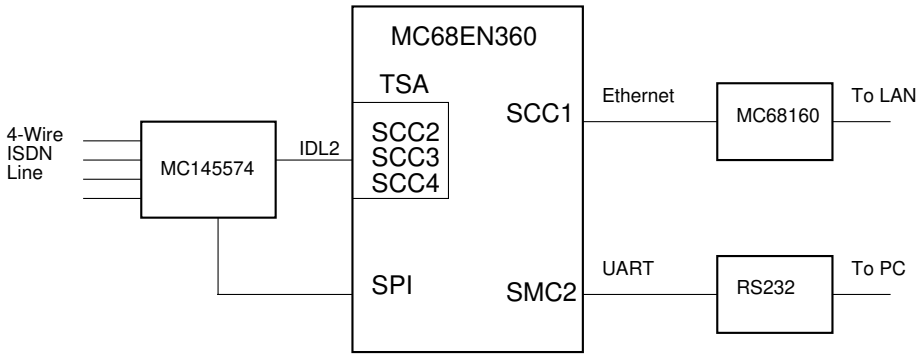

Figure 1-2. Ethernet-to-BRI Bridge Using MC68EN360

[1]The IDL2 interface is a full duplex ISDN interface used to interface to a physical layer device, such as the Motorola ISDN S/T transceiver MC145474.

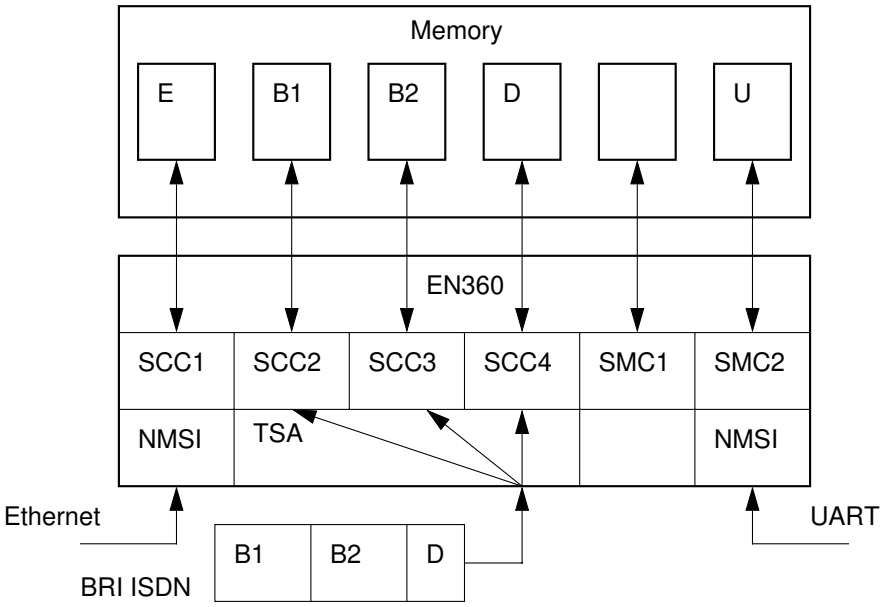

Figure 1-3. Internal Routing for Ethernet-to-BRI Bridge Using MC68EN360

The following example shows how an MC68MH360 can implement the BRI using only one SCC, leaving SCC3 and SCC4 available to run other protocols such as frame relay over HDLC and another Ethernet link, on SCC1, to the LAN. The QMC protocol allows all three channels B1, B2, and D to be routed to SCC2 using the TSA. The first byte (B1) is routed to logical channel 1, the second byte (B2) to logical channel 2, and the third byte to logical channel 3, of which only the first 2 bits represent the D channel as illustrated in Figure 1-4 and Figure 1-5. This routing is defined in the QMC time slot assignment tables. The first advantage of the QMC protocol is that it releases SCCs to run other protocols. The second advantage is highlighted in the next example.

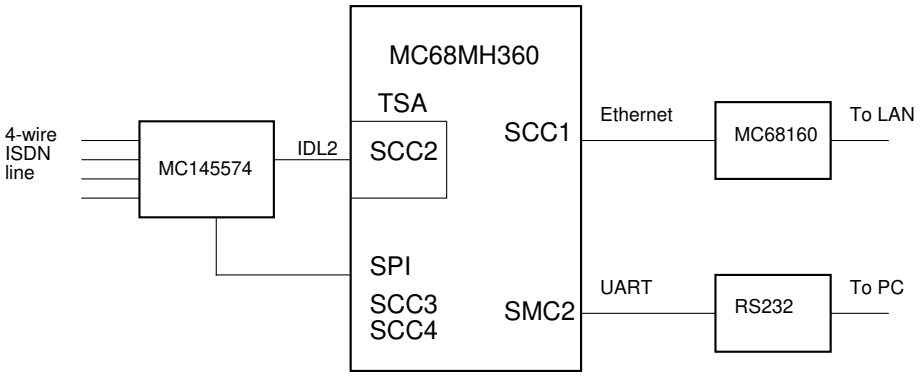

Figure 1-4. Ethernet-to-BRI Bridge Using MC68MH360

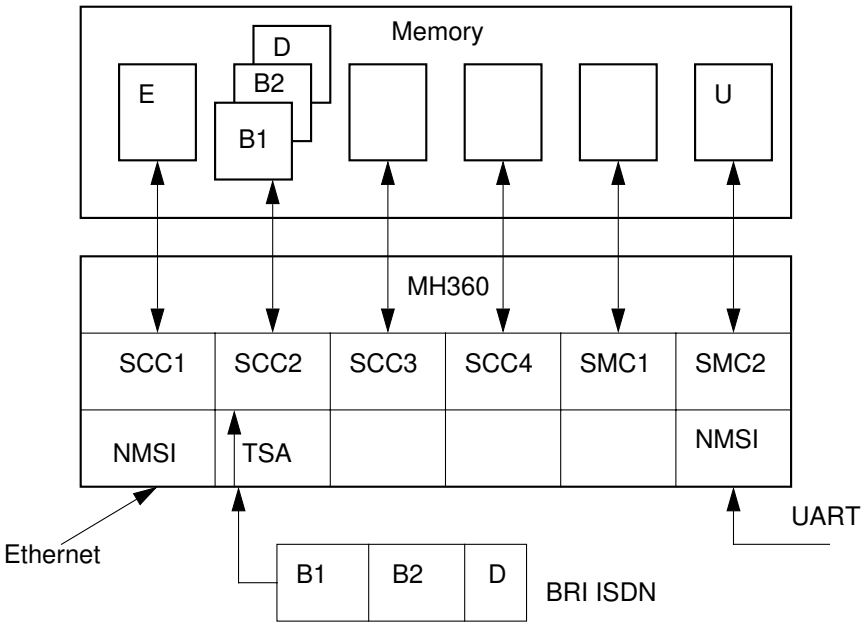

Figure 1-5. Internal Routing for Ethernet-to-BRI Bridge Using MC68MH360

Figure 1-6 and Figure 1-7 show how to build a PRI ISDN-to-Ethernet bridge using an MPC860MH. SCC1 is used for the Ethernet channel. SCC2 is configured for QMC mode in which each of the 30 B channels and the D channel are routed to separate logical channels. The true advantage of the QMC protocol is the ability to route multiple channels to a single SCC.

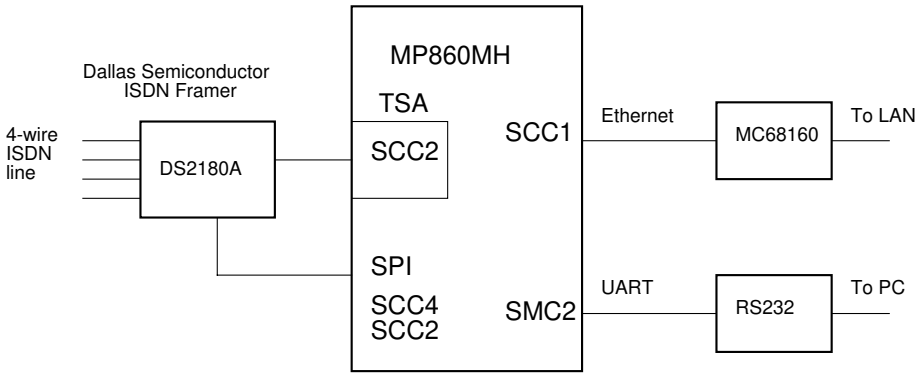

Figure 1-6. Ethernet-to-PRI Bridge Using MPC860MH

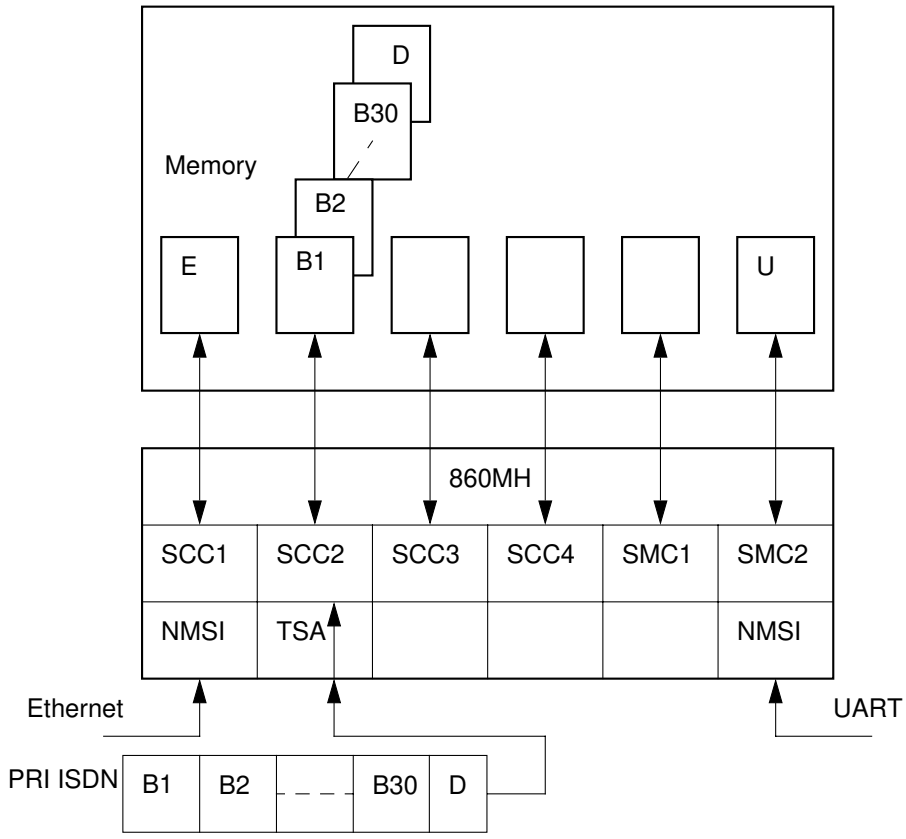

Figure 1-7. Internal Routing for Ethernet-to-PRI Bridge Using MPC860