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MC68HC705P6A

Advance Information Data Sheet

M68HC05
Microcontrollers

MC68HC705P6A
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MC68HC705P6A

Advance Information Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
November, 2001	2.0	Format update to current publication standards	N/A
		Figure 11-1. Mask Option Register (MOR) — Definition of bit 6 corrected.	92
September, 2005	2.1	Updated to meet Freescale identity guidelines.	Throughout

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Chapter 1
General Description

1.1 Introduction

The MC68HC705P6A is an EPROM version of the MC68HC05P6 microcontroller. It is a low-cost combination of an M68HC05 Family microprocessor with a 4-channel, 8-bit analog-to-digital (A/D) converter, a 16-bit timer with output compare and input capture, a serial communications port (SIOP), and a computer operating properly (COP) watchdog timer. The M68HC05 CPU core contains 176 bytes of RAM, 4672 bytes of user EPROM, 239 bytes of bootloader ROM, and 21 input/output (I/O) pins (20 bidirectional, 1 input-only). This device is available in either a 28-pin plastic dual in-line (PDIP) or a 28-pin small outline integrated circuit (SOIC) package.

A functional block diagram of the MC68HC705P6A is shown in Figure 1-1.

1.2 Features

Features of the MC68HC705P6A include:

- Low cost
- M68HC05 core
- 28-pin SOIC, PDIP, or windowed DIP package
- 4672 bytes of user EPROM (including 48 bytes of page zero EPROM and 16 bytes of user vectors)
- 239 bytes of bootloader ROM
- 176 bytes of on-chip RAM
- 4-channel 8-bit A/D converter
- SIOP serial communications port
- 16-bit timer with output compare and input capture
- 20 bidirectional I/O lines and 1 input-only line
- PC0 and PC1 high-current outputs
- Single-chip, bootloader, and test modes
- Power-saving stop, halt, and wait modes
- Static EPROM mask option register (MOR) selectable options:
  - COP watchdog timer enable or disable
  - Edge-sensitive or edge- and level-sensitive external interrupt
  - SIOP most significant bit (MSB) or least significant bit (LSB) first
  - SIOP clock rates: OSC divided by 8, 16, 32, or 64
  - Stop instruction mode, STOP or HALT
  - EPROM security external lockout
  - Programmable keyscan (pullups/interrupts) on PA0–PA7

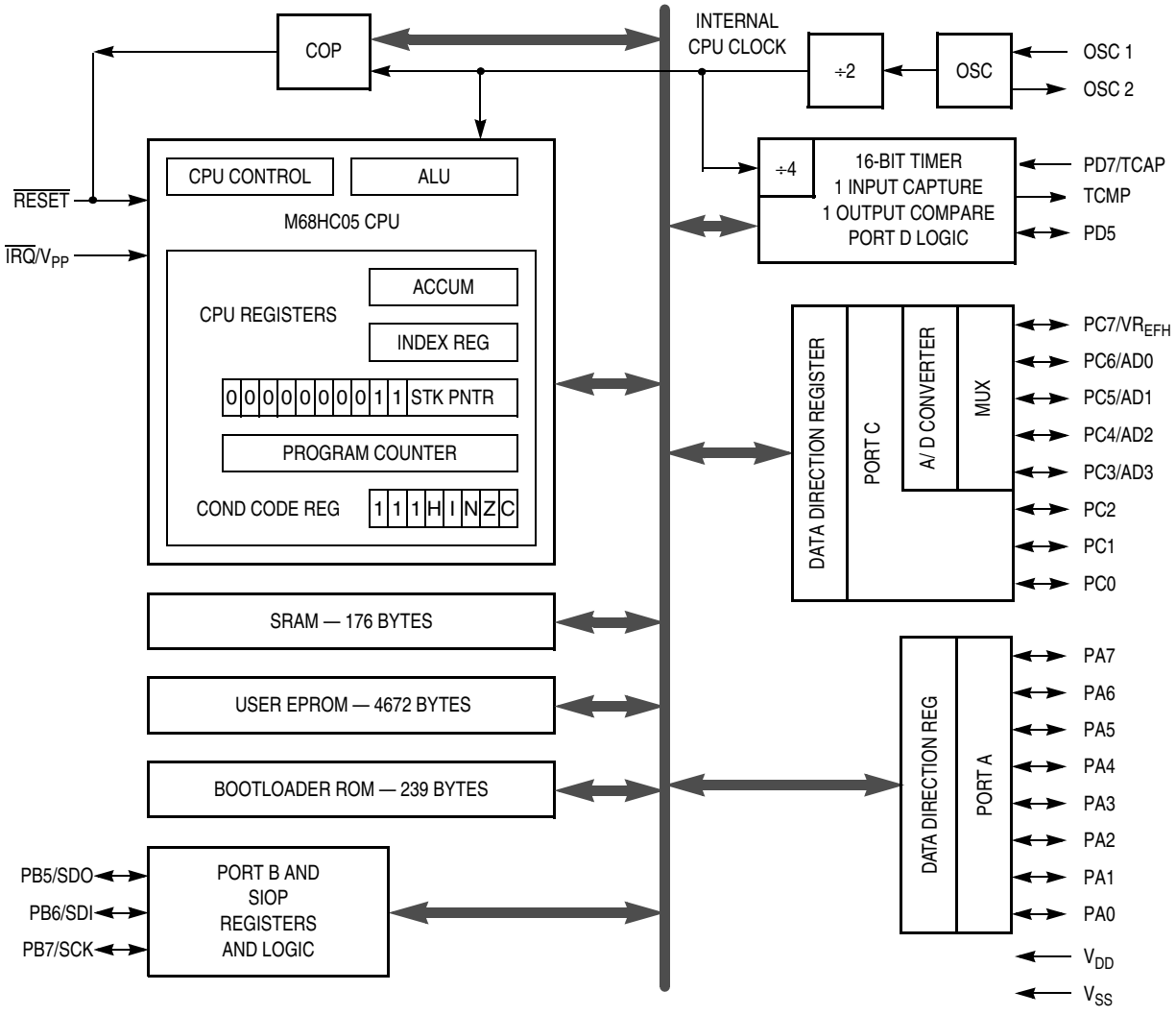


Figure 1-1. MC68HC705P6A Block Diagram

NOTE

A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{RESET}$ is active low.

Any reference to voltage, current, or frequency specified in the following sections will refer to the nominal values. The exact values and their tolerances or limits are specified in Chapter 14 Electrical Specifications.

1.3 Functional Pin Description

The following paragraphs describe the functionality of each pin on the MC68HC705P6A package. Pins connected to subsystems described in other chapters provide a reference to the chapter instead of a detailed functional description.

1.3.1 V_{DD} and V_{SS}

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is connected to a regulated +5 volt supply and V_{SS} is connected to ground.

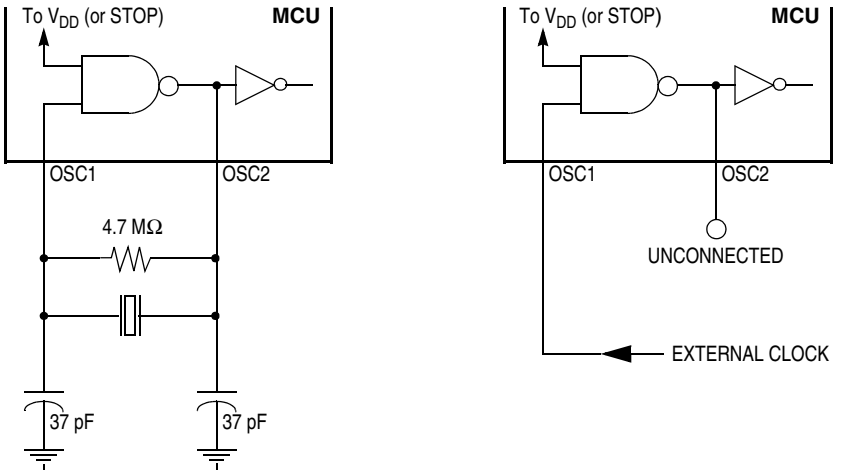
Very fast signal transitions occur on the MCU pins. The short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, take special care to provide good power supply bypassing at the MCU. Use bypass capacitors with good high-frequency characteristics and position them as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

1.3.2 OSC1 and OSC2

The OSC1 and OSC2 pins are the control connections for the on-chip oscillator. The OSC1 and OSC2 pins can accept the following:

1. A crystal as shown in Figure 1-2(a)
2. A ceramic resonator as shown in Figure 1-2(a)
3. An external clock signal as shown in Figure 1-2(b)

The frequency, f_{osc}, of the oscillator or external clock source is divided by two to produce the internal bus clock operating frequency, f_{op}. The oscillator cannot be turned off by software unless the MOR bit, SWAIT, is clear when a STOP instruction is executed.



(a) Crystal or Ceramic Resonator Connections

(b) External Clock Source Connections

Figure 1-2. Oscillator Connections

1.3.2.1 Crystal

The circuit in Figure 1-2(a) shows a typical oscillator circuit for an AT-cut, parallel resonant crystal. Follow the crystal manufacturer's recommendations, as the crystal parameters determine the external component values required to provide maximum stability and reliable startup. The load capacitance values used in the oscillator circuit design should include all stray capacitances. Mount the crystal and components as close as possible to the pins for startup stabilization and to minimize output distortion.

1.3.2.2 Ceramic Resonator

In cost-sensitive applications, use a ceramic resonator in place of a crystal. Use the circuit in Figure 1-2(a) for a ceramic resonator and follow the resonator manufacturer's recommendations, as the resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances. Mount the resonator and components as close as possible to the pins for startup stabilization and to minimize output distortion.

1.3.2.3 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in Figure 1-2(b).

1.3.3 $\overline{\text{RESET}}$

Driving this input low will reset the MCU to a known startup state. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity. Refer to Chapter 4 Resets.

1.3.4 PA0–PA7

These eight I/O pins comprise port A. The state of any pin is software programmable and all port A lines are configured as inputs during power-on or reset. Port A has mask-option register enabled interrupt capability with internal pullup devices selectable for any pin. Refer to Chapter 6 Input/Output Ports.

1.3.5 PB5/SDO, PB6/SDI, and PB7/SCK

These three I/O pins comprise port B and are shared with the SIOP communications subsystem. The state of any pin is software programmable, and all port B lines are configured as inputs during power-on or reset. Refer to Chapter 6 Input/Output Ports and Chapter 7 Serial Input/Output Port (SIOP).

1.3.6 PC0-PC2, PC3/AD3, PC4/AD2, PC5/AD1, PC6/AD0, and PC7/V_{REFH}

These eight I/O pins comprise port C and are shared with the A/D converter subsystem. The state of any pin is software programmable and all port C lines are configured as inputs during power-on or reset. Refer to Chapter 6 Input/Output Ports and Chapter 9 Analog Subsystem.

1.3.7 PD5 and PD7/TCAP

These two I/O pins comprise port D and one of them is shared with the 16-bit timer subsystem. The state of PD5 is software programmable and is configured as an input during power-on or reset. PD7 is always an input. It may be read at any time, regardless of which mode of operation the 16-bit timer is in. Refer to Chapter 6 Input/Output Ports and Chapter 8 Capture/Compare Timer.

1.3.8 TCMP

This pin is the output from the 16-bit timer's output compare function. It is low after reset. Refer to Chapter 8 Capture/Compare Timer.

1.3.9 $\overline{IRQ}/V_{PP}$ (Maskable Interrupt Request)

This input pin drives the asynchronous interrupt function of the MCU in user mode and provides the V_{PP} programming voltage in bootloader mode. The MCU will complete the current instruction being executed before it responds to the $\overline{IRQ}$ interrupt request. When the $\overline{IRQ}/V_{PP}$ pin is driven low, the event is latched internally to signify an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch is set and the interrupt mask bit (I bit) in the condition code register is clear, the MCU will begin the interrupt sequence.

Depending on the MOR LEVEL bit, the $\overline{IRQ}/V_{PP}$ pin will trigger an interrupt on either a negative edge at the $\overline{IRQ}/V_{PP}$ pin and/or while the $\overline{IRQ}/V_{PP}$ pin is held in the low state. In either case, the $\overline{IRQ}/V_{PP}$ pin must be held low for at least one t_{ILIH} time period. If the edge- and level-sensitive mode is selected (LEVEL bit set), the $\overline{IRQ}/V_{PP}$ input pin requires an external resistor connected to V_{DD} for wired-OR operation. If the $\overline{IRQ}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply. The $\overline{IRQ}/V_{PP}$ pin input circuitry contains an internal Schmitt trigger to improve noise immunity. Refer to Chapter 5 Interrupts.

NOTE

If the voltage level applied to the $\overline{IRQ}/V_{PP}$ pin exceeds V_{DD}, it may affect the MCU's mode of operation. See Chapter 3 Operating Modes.

Chapter 2
Memory

2.1 Introduction

The MC68HC705P6A utilizes 13 address lines to access an internal memory space covering 8 Kbytes. This memory space is divided into I/O, RAM, ROM, and EPROM areas.

2.2 User Mode Memory Map

When the MC68HC705P6A is in the user mode, the 32 bytes of I/O, 176 bytes of RAM, 4608 bytes of user EPROM, 48 bytes of user page zero EPROM, 239 bytes of bootloader ROM, and 16 bytes of user vectors EPROM are all active as shown in Figure 2-1.

2.3 Bootloader Mode Memory Map

Memory space is identical to the user mode. See Figure 2-1.

2.4 Input/Output and Control Registers

Figure 2-2 and Figure 2-3 briefly describe the I/O and control registers at locations $0000–$001F. Reading unimplemented bits will return unknown states, and writing unimplemented bits will be ignored.

2.5 RAM

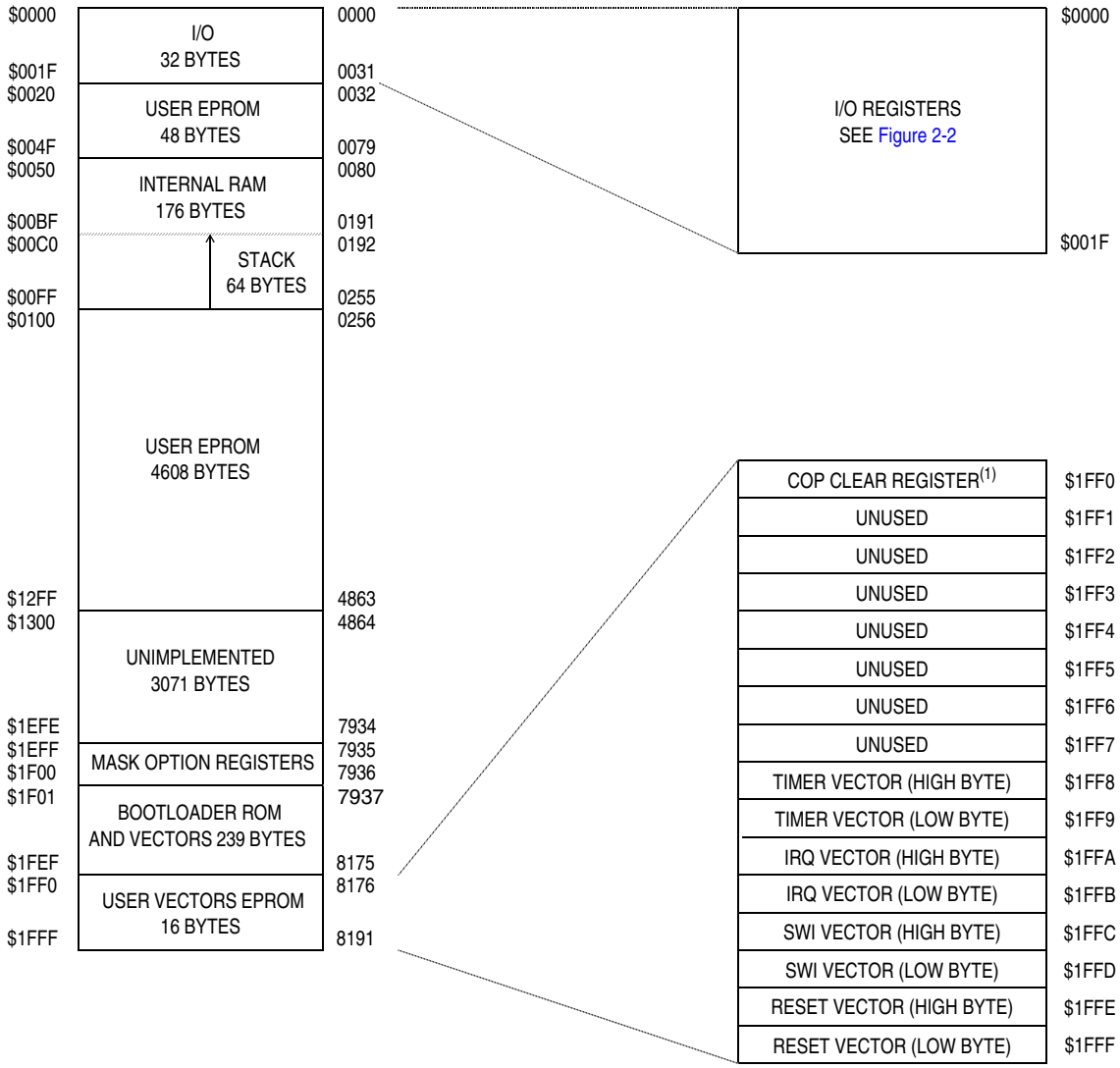
The user RAM consists of 176 bytes (including the stack) at locations $0050 through $00FF. The stack begins at address $00FF. The stack pointer can access 64 bytes of RAM from $00FF to $00C0.

NOTE

Using the stack area for data storage or temporary work locations requires care to prevent it from being overwritten due to stacking from an interrupt or subroutine call.

2.6 EPROM/ROM

There are 4608 bytes of user EPROM at locations $0100 through $12FF, plus 48 bytes in user page zero locations $0020 through $004F, and 16 additional bytes for user vectors at locations $1FF0 through $1FFF. The bootloader ROM and vectors are at locations $1F01 through $1FEF.



Note 1. Writing zero to bit 0 of $1FF0 clears the COP watchdog timer. Reading $1FF0 returns user EPROM data.

Figure 2-1. MC68HC705P6A User Mode Memory Map

PORT A DATA REGISTER	$0000
PORT B DATA REGISTER	$0001
PORT C DATA REGISTER	$0002
PORT D DATA REGISTER	$0003
PORT A DATA DIRECTION REGISTER	$0004
PORT B DATA DIRECTION REGISTER	$0005
PORT C DATA DIRECTION REGISTER	$0006
PORT D DATA DIRECTION REGISTER	$0007
UNIMPLEMENTED	$0008
UMIMPLEMENTED	$0009
SIOP CONTROL REGISTER	$000A
SIOP STATUS REGISTER	$000B
SIOP DATA REGISTER	$000C
RESERVED	$000D
UNIMPLEMENTED	$000E
UNIMPLEMENTED	$000F
UNIMPLEMENTED	$0010
UNIMPLEMENTED	$0011
TIMER CONTROL REGISTER	$0012
TIMER STATUS REGISTER	$0013
INPUT CAPTURE MSB	$0015
INPUT CAPTURE LSB	$0016
OUTPUT COMPARE MSB	$0017
OUTPUT COMPARE LSB	$0017
TIMER MSB	$0018
TIMER LSB	$0019
ALTERNATE COUNTER MSB	$001A
ALTERNATE COUNTER LSB	$001B
EPROM PROGRAMMING REGISTER	$001C
A/D CONVERTER DATA REGISTER	$001D
A/D CONVERTER CONTROL AND STATUS REGISTER	$001E
RESERVED	$001F

Figure 2-2. MC68HC705P6A I/O and Control Registers Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 37.	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 38.	Read:	PB7	PB6	PB5	0	0	0	0	0
		Write:								
		Reset:	Unaffected by reset							
$0002	Port C Data Register (PORTC) See page 38.	Read:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Write:								
		Reset:	Unaffected by reset							
$0003	Port D Data Register (PORTD) See page 39.	Read:	PD7	0	PD5	1	0	0	0	0
		Write:								
		Reset:	Unaffected by reset							
$0004	Port A Data Direction Register (DDRA) See page 37.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Port B Data Direction Register (DDRB) See page 38.	Read:	DDRB7	DDRB6	DDRB5	1	1	1	1	1
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0006	Port C Data Direction Register (DDRC) See page 38.	Read:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0007	Port D Data Direction Register (DDRD) See page 39.	Read:	0	0	DDRD5	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0008	Unimplemented									
$0009	Unimplemented									
$000A	SIOP Control Register (SCR) See page 43.	Read:	0	SPE	0	MSTR	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000B	SIOP Status Register (SSR) See page 44.	Read:	SPIF	DCOL	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000C	SIOP Data Register (SDR) See page 44.	Read:	SDR7	SDR6	SDR5	SDR4	SDR3	SSDR2	SDR1	SDR0
		Write:								
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Undetermined

Figure 2-3. I/O and Control Register Summary (Sheet 1 of 3)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000D	Reserved for Test		R	R	R	R	R	R	R	R
$000E	Unimplemented									
$000F	Unimplemented									
$0010	Unimplemented									
$0011	Unimplemented									
$0012	Timer Control Register (TCR) See page 47.	Read:	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL
		Write:								
		Reset:	0	0	0	0	0	0	U	0
$0013	Timer Status Register (TSR) See page 48.	Read:	ICF	OCF	TOF	0	0	0	0	0
		Write:								
		Reset:	U	U	U	0	0	0	0	0
$0014	Input Capture Register MSB (ICRH) See page 50.	Read:	ICRH7	ICRH6	ICRH5	ICRH4	ICRH3	ICRH2	ICRH1	ICRH0
		Write:								
		Reset:	Unaffected by reset							
$0015	Input Capture Register LSB (ICRL) See page 50.	Read:	ICRL7	ICRL6	ICRL5	ICRL4	ICRL3	ICRL2	ICRL1	ICRL0
		Write:								
		Reset:	Unaffected by reset							
$0016	Output Compare Register MSB (OCRH) See page 50.	Read:	OCRH7	OCRH6	OCRH5	OCRH4	OCRH3	OCRH2	OCRH1	OCRH0
		Write:								
		Reset:	Unaffected by reset							
$0017	Output Compare Register LSB (OCRL) See page 50.	Read:	OCRL7	OCRL6	OCRL5	OCRL4	OCRL3	OCRL2	OCRL1	OCRL0
		Write:								
		Reset:	Unaffected by reset							
$0018	Timer Register MSB (TRH) See page 49.	Read:	TRH7	TRH6	TRH5	TRH4	TRH3	TRH2	TRH1	TRH0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0019	Timer Register LSB (TRL) See page 49.	Read:	TRL7	TRL6	TRL5	TRL4	TRL3	TRL2	TRL1	TRL0
		Write:								
		Reset:	1	1	1	1	1	1	0	0
$001A	Alternate Timer Register MSB (ATRH) See page 49.	Read:	ACRH7	ACRH6	ACRH5	ACRH4	ACRH3	ACRH2	ACRH1	ACRH0
		Write:								
		Reset:	1	1	1	1	1	1	1	1

= Unimplemented R = Reserved U = Undetermined

Figure 2-3. I/O and Control Register Summary (Sheet 2 of 3)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001B	Alternate Timer Register LSB (ATRL) See page 49.	Read:	ACRL7	ACRL6	ACRL5	ACRL4	ACRL3	ACRL2	ACRL1	ACRL0
		Write:								
		Reset:	1	1	1	1	1	1	0	0
$001C	EPROM Programming Register (EPROG) See page 58.	Read:	0	0	0	0	0	ELAT	0	EPGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001D	A/D Conversion Value Data Register (ADC) See page 55.	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Write:								
		Reset:	Unaffected by reset							
$001E	A/D Status and Control Register (ADSC) See page 54.	Read:	CC	ADRC	ADON	0	0	CH2	CH1	CH0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001F	Reserved for Test		R	R	R	R	R	R	R	R

= Unimplemented R = Reserved U = Undetermined

Figure 2-3. I/O and Control Register Summary (Sheet 3 of 3)

2.7 Mask Option Register

The mask option register (MOR) is a pair of EPROM bytes located at $1EFF and $1F00. It controls the programmable options on the MC68HC705P6A. See Chapter 11 Mask Option Register (MOR) for additional information.

	$1EFF	Bit 7	6	5	4	3	2	1	Bit 0
	Read: Write:	PA7PU	PA6PU	PA5PU	PA4PU	PA3PU	PA2PU	PA1PU	PA0PU
	Erased State:	0	0	0	0	0	0	0	0

	$1F00	Bit 7	6	5	4	3	2	1	Bit 0
	Read: Write:	SECURE		SWAIT	SPR1	SPR0	LSBF	LEVEL	COP
	Erased State:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 2-4. Mask Option Register (MOR)

2.8 Computer Operating Properly (COP) Clear Register

The computer operating properly (COP) watchdog timer is located at address $1FF0. Writing a logical 0 to bit zero of this location will clear the COP watchdog counter as described in 4.3.2 Computer Operating Properly (COP) Reset.

$1FF0	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:								COPR
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 2-5. COP Watchdog Timer Location