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HC05

MC68HC05X16
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MC68HC05X16
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High-density complementary metal oxide semiconductor (HCMOS) microcontroller unit

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Where abbreviations are used in the text, an explanation can be found in the glossary, at the back of this manual. Register and bit mnemonics are defined in the paragraphs describing them.

An overbar is used to designate an active-low signal, eg: $\overline{\text{RESET}}$.

Unless otherwise stated, a shaded cell in a register diagram indicates that the bit is either unused or reserved; 'u' is used to indicate an undefined state (on reset).

Unless otherwise stated, a pin labelled as 'NU' should be tied to V_{SS} in an electrically noisy environment. Pins labelled 'NC' can be left floating, since they are not bonded to any part of the device.

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1
INTRODUCTION

The MC68HC05X16 microcomputer (MCU) is a member of Motorola's MC68HC05 family of low-cost single chip microcomputers. This 8-bit MCU contains an on-board controller area network module (MCAN), complete with interface circuitry, comprising output drivers, input comparators and a $V_{DD}/2$ generator. In addition, the device contains an on-chip oscillator, CPU, RAM, ROM, EEPROM, A/D converter, pulse length modulated outputs, I/O, serial communications interface, programmable timer system and watchdog. The fully static design allows operation at frequencies down to dc, reducing power consumption to a few micro-amps.

This data sheet is structured such that devices similar to the MC68HC05X16 are described in a set of appendices (see Table 1-1).

Table 1-1 Data sheet appendices

Device	Appendix	Differences from MC68HC05X16
MC68HC05X32	A	32K bytes ROM; increased RAM
MC68HC705X32	B	32K bytes EPROM; increased RAM; bootstrap firmware replaced
MC68HC05X32	C	32K bytes ROM; increased RAM; high speed operation

Note: Appendix C contains only electrical characteristics exclusive to the high speed operation of the MC68HC05X32. For all other information concerning this device, refer to Appendix A.

1.1 Features

Hardware features

- Fully static design featuring the industry standard M68HC05 family CPU core
- On chip crystal oscillator with divide-by -2, -4, -8 or -10, or a software selectable divide-by -32, -64, -128 or -160 option (SLOW mode)
- 352 bytes of RAM
- 15102 bytes of user ROM plus 16 bytes of user vectors
- 256 bytes of byte erasable EEPROM with internal charge pump and security bit
- Write/erase protect bit for 224 of the 256 bytes EEPROM
- Bootstrap firmware
- Power saving STOP, WAIT and SLOW modes
- Three 8-bit parallel I/O ports and one 8-bit input-only port; wired-OR interrupt capability on all port B pins
- Motorola controller area network (MCAN) with line interface circuitry
- Software option available to output the internal E-clock to port pin PC2
- 16-bit timer with 2 input captures and 2 output compares
- Computer operating properly (COP) watchdog timer
- Serial communications interface system (SCI) with independent transmitter/receiver baud rate selection; receiver wake-up function for use in multi-receiver systems
- 8 channel A/D converter
- 2 pulse length modulation systems which can be used as D/A converters
- One interrupt request input plus 4 on-board hardware interrupt sources
- 2.2 MHz bus speed
- –40 to +125°C temperature range
- Available in 64-pin quad flat pack (QFP) package
- Complete development system support available using the MMDS05 or M68MMPFB0508 development station with the M68EML05X32 emulation module or the M68HC05XEVS evaluation system

1.2 Mask options for the MC68HC05X16

The MC68HC05X16 has six mask options that are programmed during manufacture and must be specified on the order form.

- Oscillator division ratio selection (divide-by-2, -4, -8 or -10)
- Oscillator start-up delay following power-on or STOP (t_{PORL}) = 16 or 4064 cycles
- Automatic watchdog enable/disable following a power-on or external reset
- Watchdog enable/disable during WAIT mode
- Wired-OR interrupt enable
- Resistive pull-downs on ports B and/or C

Note: It is recommended that an external clock is always used if t_{PORL} is set to 16 cycles. This will prevent any problems arising from oscillator stability when the device is put into STOP mode.

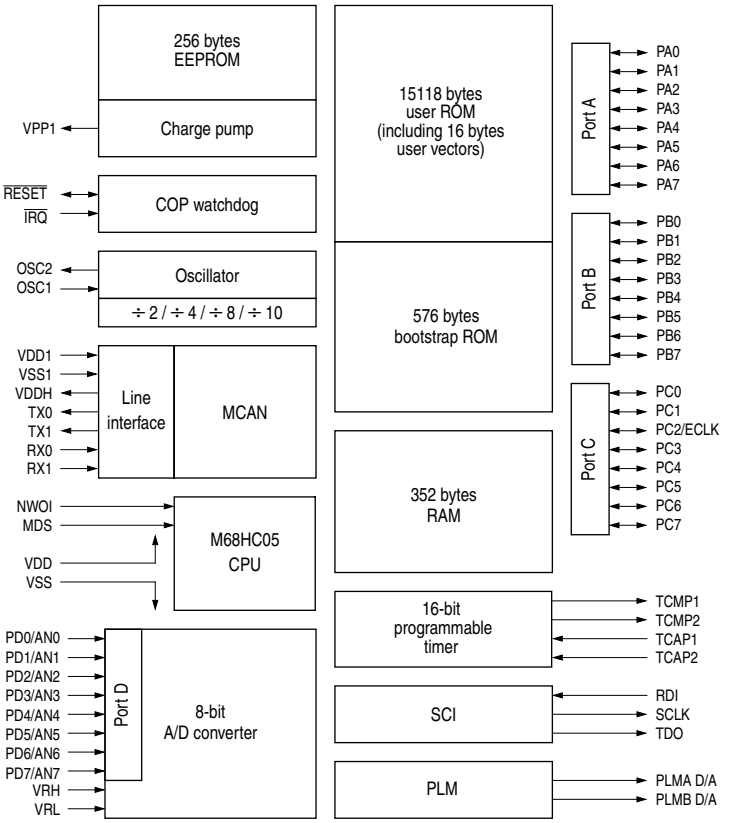

Figure 1-1 MC68HC05X16 block diagram

2
MODES OF OPERATION AND PIN DESCRIPTIONS

2.1 Modes of operation

The MC68HC05X16 MCU has two modes of operation, single-chip mode and bootstrap mode. In the MC68HC05X16 the single-chip mode is the normal user operating frequency Table 2-1 shows the conditions required to enter each mode on the rising edge of $\overline{\text{RESET}}$.

Table 2-1 Mode of operation selection

MDS		IRQ	TCAP1	TCAP2	PD3	PD4	Mode
V_{SS}	AND	V_{SS} to V_{DD}	V_{SS} to V_{DD}	X	X	X	Single-chip
V_{DD}	OR	$2V_{DD}$	V_{SS}	X	0	0	Reserved for Motorola use
							Bootstrap mode:
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	1	1	Serial RAM loader
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	1	0	Jump to RAM + 1
V_{DD}	OR	$2V_{DD}$	V_{DD}	V_{SS}	0	1	Jump to any address

Note: On the rising edge of $\overline{\text{RESET}}$, holding the $\overline{\text{IRQ}}$ pin at 2 x V_{DD} is equivalent to holding the MDS pin at V_{DD}. The device cannot enter single-chip mode unless MDS is tied to V_{SS} (or left floating) **and** IRQ is below V_{DD}.

2.1.1 Single-chip mode

This is the normal user operating mode of the MC68HC05X16. In this mode the device functions as a self-contained microcomputer (MCU) with all on-board peripherals, including the three 8-bit I/O ports and the 8-bit input-only port, available to the user. All address and data activity occurs within the MCU.