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MC74HC4051A,
MC74HC4052A,
MC74HC4053A

Analog Multiplexers / Demultiplexers

High−Performance Silicon−Gate CMOS

The MC74HC4051A, MC74HC4052A and MC74HC4053A utilize silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The HC4051A, HC4052A and HC4053A are identical in pinout to the metal−gate MC14051AB, MC14052AB and MC14053AB. The Channel−Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel−Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.
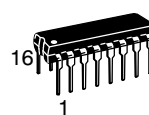
These devices have been designed so that the ON resistance (R_{on}) is more linear over input voltage than R_{on} of metal−gate CMOS analog switches.

For a multiplexer/demultiplexer with injection current protection, see HC4851A and HC4852A.
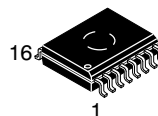
Features

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC} - V_{EE}) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range (V_{CC} - GND) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal−Gate Counterparts
- Low Noise
- In Compliance with the Requirements of JEDEC Standard No. 7A
- Chip Complexity: HC4051A — 184 FETs or 46 Equivalent Gates
                     HC4052A — 168 FETs or 42 Equivalent Gates
                     HC4053A — 156 FETs or 39 Equivalent Gates
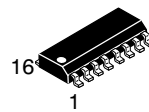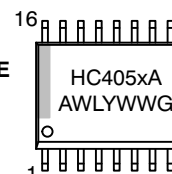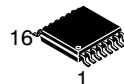- Pb−Free Packages are Available

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MARKING DIAGRAMS

PDIP−16
N SUFFIX
CASE 648

MC74HC405xAN
AWLYYWWG

SOIC−16 WIDE
DW SUFFIX
CASE 751G

HC405xA
AWLYWWG

SOIC−16
D SUFFIX
CASE 751B

HC405xAG
AWLYWW

TSSOP−16
DT SUFFIX
CASE 948F

HC40
5xA
ALYW■

SOEIAJ−16
F SUFFIX
CASE 966

74HC405xA
ALYWG
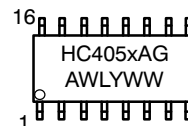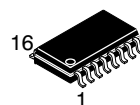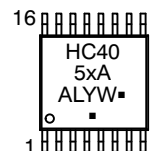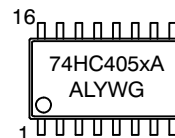
x	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package
■	= Pb−Free Package

(Note: Microdot may be in either location)
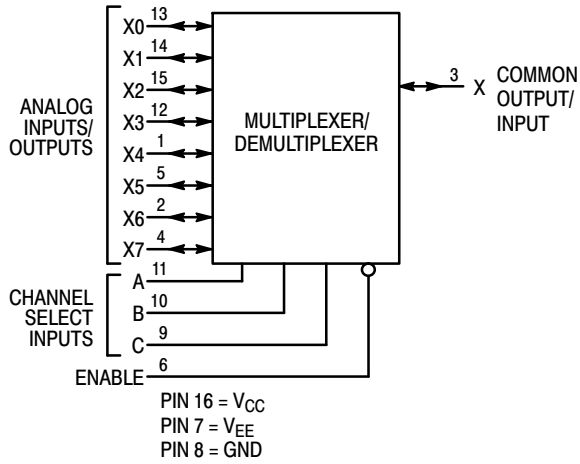
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

1

MC74HC4051A, MC74HC4052A, MC74HC4053A

LOGIC DIAGRAM
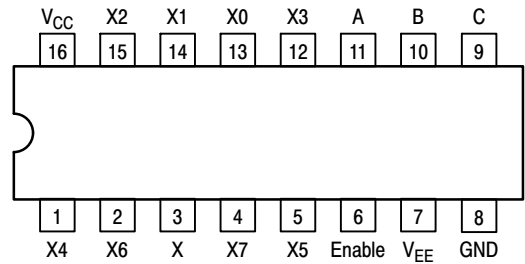### MC74HC4051A
Single–Pole, 8-Position Plus Common Off

X0 13
X1 14
X2 15
X3 12
X4 1
X5 5
X6 2
X7 4

ANALOG INPUTS/OUTPUTS

MULTIPLEXER/DEMULTIPLEXER

3 X COMMON OUTPUT/INPUT

A 11
B 10
C 9

CHANNEL SELECT INPUTS

ENABLE 6

PIN 16 = V_{CC}
PIN 7 = V_{EE}
PIN 8 = GND

FUNCTION TABLE – MC74HC4051A

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

Pinout: MC74HC4051A (Top View)

V_{CC}	X2	X1	X0	X3	A	B	C
16	15	14	13	12	11	10	9

1	2	3	4	5	6	7	8
X4	X6	X	X7	X5	Enable	V_{EE}	GND

LOGIC DIAGRAM
MC74HC4052A
Double–Pole, 4-Position Plus Common Off

X0 12
X1 14
X2 15
X3 11

X SWITCH

13 X

ANALOG INPUTS/OUTPUTS

Y0 1
Y1 5
Y2 2
Y3 4

Y SWITCH

3 Y

COMMON OUTPUTS/INPUTS

A 10
B 9

CHANNEL-SELECT INPUTS

ENABLE 6

PIN 16 = V_{CC}
PIN 7 = V_{EE}
PIN 8 = GND
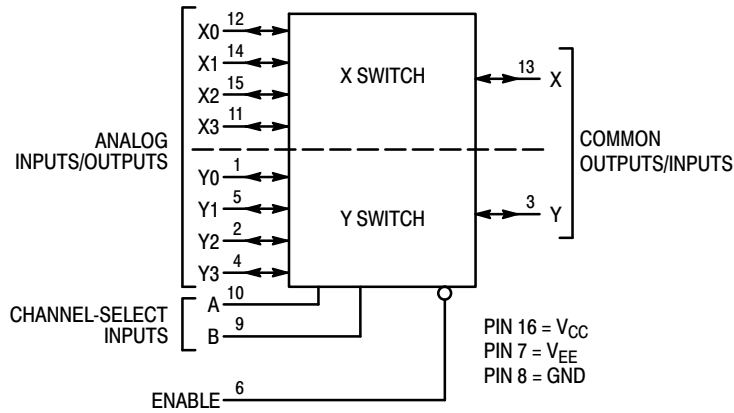
FUNCTION TABLE – MC74HC4052A

Control Inputs			ON Channels	
	Select			
Enable	B	A		
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

Pinout: MC74HC4052A (Top View)
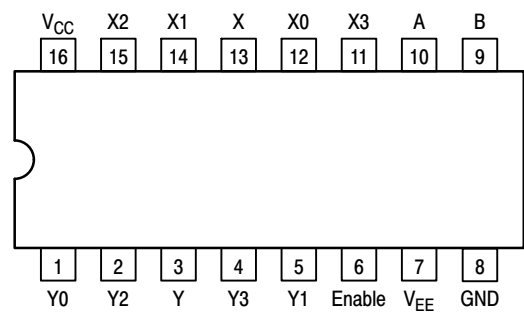
V_{CC}	X2	X1	X	X0	X3	A	B
16	15	14	13	12	11	10	9

1	2	3	4	5	6	7	8
Y0	Y2	Y	Y3	Y1	Enable	V_{EE}	GND

MC74HC4051A, MC74HC4052A, MC74HC4053A

LOGIC DIAGRAM
MC74HC4053A
Triple Single–Pole, Double–Position Plus Common Off

ANALOG INPUTS/OUTPUTS

COMMON OUTPUTS/INPUTS

CHANNEL-SELECT INPUTS

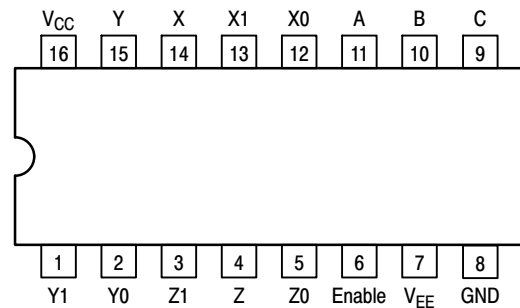PIN 16 = V_{CC}
PIN 7 = V_{EE}
PIN 8 = GND
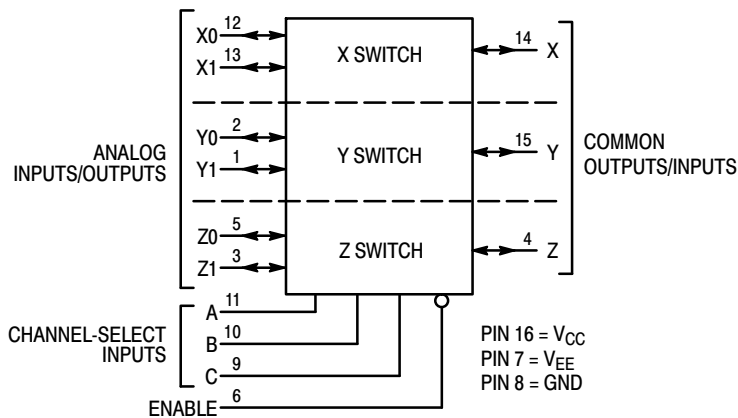
ENABLE

NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

FUNCTION TABLE – MC74HC4053A

Control Inputs						
	Select					
Enable	C	B	A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

Pinout: MC74HC4053A (Top View)

V_{CC}	Y	X	X1	X0	A	B	C
16	15	14	13	12	11	10	9

1	2	3	4	5	6	7	8
Y1	Y0	Z1	Z	Z0	Enable	V_{EE}	GND

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND) (Referenced to V_{EE})	$-$ 0.5 to $+$ 7.0 $-$ 0.5 to $+$ 14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)		$-$ 7.0 to $+$ 5.0	V
V_{IS}	Analog Input Voltage		V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	Digital Input Voltage (Referenced to GND)		$-$ 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin		$\pm$ 25	mA
P_D	Power Dissipation in Still Air,	Plastic DIP† EIAJ/SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature Range		$-$ 65 to $+$ 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
†Derating — Plastic DIP: $-$ 10 mW/°C from 65° to 125°C
EIAJ/SOIC Package: $-$ 7 mW/°C from 65° to 125°C
TSSOP Package: $-$ 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
		(Referenced to V_{EE})	2.0	12.0	
V_{EE}	Negative DC Supply Voltage, Output (Referenced to GND)		– 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch			1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 3.0 V	0	600	
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
I_{in}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{in} = V_{CC} or GND, V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND; V_{EE} = GND	6.0	1	10	20	μA
		V_{IO} = 0 V V_{EE} = – 6.0	6.0	4	40	80	

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V_{CC}	V_{EE}	Guaranteed Limit			Unit
					−55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = V_{CC}$ to V_{EE}; $I_S \leq 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 − 4.5 − 6.0	190 120 100	240 150 125	280 170 140	Ω
		$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = V_{CC}$ or V_{EE} (Endpoints); $I_S \leq 2.0$ mA (Figures 1, 2)	4.5 4.5 6.0	0.0 − 4.5 − 6.0	150 100 80	190 125 100	230 140 115	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = 1/2\,(V_{CC} - V_{EE})$; $I_S \leq 2.0$ mA	4.5 4.5 6.0	0.0 − 4.5 − 6.0	30 12 10	35 15 12	40 18 14	Ω
I_{off}	Maximum Off-Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or V_{IH}; $V_{IO} = V_{CC} - V_{EE}$; Switch Off (Figure 3)	6.0	− 6.0	0.1	0.5	1.0	µA
	Maximum Off-Channel Leakage Current, Common Channel HC4051A HC4052A HC4053A	$V_{in} = V_{IL}$ or V_{IH}; $V_{IO} = V_{CC} - V_{EE}$; Switch Off (Figure 4)	6.0 6.0 6.0	− 6.0 − 6.0 − 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	
I_{on}	Maximum On-Channel Leakage Current, Channel-to-Channel HC4051A HC4052A HC4053A	$V_{in} = V_{IL}$ or V_{IH}; Switch-to-Switch = $V_{CC} - V_{EE}$; (Figure 5)	6.0 6.0 6.0	− 6.0 − 6.0 − 6.0	0.2 0.1 0.1	2.0 1.0 1.0	4.0 2.0 2.0	µA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel-Select to Analog Output (Figure 9)	2.0 3.0 4.5 6.0	270 90 59 45	320 110 79 65	350 125 85 75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0 3.0 4.5 6.0	40 25 12 10	60 30 15 13	70 32 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	160 70 48 39	200 95 63 55	220 110 76 63	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0 3.0 4.5 6.0	245 115 49 39	315 145 69 58	345 155 83 67	ns
C_{in}	Maximum Input Capacitance, Channel-Select or Enable Inputs		10	10	10	pF
$C_{I/O}$	Maximum Capacitance Analog I/O		35	35	35	pF
	(All Switches Off) Common O/I: HC4051A HC4052A HC4053A		130 80 50	130 80 50	130 80 50	
	Feed-through		1.0	1.0	1.0	

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D)

			Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Figure 13)*	HC4051A HC4052A HC4053A	45 80 45	pF

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Limit* 25°C			Unit
					'51	'52	'53	
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f_{in} = 1MHz Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{OS}; Increase f_{in} Frequency Until dB Meter Reads –3dB; R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	80 80 80	95 95 95	120 120 120	MHz
–	Off–Channel Feed–through Isolation (Figure 7)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–50 –50 –50			dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–40 –40 –40			
–	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	$V_{in} \leq$ 1MHz Square Wave ($t_r = t_f$ = 6ns); Adjust R_L at Setup so that I_S = 0A; Enable = GND R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	25 105 135			mV_{PP}
		R_L = 10kΩ, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	35 145 190			
–	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to HC4051A)	f_{in} = Sine Wave; Adjust f_{in} Voltage to Obtain 0dBm at V_{IS} f_{in} = 10kHz, R_L = 600Ω, C_L = 50pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–50 –50 –50			dB
		f_{in} = 1.0MHz, R_L = 50Ω, C_L = 10pF	2.25 4.50 6.00	–2.25 –4.50 –6.00	–60 –60 –60			
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1kHz, R_L = 10kΩ, C_L = 50pF THD = $THD_{measured} - THD_{source}$ V_{IS} = 4.0V_{PP} sine wave V_{IS} = 8.0V_{PP} sine wave V_{IS} = 11.0V_{PP} sine wave	2.25 4.50 6.00	–2.25 –4.50 –6.00	0.10 0.08 0.05			%

*Limits not tested. Determined by design and verified by qualification.
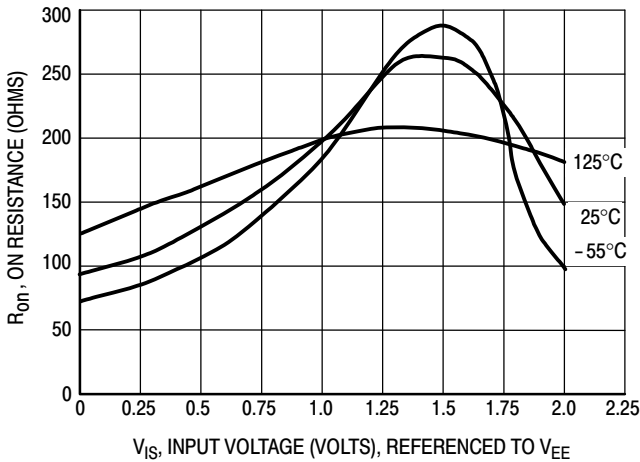
Figure 1a. Typical On Resistance, $V_{CC} - V_{EE}$ = 2.0 V
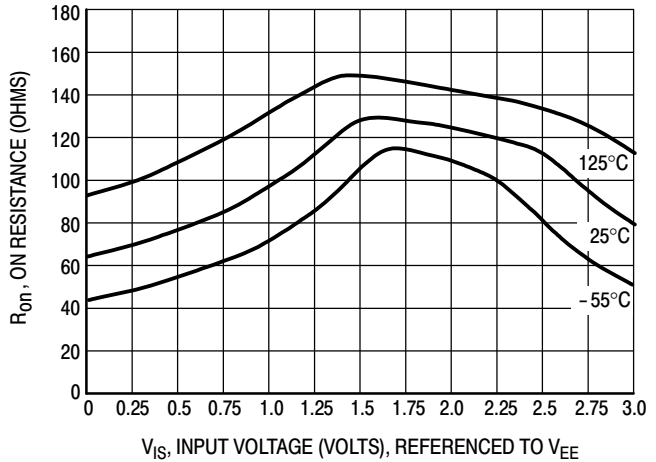
Figure 1b. Typical On Resistance, $V_{CC} - V_{EE}$ = 3.0 V
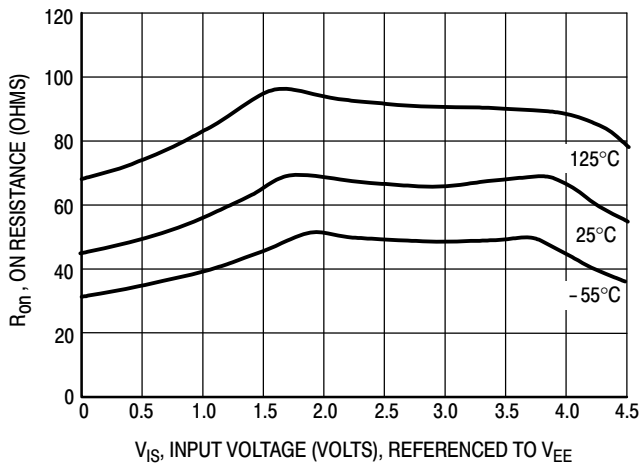
Figure 1c. Typical On Resistance, $V_{CC} - V_{EE}$ = 4.5 V
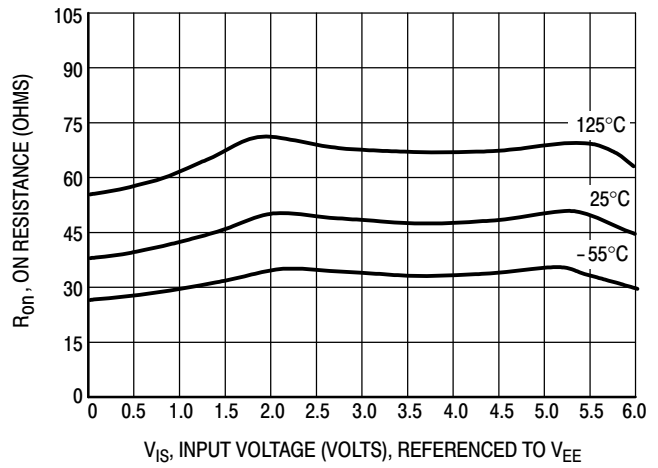
Figure 1d. Typical On Resistance, $V_{CC} - V_{EE}$ = 6.0 V
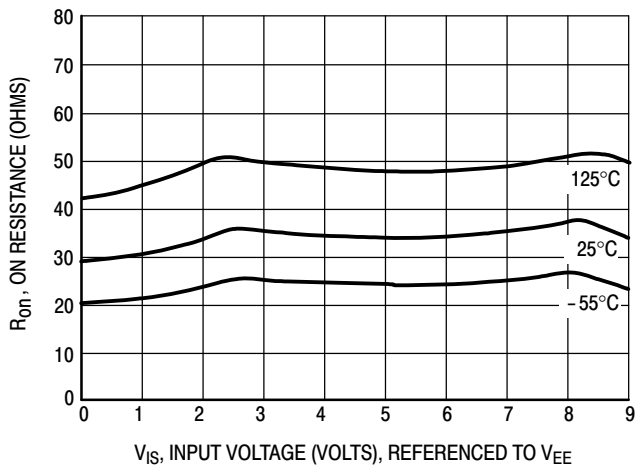
Figure 1e. Typical On Resistance, $V_{CC} - V_{EE}$ = 9.0 V
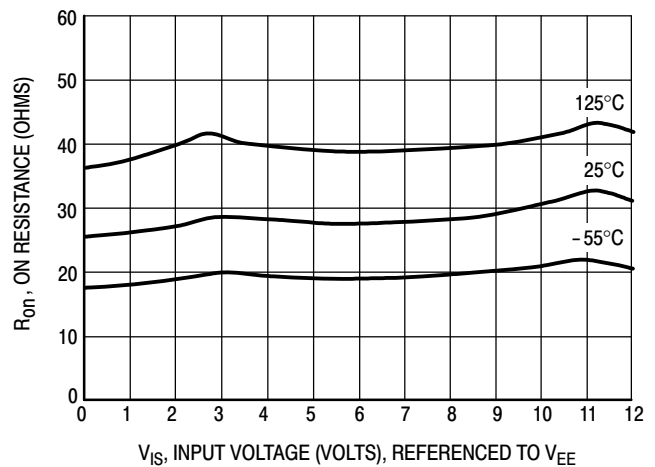
Figure 1f. Typical On Resistance, $V_{CC} - V_{EE}$ = 12.0 V
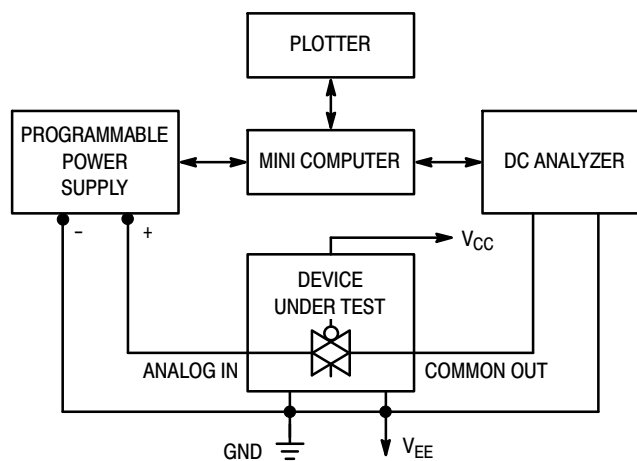
Figure 2. On Resistance Test Set–Up
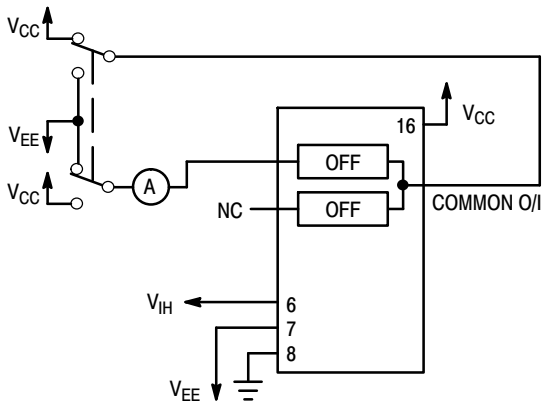
Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up
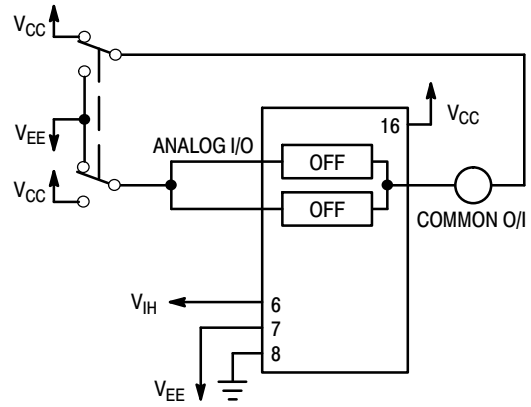
Figure 4. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up
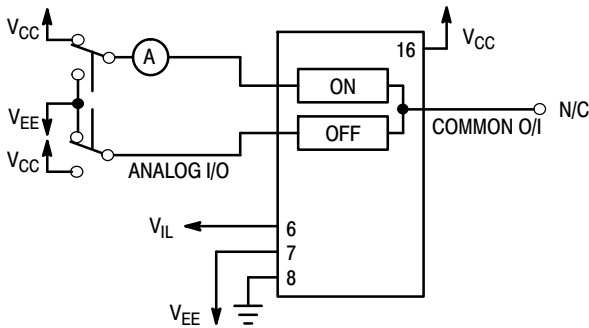
Figure 5. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

*Includes all probe and jig capacitance
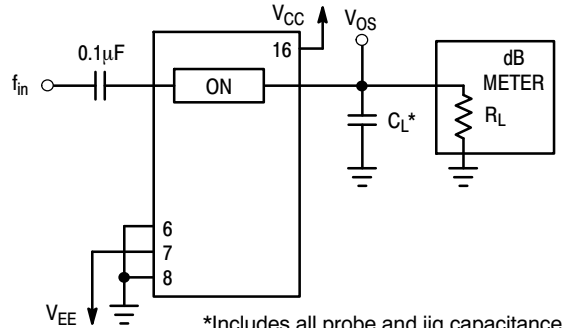
Figure 6. Maximum On Channel Bandwidth, Test Set–Up

*Includes all probe and jig capacitance
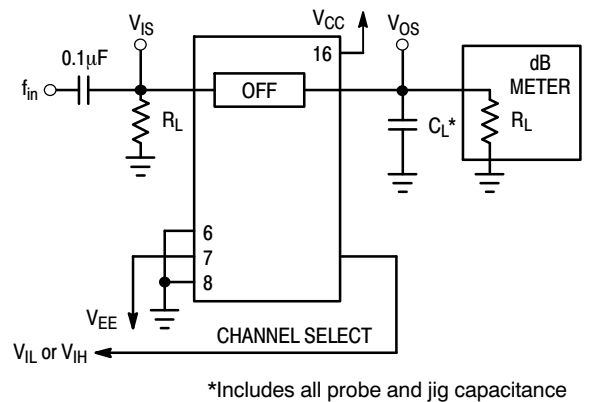
Figure 7. Off Channel Feedthrough Isolation, Test Set–Up

*Includes all probe and jig capacitance
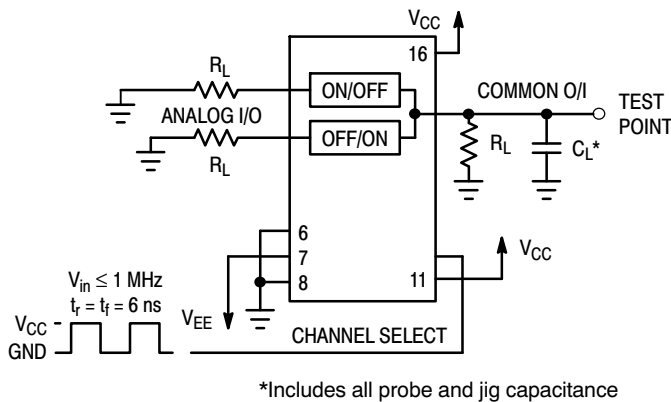
Figure 8. Feedthrough Noise, Channel Select to Common Out, Test Set–Up
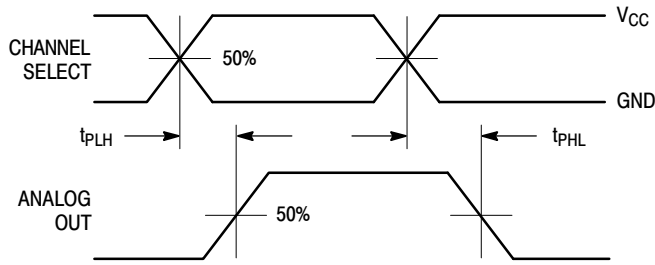
Figure 9a. Propagation Delays, Channel Select to Analog Out
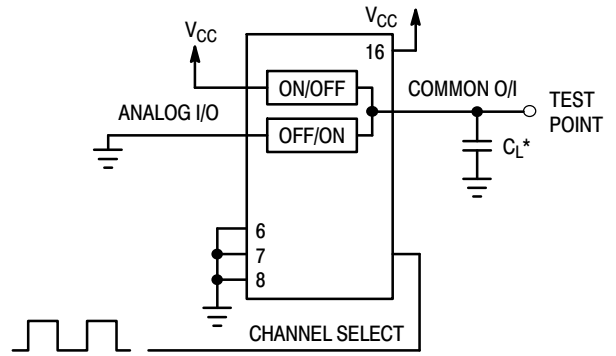
*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set−Up Channel Select to Analog Out
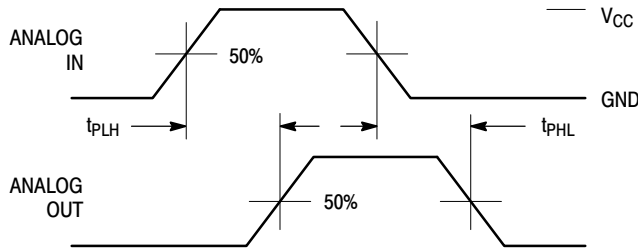
Figure 10a. Propagation Delays, Analog In to Analog Out
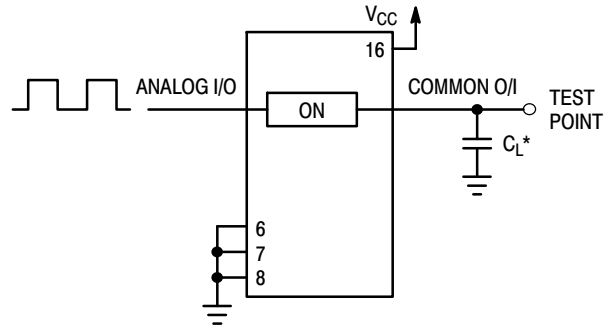
*Includes all probe and jig capacitance

Figure 10b. Propagation Delay, Test Set−Up Analog In to Analog Out
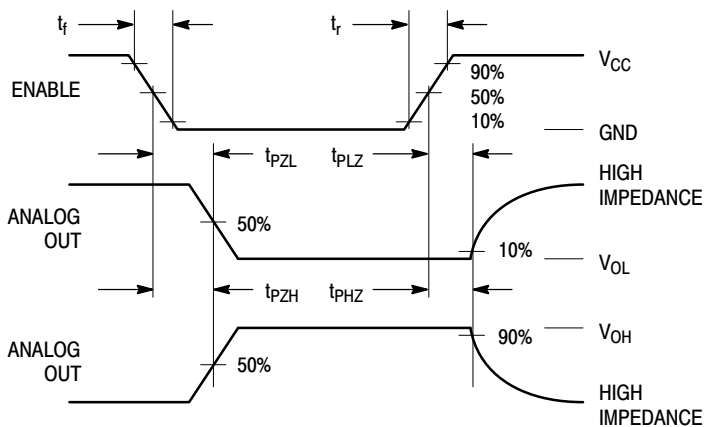
Figure 11a. Propagation Delays, Enable to Analog Out
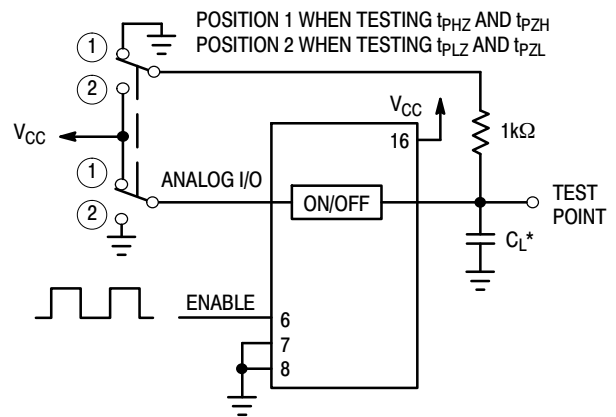
Figure 11b. Propagation Delay, Test Set−Up Enable to Analog Out
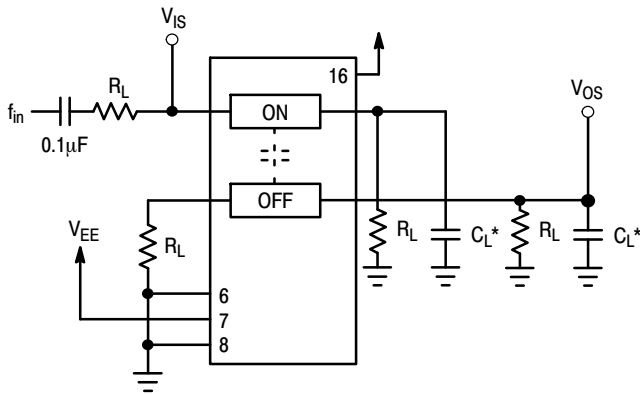
Figure 12. Crosstalk Between Any Two
Switches, Test Set–Up
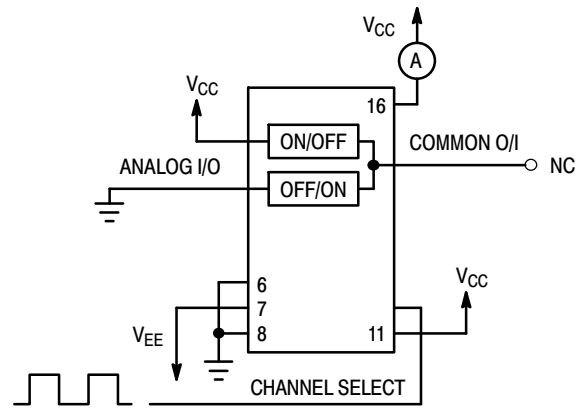
Figure 13. Power Dissipation Capacitance,
Test Set–Up
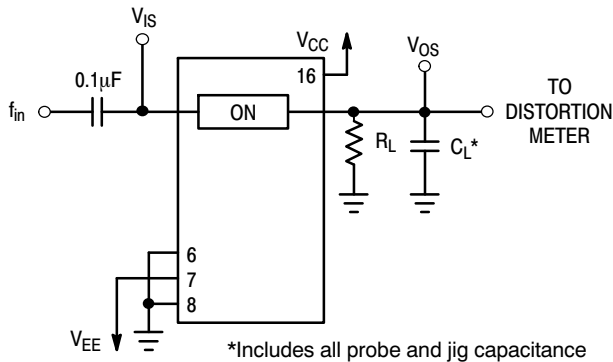
Figure 14a. Total Harmonic Distortion, Test Set–Up
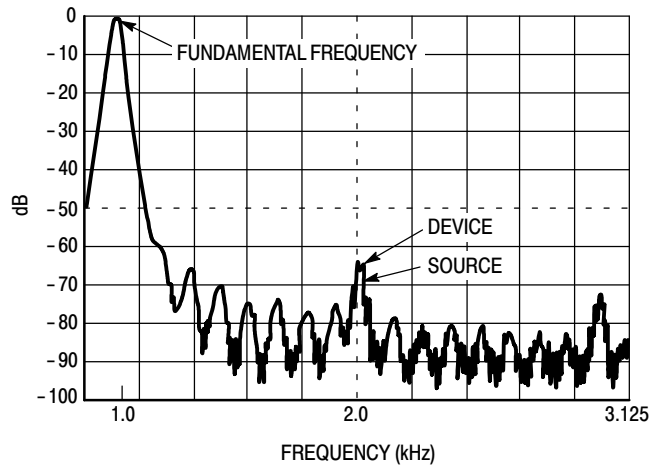
Figure 14b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5V = \text{logic high}$$
$$GND = 0V = \text{logic low}$$

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak–to–peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feed–through noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{CC} - GND = 2 \text{ to } 6 \text{ volts}$$
$$V_{EE} - GND = 0 \text{ to } -6 \text{ volts}$$
$$V_{CC} - V_{EE} = 2 \text{ to } 12 \text{ volts}$$
$$\text{and } V_{EE} \leq GND$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.
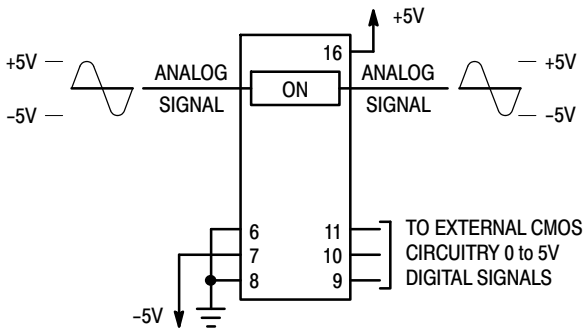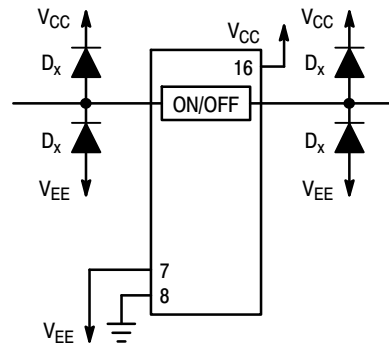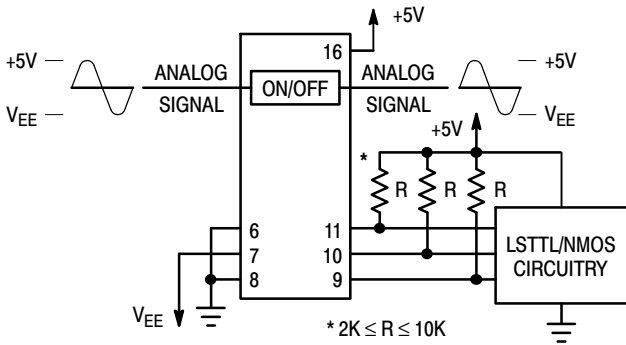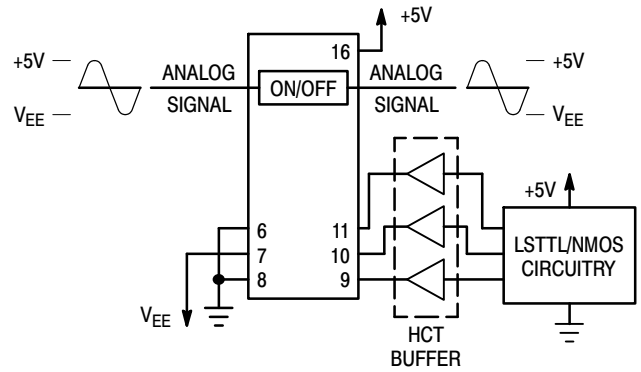
Figure 15. Application Example

Figure 16. External Germanium or Schottky Clipping Diodes

a. Using Pull−Up Resistors

* 2K ≤ R ≤ 10K

b. Using HCT Interface

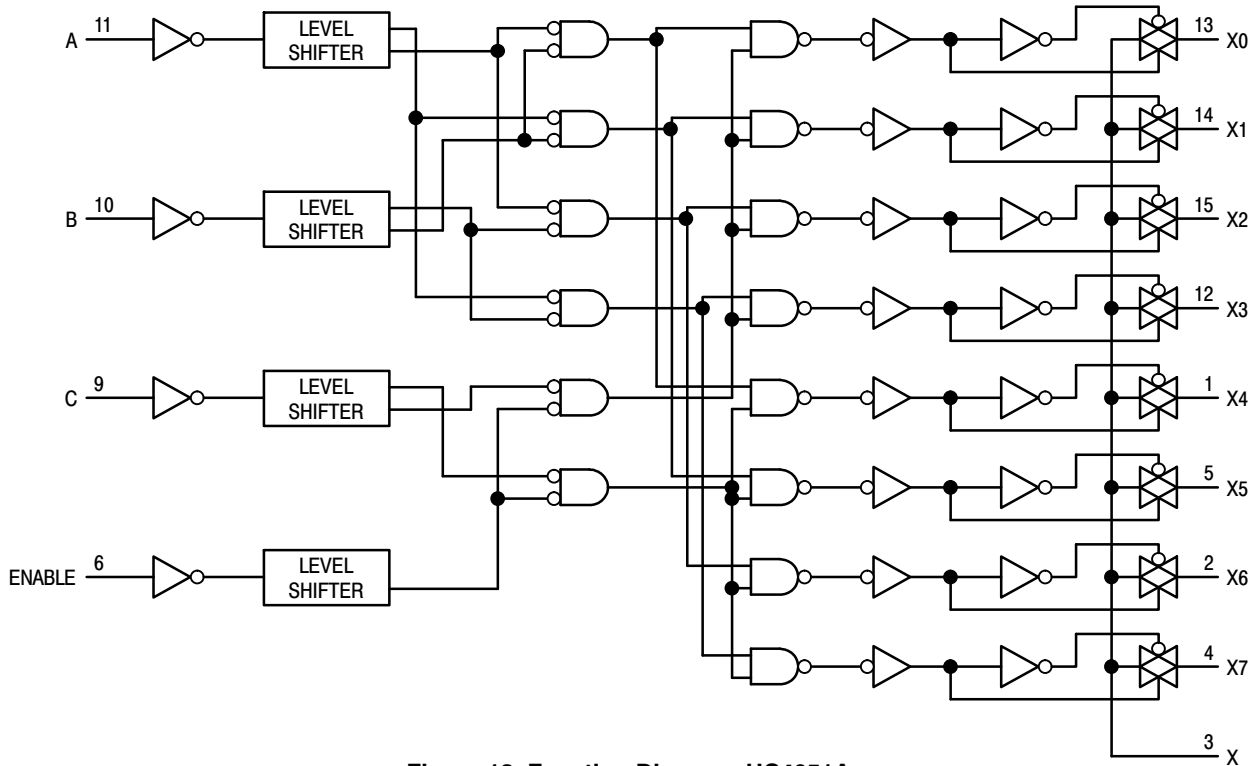Figure 17. Interfacing LSTTL/NMOS to CMOS Inputs

Figure 18. Function Diagram, HC4051A
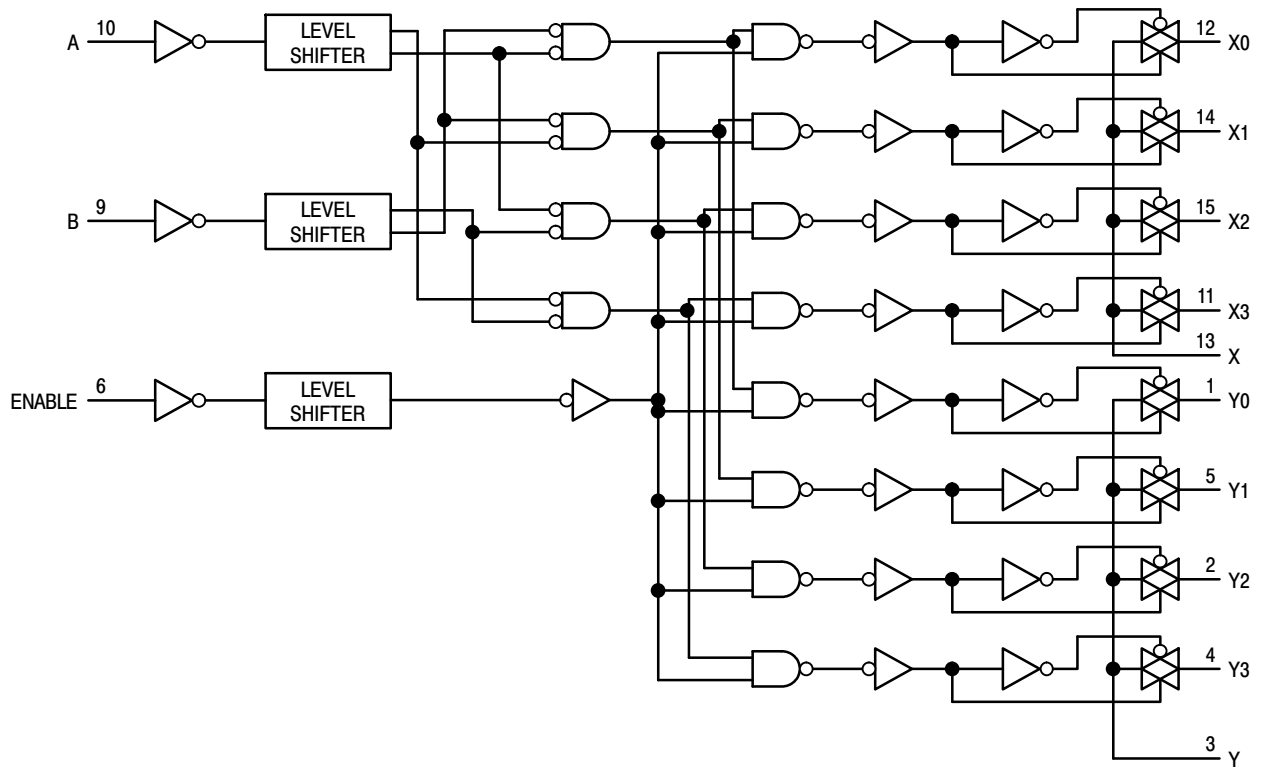
MC74HC4051A, MC74HC4052A, MC74HC4053A

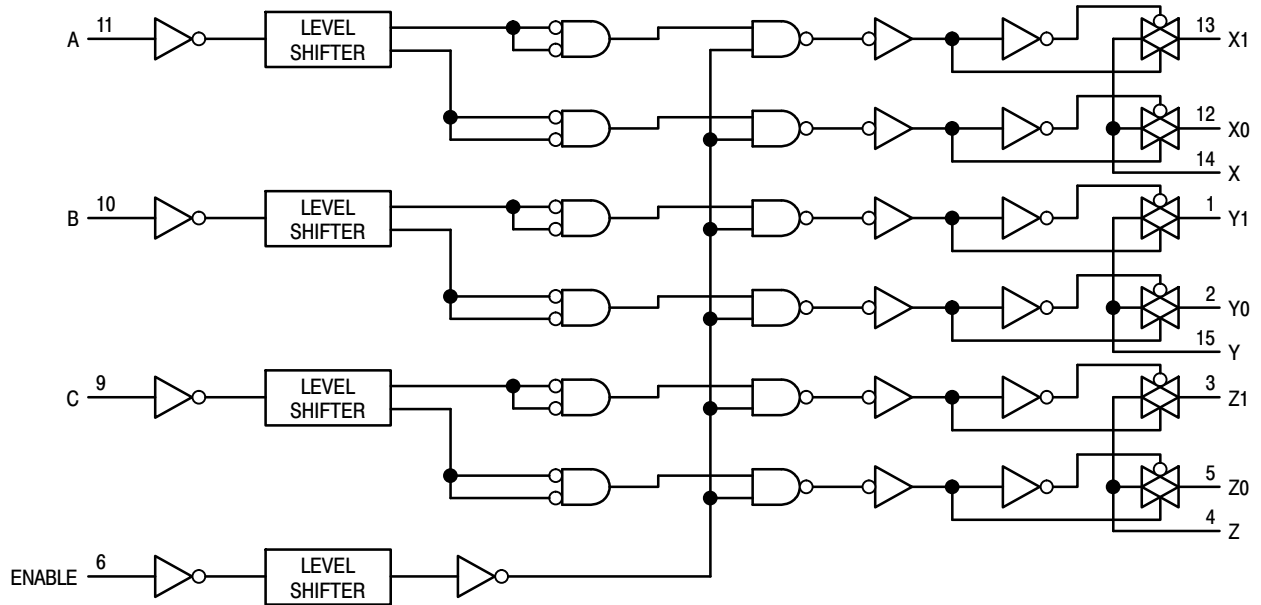**Figure 19. Function Diagram, HC4052A**

Figure 20. Function Diagram, HC4053A

MC74HC4051A, MC74HC4052A, MC74HC4053A

ORDERING INFORMATION

| Device	Package	Shipping[†]
MC74HC4051AN	PDIP–16	500 Units / Box
MC74HC4051ANG	PDIP–16 (Pb–Free)	500 Units / Box
MC74HC4051AD	SOIC–16	48 Units / Rail
MC74HC4051ADG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74HC4051ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4051ADR2G	SOIC–16 (Pb–Free)	2500 Units / Tape & Reel
MC74HC4051ADT	TSSOP–16*	96 Units / Rail
MC74HC4051ADTG	TSSOP–16*	96 Units / Rail
MC74HC4051ADTR2	TSSOP–16*	2500 Units / Tape & Reel
MC74HC4051ADTR2G	TSSOP–16*	2500 Units / Tape & Reel
MC74HC4051ADW	SOIC–16 WIDE	48 Units / Rail
MC74HC4051ADWG	SOIC–16 WIDE (Pb–Free)	48 Units / Rail
MC74HC4051ADWR2	SOIC–16 WIDE	1000 Units / Tape & Reel
MC74HC4051ADWR2G	SOIC–16 WIDE (Pb–Free)	1000 Units / Tape & Reel
MC74HC4051AFEL	SOEIAJ–16	2000 Units / Tape & Reel
MC74HC4051AFELG	SOEIAJ–16 (Pb–Free)	2000 Units / Tape & Reel
MC74HC4052AN	PDIP–16	500 Units / Box
MC74HC4052ANG	PDIP–16 (Pb–Free)	500 Units / Box
MC74HC4052AD	SOIC–16	48 Units / Rail
MC74HC4052ADG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74HC4052ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4052ADR2G	SOIC–16 (Pb–Free)	2500 Units / Tape & Reel
MC74HC4052ADT	TSSOP–16*	96 Units / Rail
MC74HC4052ADTG	TSSOP–16*	96 Units / Rail
MC74HC4052ADTR2	TSSOP–16*	2500 Units / Tape & Reel
MC74HC4052ADTR2G	TSSOP–16*	2500 Units / Tape & Reel
MC74HC4052ADW	SOIC–16 WIDE	48 Units / Rail
MC74HC4052ADWG	SOIC–16 WIDE (Pb–Free)	48 Units / Rail
MC74HC4052ADWR2	SOIC–16 WIDE	1000 Units / Tape & Reel
MC74HC4052ADWR2G	SOIC–16 WIDE (Pb–Free)	1000 Units / Tape & Reel
MC74HC4052AFG	SOEIAJ–16 (Pb–Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb–Free.

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC4053AN	PDIP–16	500 Units / Box
MC74HC4053ANG	PDIP–16 (Pb–Free)	500 Units / Box
MC74HC4053AD	SOIC–16	48 Units / Rail
MC74HC4053ADG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74HC4053ADR2	SOIC–16	2500 Units / Tape & Reel
MC74HC4053ADR2G	SOIC–16 (Pb–Free)	2500 Units / Tape & Reel
MC74HC4053ADT	TSSOP–16*	96 Units / Rail
MC74HC4053ADTG	TSSOP–16*	96 Units / Rail
MC74HC4053ADTR2	TSSOP–16*	2500 Units / Tape & Reel
MC74HC4053ADTR2G	TSSOP–16*	2500 Units / Tape & Reel
MC74HC4053ADW	SOIC–16 WIDE	48 Units / Rail
MC74HC4053ADWG	SOIC–16 WIDE (Pb–Free)	48 Units / Rail
MC74HC4053ADWR2	SOIC–16 WIDE	1000 Units / Tape & Reel
MC74HC4053ADWR2G	SOIC–16 WIDE (Pb–Free)	1000 Units / Tape & Reel
MC74HC4053AF	SOEIAJ–16	50 Units / Rail
MC74HC4053AFG	SOEIAJ–16 (Pb–Free)	50 Units / Rail
MC74HC4053AFEL	SOEIAJ–16	2000 Units / Tape & Reel
MC74HC4053AFELG	SOEIAJ–16 (Pb–Free)	2000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb–Free.

PACKAGE DIMENSIONS

PDIP–16
N SUFFIX
CASE 648–08
ISSUE T
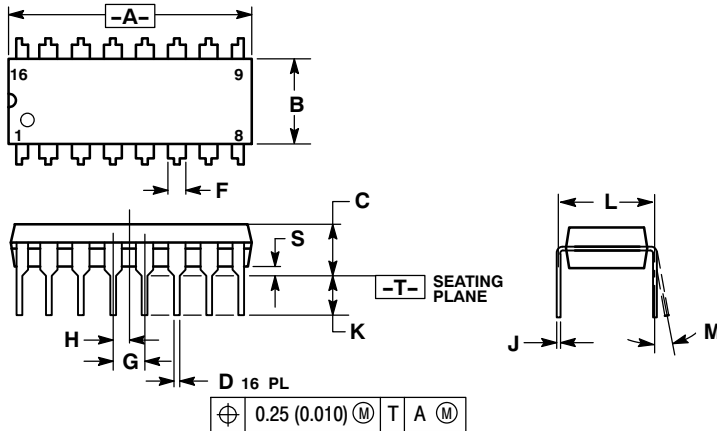
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
---	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOIC–16 WIDE
DW SUFFIX
CASE 751G–03
ISSUE C
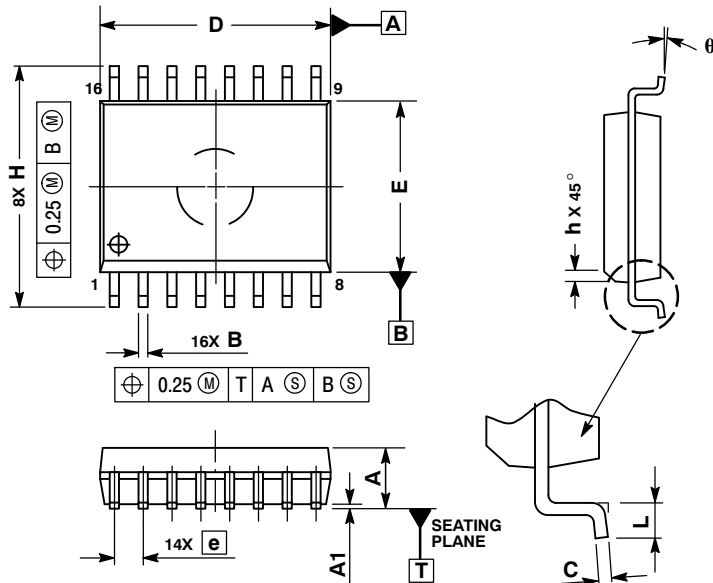
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
---	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 °	7 °

PACKAGE DIMENSIONS

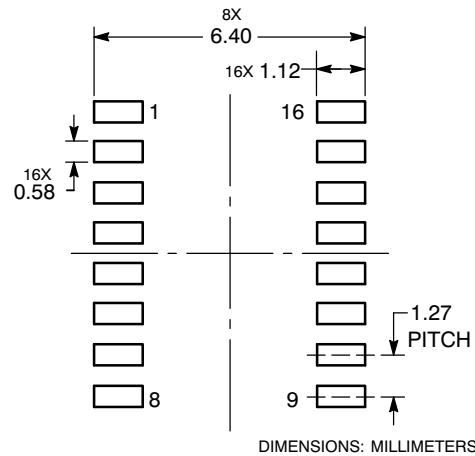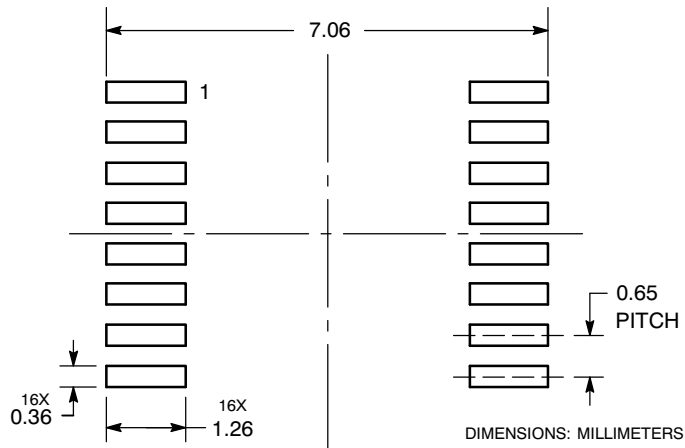**SOIC–16**
D SUFFIX
CASE 751B–05
ISSUE K
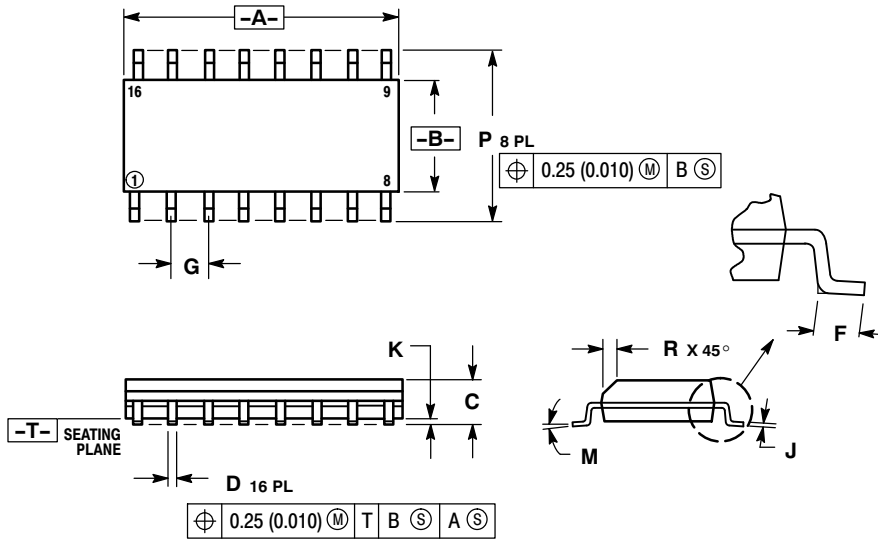
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP−16
DT SUFFIX
CASE 948F−01
ISSUE B
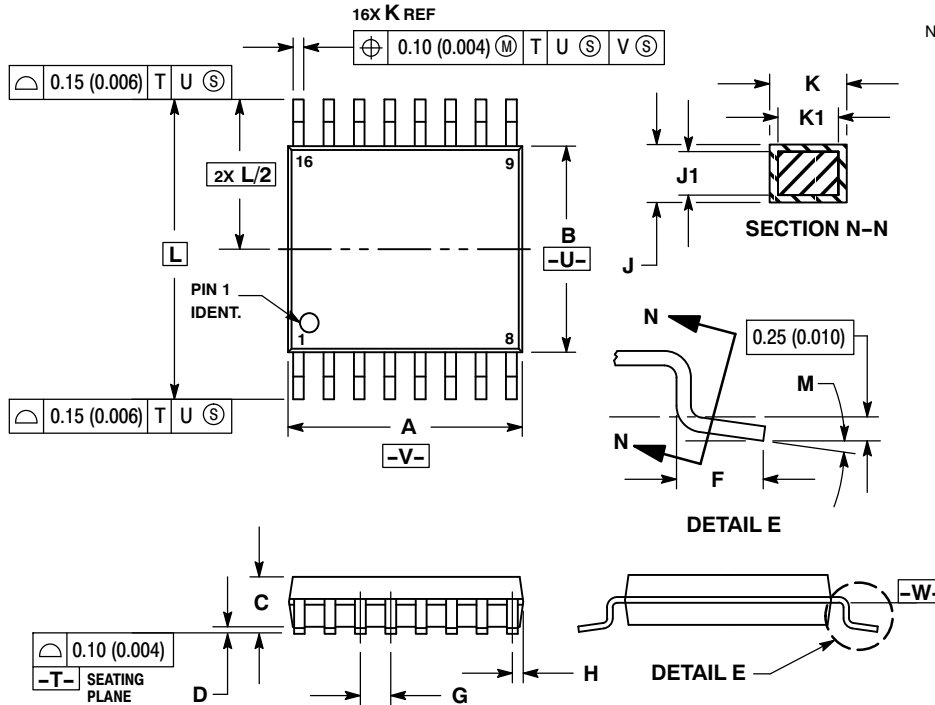
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SECTION N−N

DETAIL E

SOLDERING FOOTPRINT*

7.06

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOEIAJ–16
F SUFFIX
CASE 966–01
ISSUE A
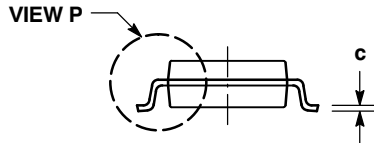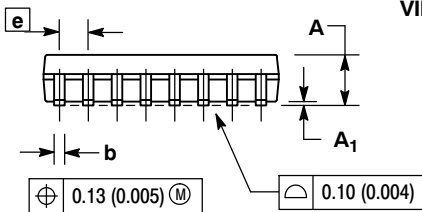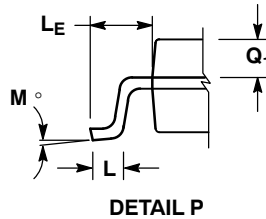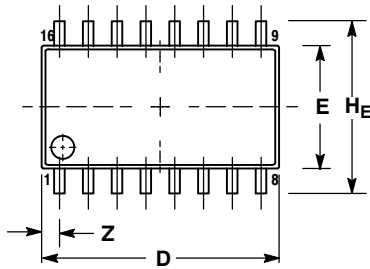
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031