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Hex Inverter

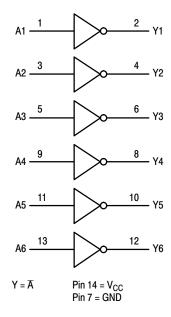
With LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT04A may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs. The HCT04A is identical in pinout to the LS04.

Features

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μA
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 48 FETs or 12 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

LOGIC DIAGRAM





ON Semiconductor®

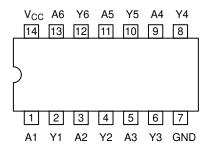
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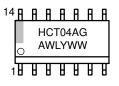
SOIC-14 NB D SUFFIX CASE 751A TSSOP-14 DT SUFFIX CASE 948G

PIN ASSIGNMENT



14-Lead (Top View)

MARKING DIAGRAMS





SOIC-14 NB

TSSOP-14

A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs	Outputs
Α	Υ
L	Н
н	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I _{in}	DC Input Current, per Pin	±20	mA
l _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C TSSOP Package: -6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature Range, All Package Types	- 55	+125	°C
t _r , t _f	Input Rise/Fall Time (Figure 1)	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS (Voltages Referenced to GND)

			Vcc	Guaranteed Limit			
Symbol	Parameter	Condition	v	–55 to 25°C	≤85°C	≤125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1V$ $ I_{out} \le 20\mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	٧
V _{IL}	Maximum Low-Level Input Voltage	$\begin{aligned} V_{out} &= V_{CC} - 0.1V \\ I_{out} &\leq 20 \mu A \end{aligned}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	٧
V _{OH}	Minimum High-Level Output Voltage	$\begin{aligned} &V_{in} = V_{IL} \\ & I_{out} \leq 20 \mu A \end{aligned}$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IL}$ $ I_{out} \le 4.0 \text{mA}$	4.5	3.98	3.84	3.70	
V _{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out} \le 20\mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \le 4.0 \text{mA}$	4.5	0.26	0.33	0.40	
l _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	5.5	1	10	40	μΑ
ΔI_{CC}	Additional Quiescent Supply Current	V _{in} = 2.4V, Any One Input V _{in} = V _{CC} or GND, Other Inputs		≥ –55 °C	25 to	125°C	
	Ourient	$I_{out} = 0\mu A$	5.5	2.9	2	.4	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

AC CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, $C_L = 50pF$, Input $t_r = t_f = 6ns$)

		Guaranteed Limit			
Symbol	Parameter	-55 to 25°C	≤85°C	≤125°C	Unit
t _{PLH} ,	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	15 17	19 21	22 26	ns
t _{TLH} ,	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	22	pF

^{*} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

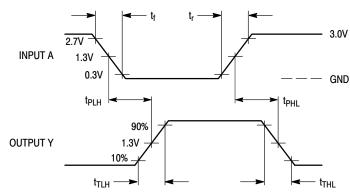
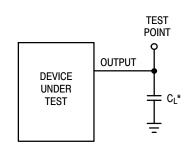


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

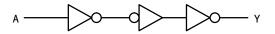


Figure 3. Expanded Logic Diagram (1/6 of the Device Shown)

ORDERING INFORMATION

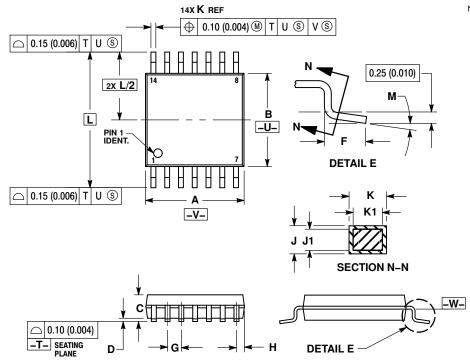
Device	Package	Shipping [†]
MC74HCT04ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HCT04ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
MC74HCT04ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HCT04ADG*	SOIC-14 NB (Pb-Free)	55 Units / Rail
NLV74HCT04ADR2G*	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel
NLV74HCT04ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

TSSOP-14 CASE 948G **ISSUE B**



- JIES:

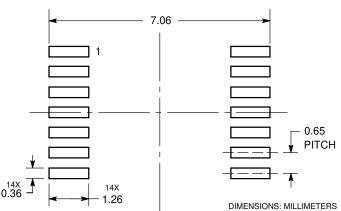
 1. DIMENSIONING AND TOLERANCING PER
 ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD
 FLASH, PROTRUSIONS OR GATE BURRS.
 MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL
- NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE
 DAMBAR PROTRUSION. ALLOWABLE
 DAMBAR PROTRUSION SHALL BE 0.08
 (0.003) TOTAL IN EXCESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL
 CONDITION.
- CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
Κ	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252 BSC	
М	0 °	8 °	0 °	8 °

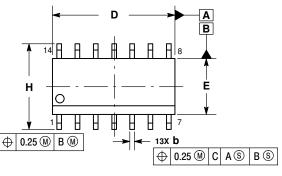
SOLDERING FOOTPRINT*



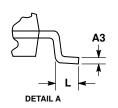
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

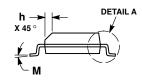
PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 ISSUE K



е



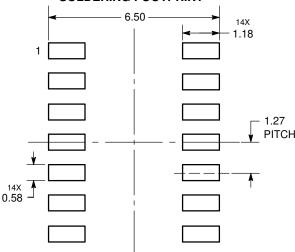


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
- 2. CON I HOLLING DIMENSION: MILLIME I ERS.
 3. DIMENSION & DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE PROTRUSION
 SHALL BE 0.13 TOTAL IN EXCESS OF AT
 MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE
- MOLD PROTRUSIONS.
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
А3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
е	1.27	1.27 BSC		BSC
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
М	0 °	7°	0 °	7°

SOLDERING FOOTPRINT*

C SEATING PLANE



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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