Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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MC74LVX139

Dual 2-to-4 Decoder/ Demultiplexer

The MC74LVX139 is an advanced high speed CMOS 2–to–4 decoder/ demultiplexer fabricated with silicon gate CMOS technology.

When the device is enabled ($\overline{E}$ = low), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

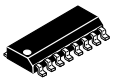
- High Speed: t_{PD} = 6.0 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise: V_{OLP} = 0.5 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
- Pb–Free Packages are Available*

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

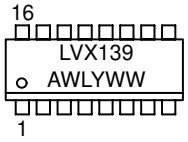
ON Semiconductor®

http://onsemi.com

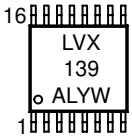
MARKING DIAGRAMS

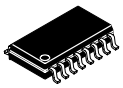


SOIC–16
D SUFFIX
CASE 751B

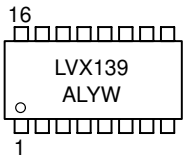


TSSOP–16
DT SUFFIX
CASE 948F





SOEIAJ–16
M SUFFIX
CASE 966



A	=	Assembly Location
WL or L	=	Wafer Lot
Y	=	Year
WW or W	=	Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

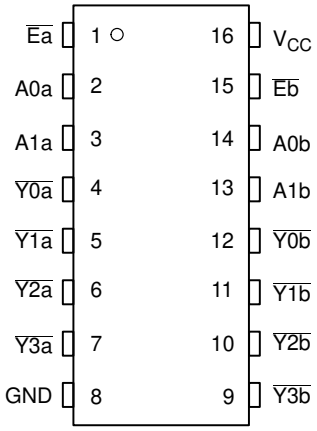


Figure 1. Pin Assignment

FUNCTION TABLE

Inputs			Outputs			
$\overline{E}$	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

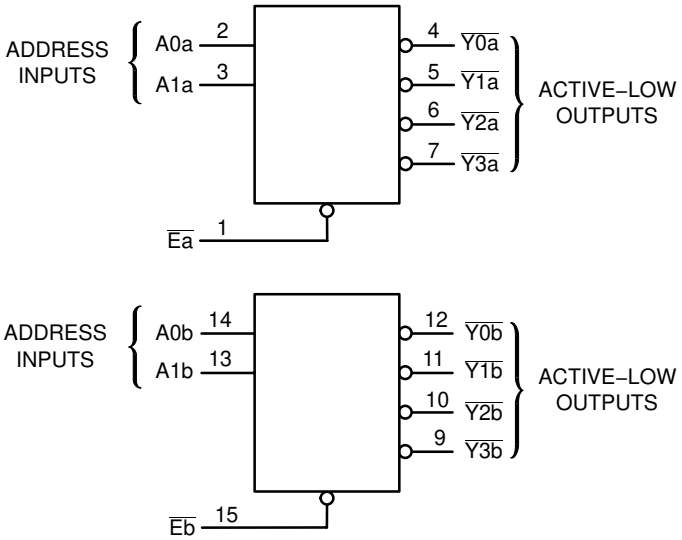


Figure 2. Logic Diagram

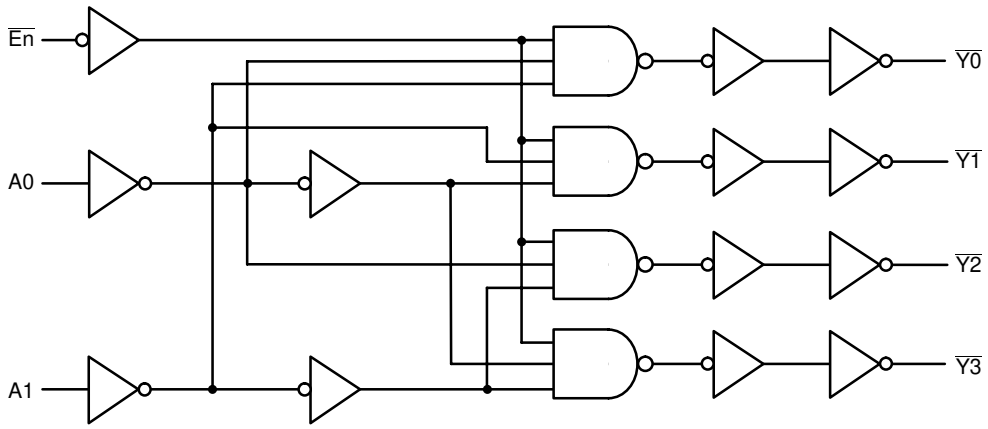


Figure 3. Expanded Logic Diagram
(1/2 of Device)

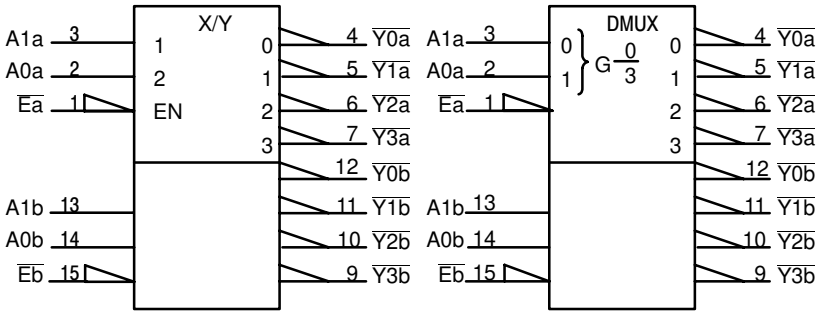


Figure 4. IEC Logic Diagram

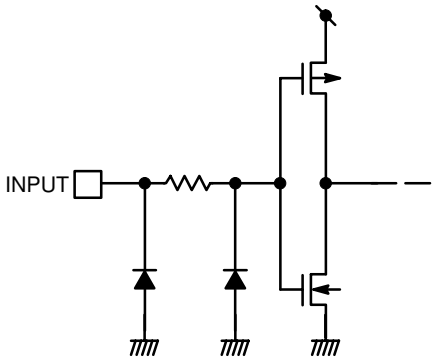


Figure 5. Input Equivalent Circuit

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		–0.5 to +7.0	V
V_{IN}	Digital Input Voltage		–0.5 to +7.0	V
V_{OUT}	DC Output Voltage		–0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		–20	mA
I_{OK}	Output Diode Current		± 20	mA
I_{OUT}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
T_{STG}	Storage Temperature Range		–65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >200 >2000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4)	± 300	mA
θ_{JA}	Thermal Resistance, Junction–to–Ambient	SOIC Package TSSOP	143 164	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22–A114–A
2. Tested to EIA/JESD22–A115–A
3. Tested to JESD22–C101–A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	3.6	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage	Output in 3–State High or Low State	0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types		–40	85	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 5.0 V ± 0.5 V	0	100	ns/V

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	–40°C ≤ T_A ≤ 85°C Min	–40°C ≤ T_A ≤ 85°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 3.6	0.75 V_{CC} 0.7 V_{CC} 0.7 V_{CC}	– – –	– – –	0.75 V_{CC} 0.7 V_{CC} 0.7 V_{CC}	– – –	V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 3.6	– – –	– – –	0.25 V_{CC} 0.3 V_{CC} 0.3 V_{CC}	– – –	0.25 V_{CC} 0.3 V_{CC} 0.3 V_{CC}	V
V_{OH}	High–Level Output Voltage	I_{OH} = –50 μA I_{OH} = –50 μA I_{OH} = –4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 3.0	– – –	1.9 2.9 2.48	– – –	V
V_{OL}	Low–Level Output Voltage	I_{OL} = 50 μA I_{OH} = 50 μA I_{OH} = 4 mA	2.0 3.0 3.0	– – –	0.0	0.1 0.1 0.36	– – –	0.1 0.1 0.44	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 3.6	–	–	±0.1	–	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_{IN} = V_{CC} or GND	3.6	1.0	1.0	2.0	–	–	μA

AC ELECTRICAL CHARACTERISTICS Input $t_r = t_f$ = 3.0 ns

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	–40°C ≤ T_A ≤ 85°C Min	–40°C ≤ T_A ≤ 85°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to Y	V_{CC} = 2.7 V	C_L = 15 pF C_L = 50 pF	– –	8.5 11.0	15.0 16.5	1.0 1.0	17.8 18.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15 pF C_L = 50 pF	– –	6.0 8.5	10.0 13.0	1.0 1.0	12.0 15.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{E}$ to Y	V_{CC} = 2.7 V	C_L = 15 pF C_L = 50 pF	– –	8.0 10.0	13.0 16.5	1.0 1.0	15.5 18.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15 pF C_L = 50 pF	– –	5.5 7.5	8.2 13.0	1.0 1.0	10.0 15.0	
C_{IN}	Maximum Input Capacitance			–	4	10	–	10	pF
				Typical @ 25°C, V_{CC} = 3.3 V					
C_{PD}	Power Dissipation Capacitance (Note 5)			26					pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per decoder). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

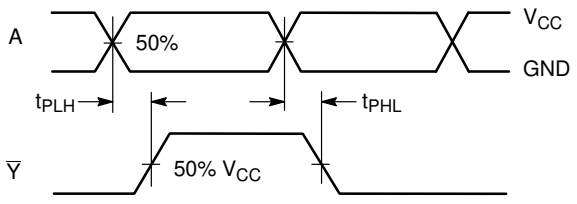


Figure 6. Switching Waveform

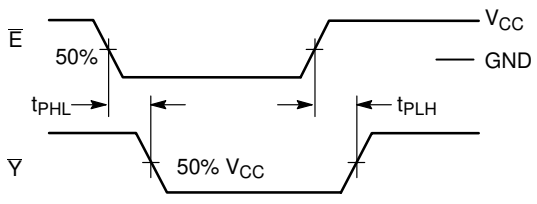
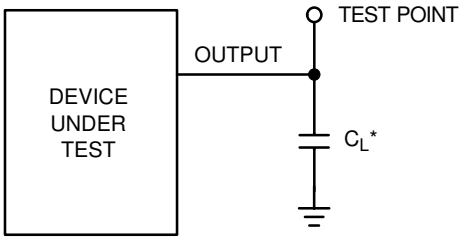


Figure 7. Switching Waveform



*Includes all probe and jig capacitance

Figure 8. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX139DR2	SOIC−16	2500 Tape & Reel
MC74LVX139DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74LVX139DTR2	TSSOP−16*	2500 Tape & Reel
MC74LVX139M	SOEIAJ−16	50 Units / Rail
MC74LVX139MG	SOEIAJ−16 (Pb−Free)	50 Units / Rail
MC74LVX139MEL	SOEIAJ−16	2000 Tape & Reel
MC74LVX139MELG	SOEIAJ−16 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

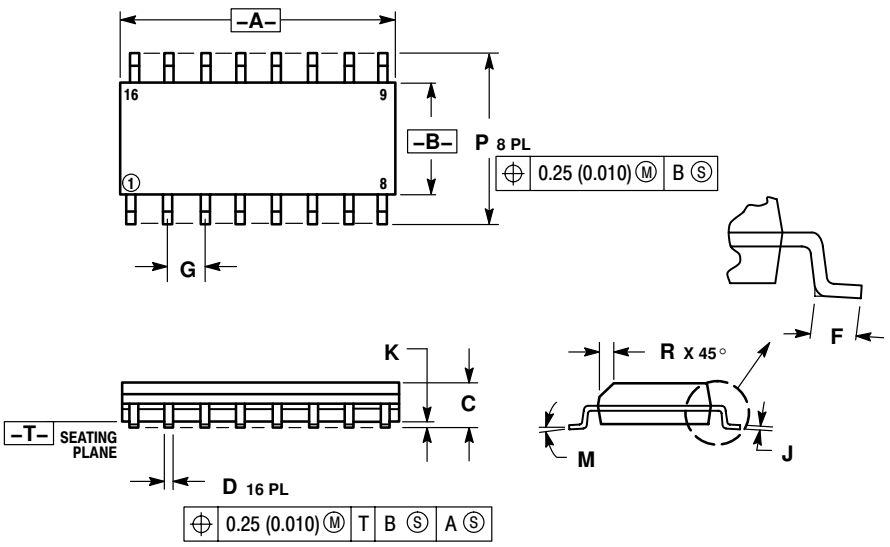
EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 −0.0 (0.059" +0.004 −0.0)	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

6. Metric Dimensions Govern−English are in parentheses for reference only.
7. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

PACKAGE DIMENSIONS

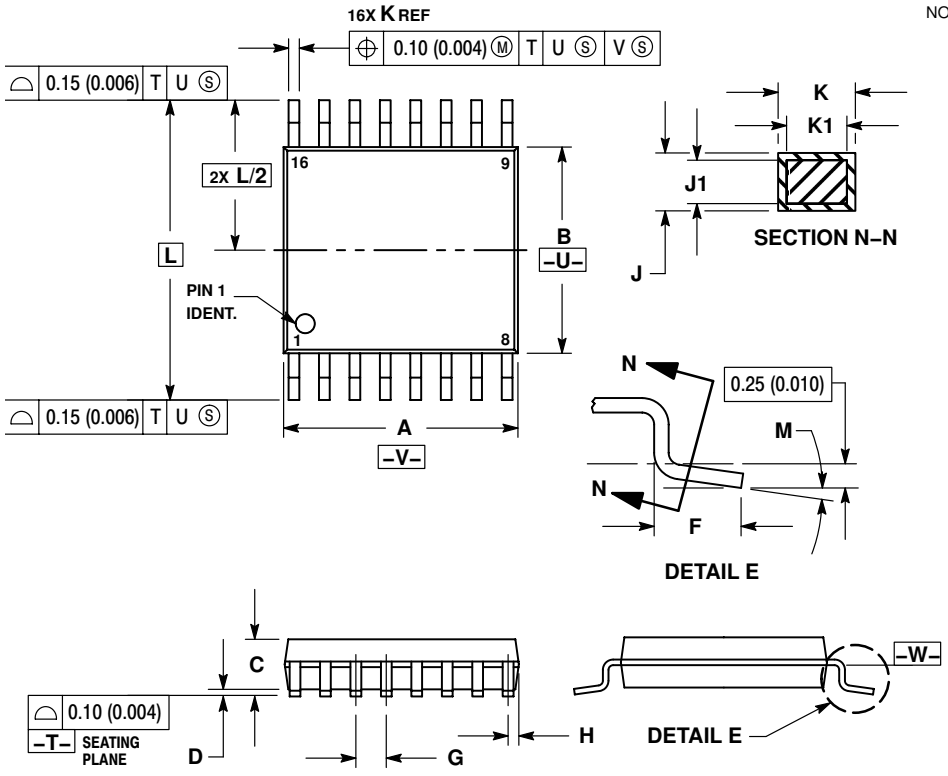
SOIC–16
D SUFFIX
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

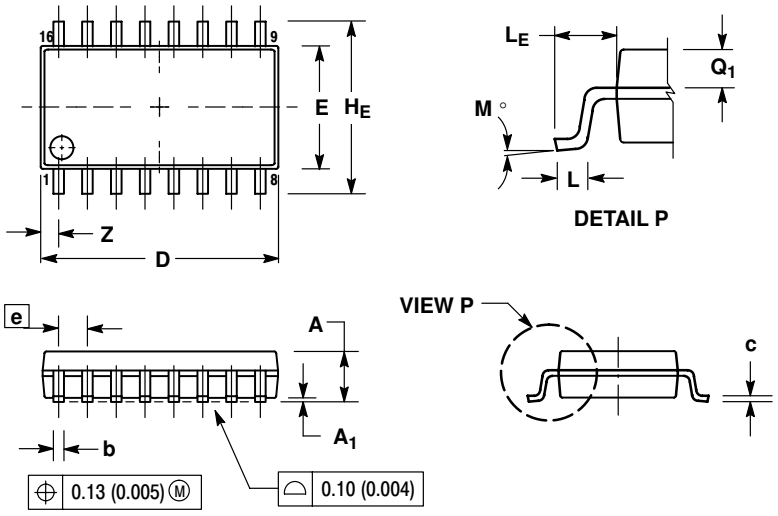
TSSOP–16
DT SUFFIX
CASE 948F–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOEIAJ–16
M SUFFIX
CASE 966–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

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MC74LVX139/D