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MC68HC908AP64
MC68HC908AP32
MC68HC908AP16
MC68HC908AP8

Data Sheet

M68HC08
Microcontrollers

MC68HC908AP64
Rev. 4
01/2007

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MC68HC908AP64
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Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
January 2007	4	15.7.2 ADC Clock Control Register — Changed “The ADC clock should be set to between 500kHz and 2MHz” to “The ADC clock should be set to between 500kHz and 1MHz”	254
August 2005	3	Table 22-4 . DC Electrical Characteristics (5V) — Updated V_{OL} values.	299
		Table 22-6 . Oscillator Specifications (5V) and Table 22-10 . Oscillator Specifications (3V) — Corrected internal oscillator clock frequency, f_{ICLK}. Updated crystal oscillator component values C_L, C_1, C_2, R_B, and R_S.	301, 305
October 2003	2.5	Added MC68HC908AP16/AP8 information throughout.	—
		Section 10. Monitor ROM (MON) — Corrected RAM address to $60.	167
		Section 24. Electrical Specifications — Added run and wait I_{DD} data for 8MHz at 3V.	421
August 2003	2.4	Section 24. Electrical Specifications — Updated stop I_{DD} data.	417, 421
July 2003	2.3	Removed MC68HC908AP16 references throughout.	—
		Table 1-2 . Pin Functions — Added footnote for V_{REG}.	30
		5.3 Configuration Register 1 (CONFIG1) — Clarified LVIPWRD and LVIREGD bits.	67
		Section 8. Clock Generator Module (CGM), 8.7.2 Stop Mode — Updated BSC bit behavior.	125
		10.5 ROM-Resident Routines — Corrected data size limits and control byte size for EE_READ and EE_WRITE.	168–193
		Figure 12-2 . Timebase Control Register (TBCR) — Corrected register address.	207
		Section 24. Electrical Specifications — Updated.	415
May 2003	2.2	Updated for f_{NOM} = 125kHz and filter components in CGM section.	101
		Updated electricals.	415

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Chapter 1
General Description

1.1 Introduction

The MC68HC908AP64 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Table 1-1. Summary of Device Variations

Device	RAM Size (bytes)	FLASH Memory Size (bytes)
MC68HC908AP64	2,048	62,368
MC68HC908AP32	2,048	32,768
MC68HC908AP16	1,024	16,384
MC68HC908AP8	1,024	8,192

1.2 Features

Features of the MC68HC908AP64 include the following:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- Maximum internal bus frequency:
  - 8-MHz at 5V or 3V operating voltage
- Clock input options:
  - RC-oscillator
  - 32-kHz crystal-oscillator with 32MHz internal PLL
- User program FLASH memory with security[1] feature
  - 62,368 bytes for MC68HC908AP64
  - 32,768 bytes for MC68HC908AP32
  - 16,384 bytes for MC68HC908AP16
  - 8,192 bytes for MC68HC908AP8
- On-chip RAM
  - 2,048 bytes for MC68HC908AP64 and MC68HC908AP32
  - 1,024 bytes for MC68HC908AP16 and MC68HC908AP8
- Two 16-bit, 2-channel timer interface modules (TIM1 and TIM2) with selectable input capture, output compare, and PWM capability on each channel

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

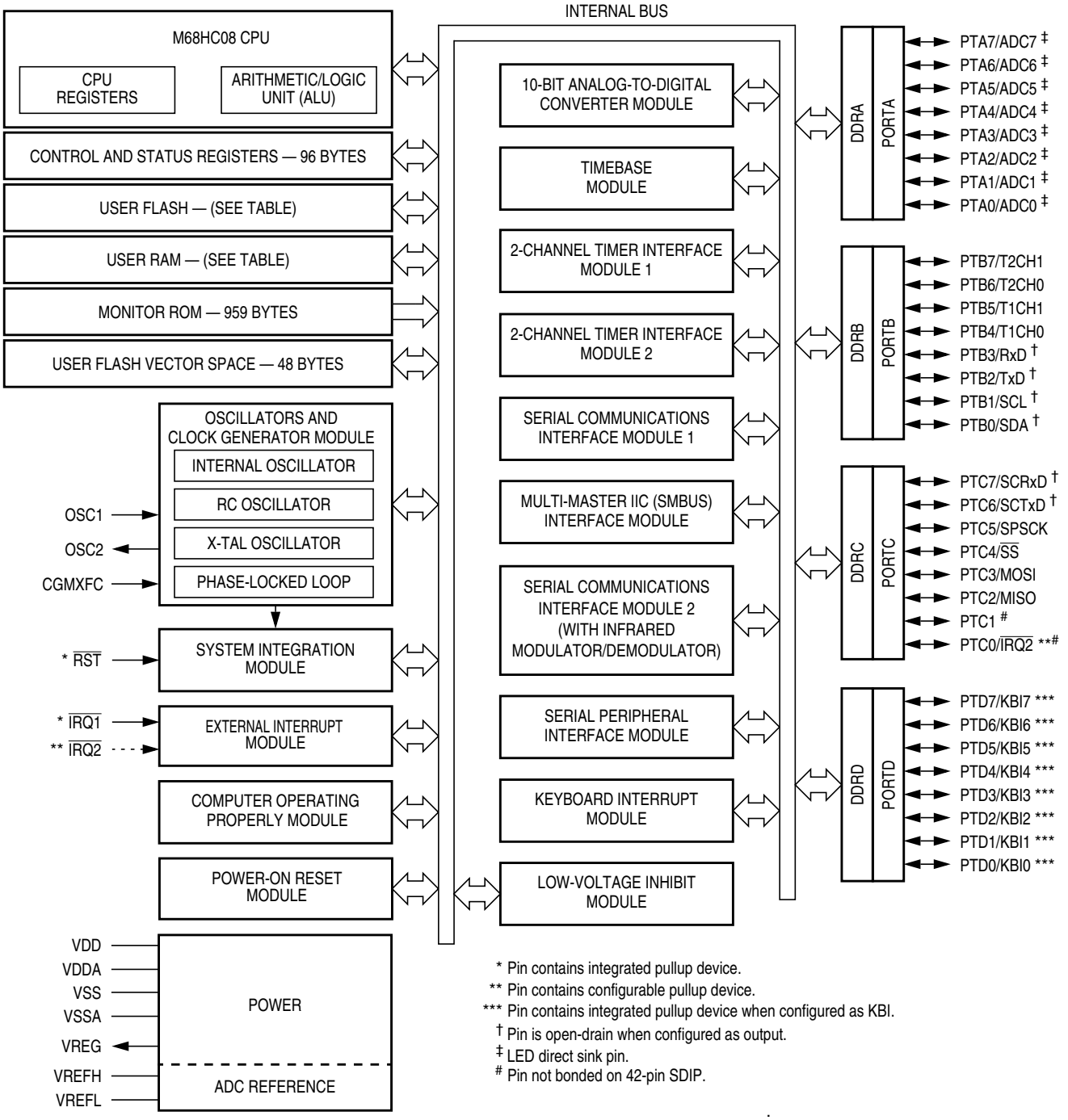
- Timebase module
- Serial communications interface module 1 (SCI)
- Serial communications interface module 2 (SCI) with infrared (IR) encoder/decoder
- Serial peripheral interface module (SPI)
- System management bus (SMBus), version 1.0/1.1 (multi-master IIC bus)
- 8-channel, 10-bit analog-to-digital converter (ADC)
- $\overline{\text{IRQ1}}$ external interrupt pin with integrated pullup
- $\overline{\text{IRQ2}}$ external interrupt pin with programmable pullup
- 8-bit keyboard wakeup port with integrated pullup
- 32 general-purpose input/output (I/O) pins:
  - 31 shared-function I/O pins
  - 8 LED drivers (sink)
  - 6 25mA open-drain I/O with pullup
- Low-power design (fully static with stop and wait modes)
- Master reset pin (with integrated pullup) and power-on reset
- System protection features
  - Optional computer operating properly (COP) reset, driven by internal RC oscillator
  - Low-voltage detection with optional reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- 48-pin low quad flat pack (LQFP), 44-pin quad flat pack (QFP), and 42-pin shrink dual-in-line package (SDIP)
- Specific features of the MC68HC908AP64 in 42-pin SDIP are:
  - 30 general-purpose I/Os only
  - External interrupt on $\overline{\text{IRQ1}}$ only

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit Index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

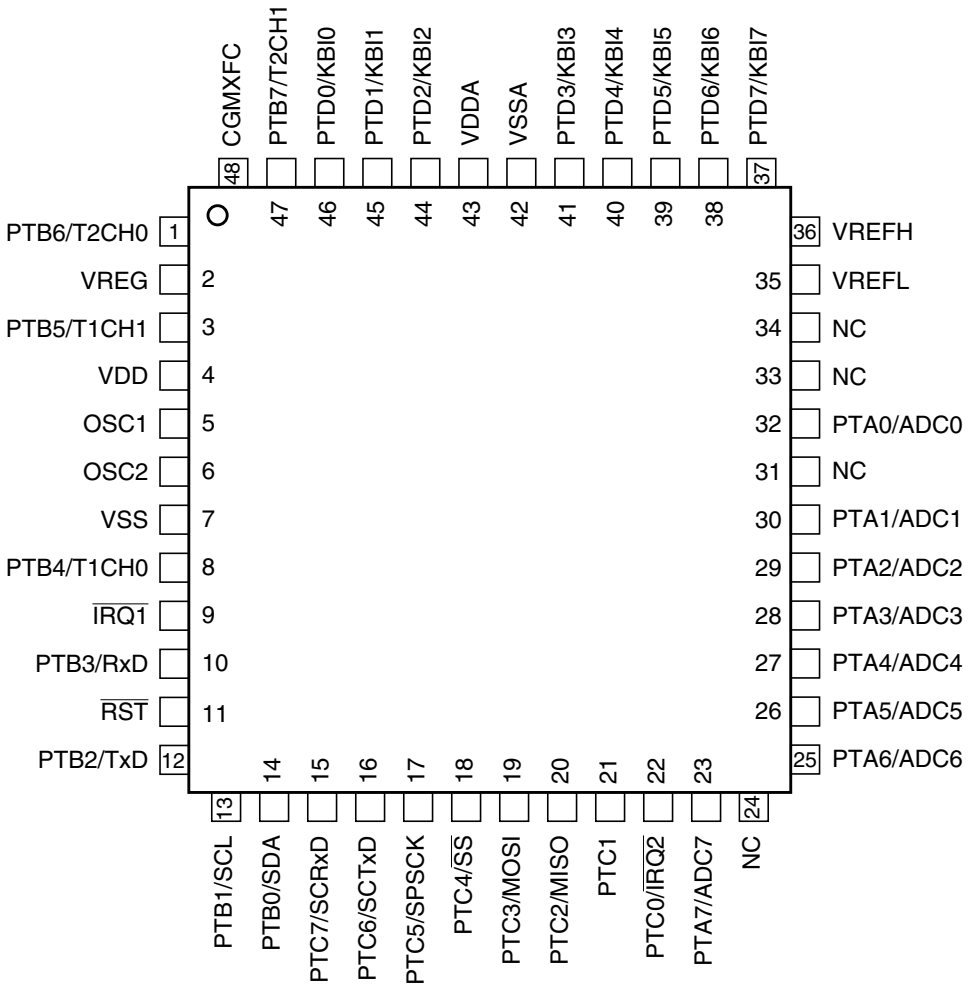
Figure 1-1 shows the structure of the MC68HC908AP64.



DEVICE	USER RAM (bytes)	USER FLASH (bytes)
MC68HC908AP64	2,048	62,368
MC68HC908AP32	2,048	32,768
MC68HC908AP16	1,024	16,384
MC68HC908AP8	1,024	8,192

Figure 1-1. MC68HC908AP64 Block Diagram

1.4 Pin Assignment



NC: No connection

Figure 1-2. 48-Pin LQFP Pin Assignments

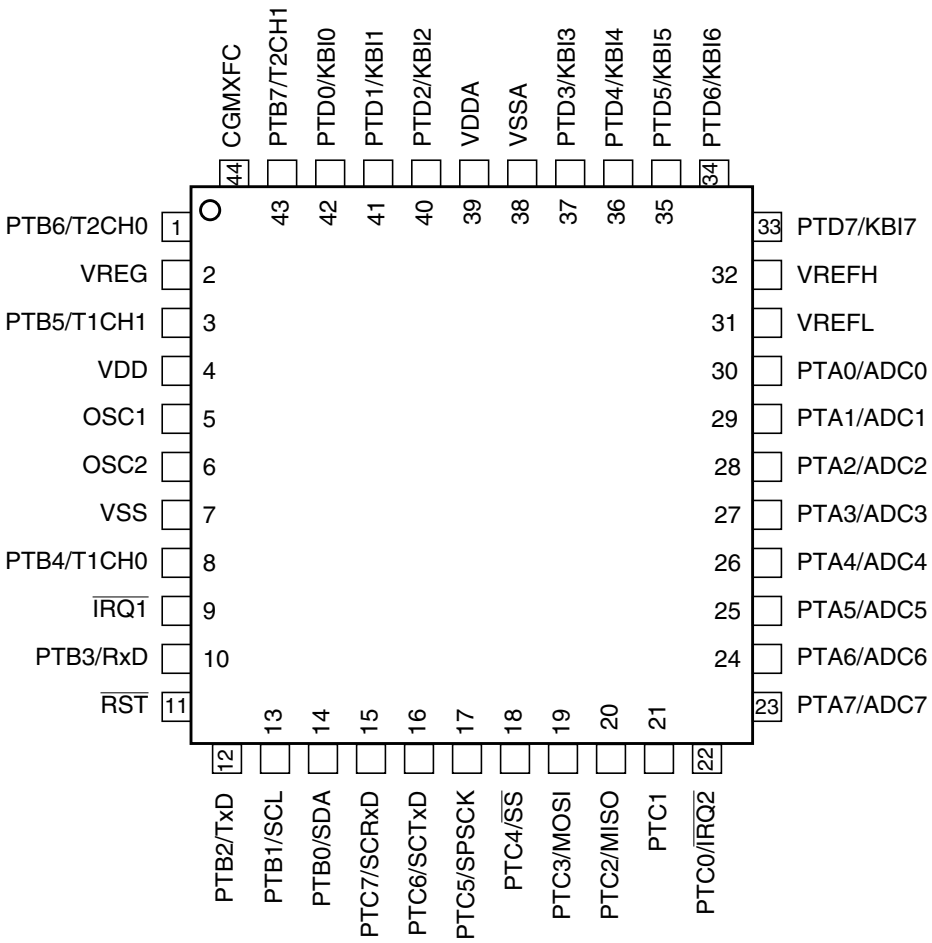
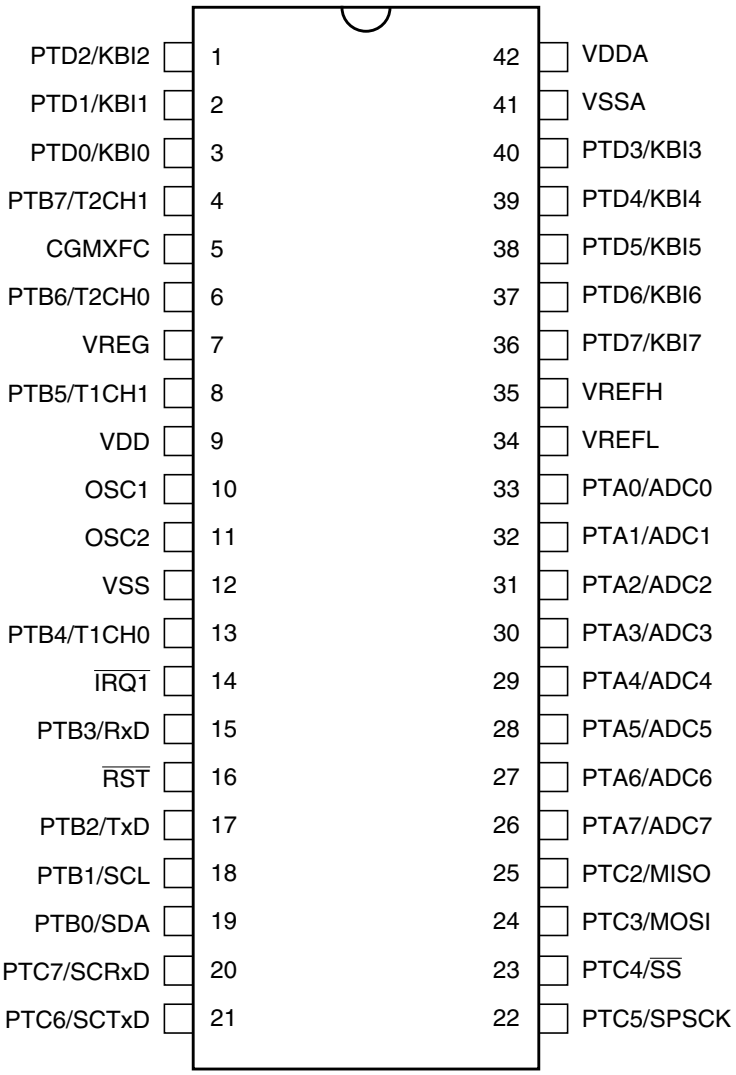


Figure 1-3. 44-Pin QFP Pin Assignments



Pins not available on 42-pin package	Internal connection
PTC0/IRQ2	Unconnected
PTC1	Unconnected

Figure 1-4. 42-Pin SDIP Pin Assignment

1.5 Pin Functions

Description of the pin functions are provided in Table 1-2.

Table 1-2. Pin Functions

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
V_{DD}	Power supply.	In	4.5 to 5.5 or 2.7 to 3.3
V_{SS}	Power supply ground.	Out	0 V
V_{DDA}	Power supply for analog circuits.	In	V_{DD}
V_{SSA}	Power supply ground for analog circuits.	Out	V_{SS}
V_{REFH}	ADC input reference high.	In	V_{DDA}
V_{REFL}	ADC input reference low.	Out	V_{SSA}
V_{REG}	Internal (2.5V) regulator output. Require external capacitors for decoupling.	Out	2.5V(1)
$\overline{RST}$	Reset input, active low; with internal pullup and schmitt trigger input.	In	V_{DD}
$\overline{IRQ1}$	External IRQ1 pin; with internal pullup and schmitt trigger input.	In	V_{DD}
	Used for mode entry selection.	In	V_{DD} to V_{TST}
OSC1	Crystal or RC oscillator input.	In	V_{REG}
OSC2	Crystal OSC option: crystal oscillator output; inverted OSC1.	Out	V_{REG}
	RC OSC option: bus clock output.	Out	V_{REG}
	Internal OSC option: bus clock output.	Out	V_{REG}
CGMXFC	CGM external filter capacitor connection.	In/Out	Analog
PTA0/ADC0 : PTA7/ADC7	8-bit general purpose I/O port.	In/Out	V_{DD}
	Pins as ADC inputs, ADC0–ADC7.	In	V_{REFH}
	Each pin has high current sink for LED.	Out	V_{DD}