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# MC68HC908AS32A

Data Sheet

***M68HC08  
Microcontrollers***

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Rev. 2.0  
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# MC68HC908AS32A

## Data Sheet

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## Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

## Revision History

Date	Revision Level	Description	Page Number(s)
September, 2005	1.0	Reformatted to meet new publications guidelines. Modules updated with additional data	Throughout
		1.4.16 BDLC Receive Pin (BDRxD) — Corrected name of BDLC receive pin to BDRxD.	25
		Removed Keyboard Interface Module	N/A
		Removed Timer Interface Module B Removed all references to TIMB and TBCLK	N/A
May, 2006	2.0	<a href="#">Figure 1-3. 64-Pin QFP Assignments (Top View)</a> — Added pin assignment diagram for the 64-pin QFP.	<a href="#">23</a>
		<a href="#">Figure 2-2. I/O Data, Status and Control Registers</a> — Corrected two register entries: <a href="#">SPI Status and Control Register (SPSCR)</a> <a href="#">FLASH Control Register (FLCR)</a>	<a href="#">32</a> <a href="#">38</a>
		<a href="#">Chapter 20 Ordering Information and Mechanical Specifications</a> — Added information pertaining to the 64-pin quad flag pack (QFP).	<a href="#">271</a>

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## Chapter 20

### Ordering Information and Mechanical Specifications

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# Chapter 1

## General Description

### 1.1 Introduction

The MC68HC908AS32A is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

### 1.2 Features

Features include:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8.4 MHz internal bus frequency
- 32,256 bytes of FLASH electrically erasable read-only memory (FLASH)
- FLASH data security<sup>(1)</sup>
- 512 bytes of on-chip electrically erasable programmable read-only memory with security option (EEPROM)<sup>(1)</sup>
- 1 Kbyte of on-chip RAM
- Clock generator module (CGM)
- Serial peripheral interface module (SPI)
- Serial communications interface module (SCI)
- 8-bit, 15-channel analog-to-digital converter (ADC)
- 16-bit, 6-channel timer interface module (TIM)
- Programmable interrupt timer (PIT)
- System protection features
  - Computer operating properly (COP) with optional reset
  - Low-voltage detection with optional reset
  - Illegal opcode detection with optional reset
  - Illegal address detection with optional reset
- Low-power design (fully static with stop and wait modes)
- Master reset pin and power-on reset
- SAE J1850 byte data link controller digital module

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1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH and EEPROM difficult for unauthorized users.

## General Description

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast  $8 \times 8$  multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- C language support

## 1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908AS32A.

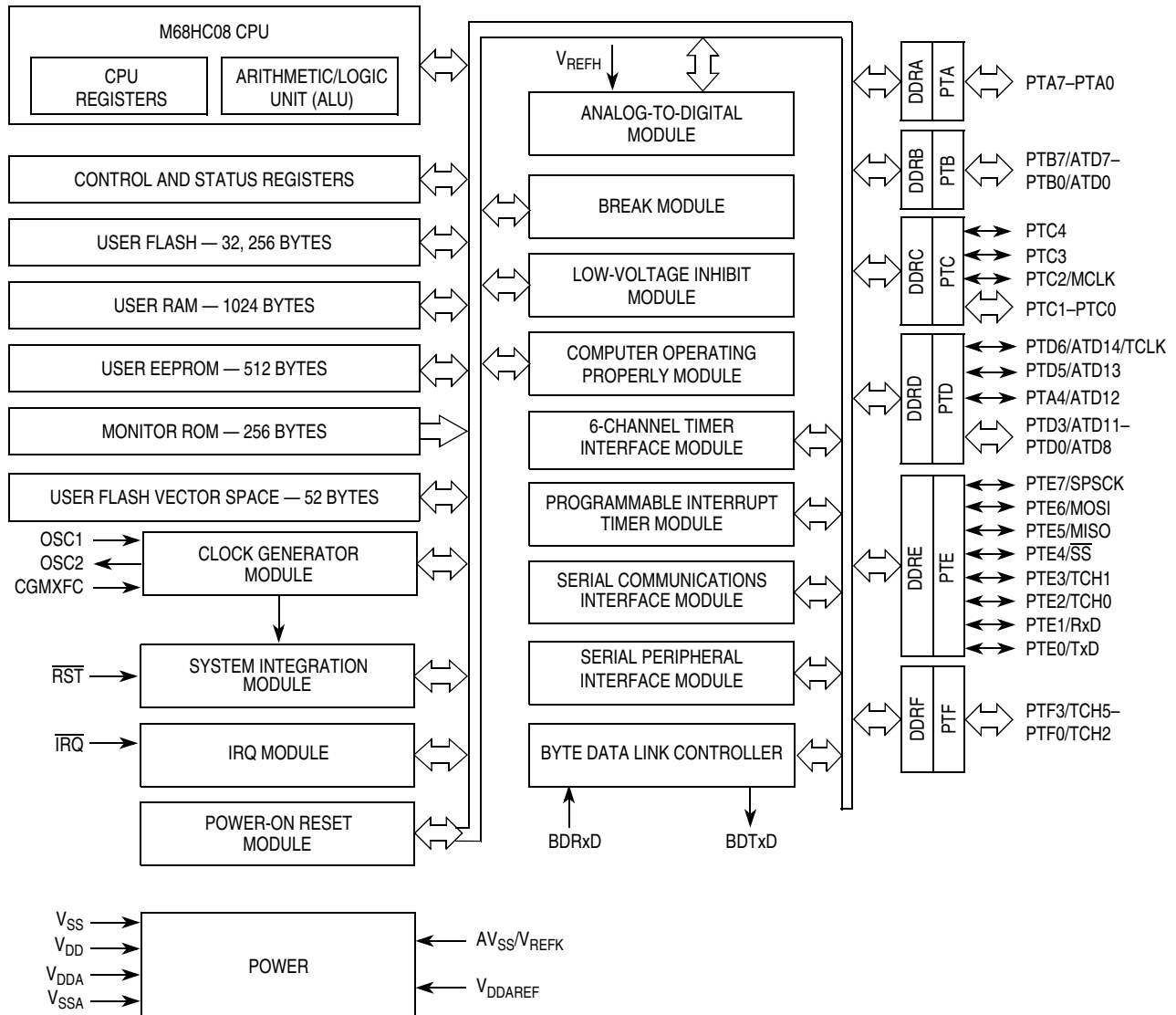


Figure 1-1. MCU Block Diagram for the MC68HC908AS32A



## 1.4 Pin Assignments

The MC68HC908AS32A is available in a 52-pin plastic leaded chip carrier (PLCC) and a 64-pin quad flat pack (QFP). Figure 1-2 and Figure 1-3 show the pin assignments for these packages.

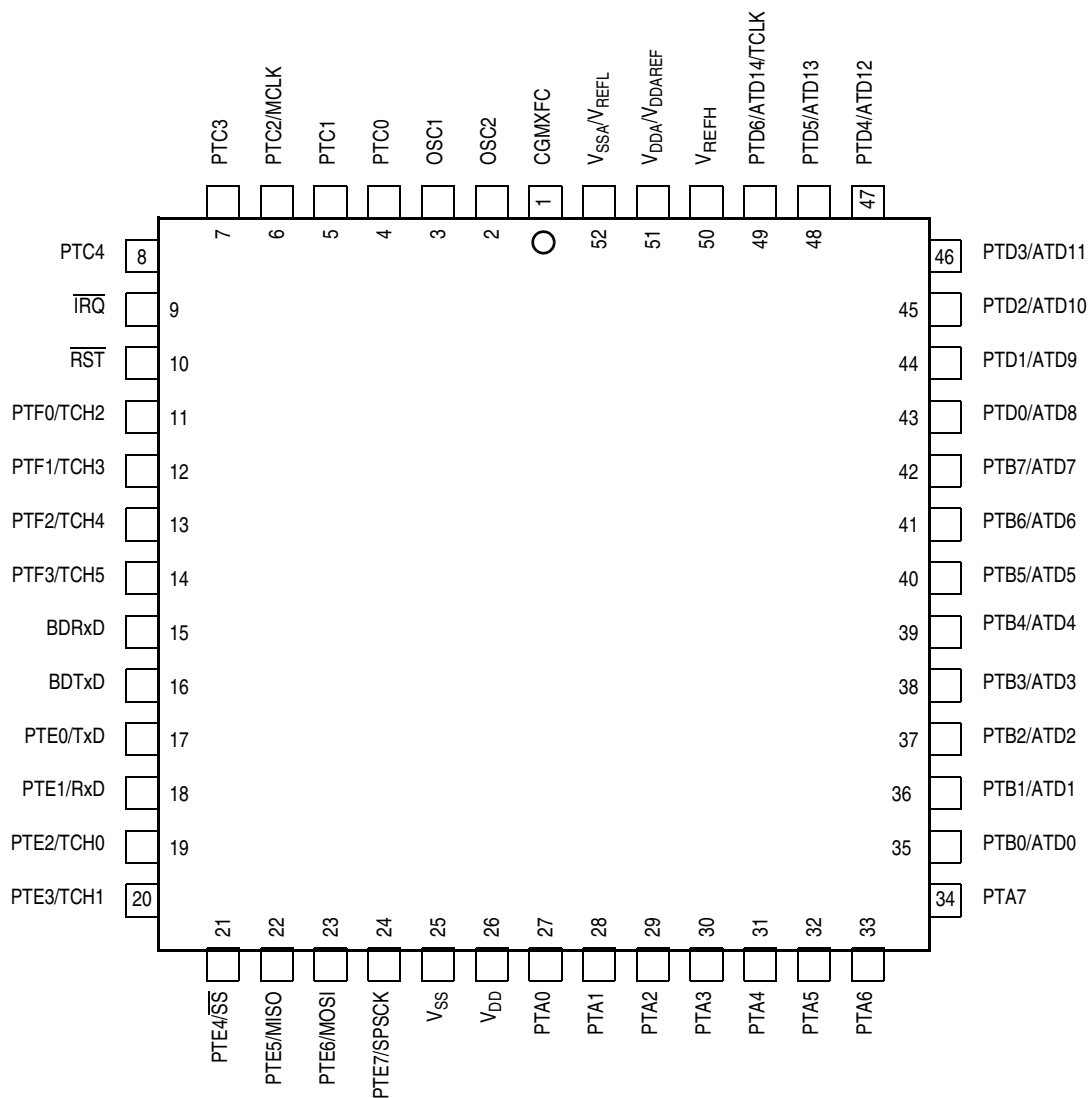
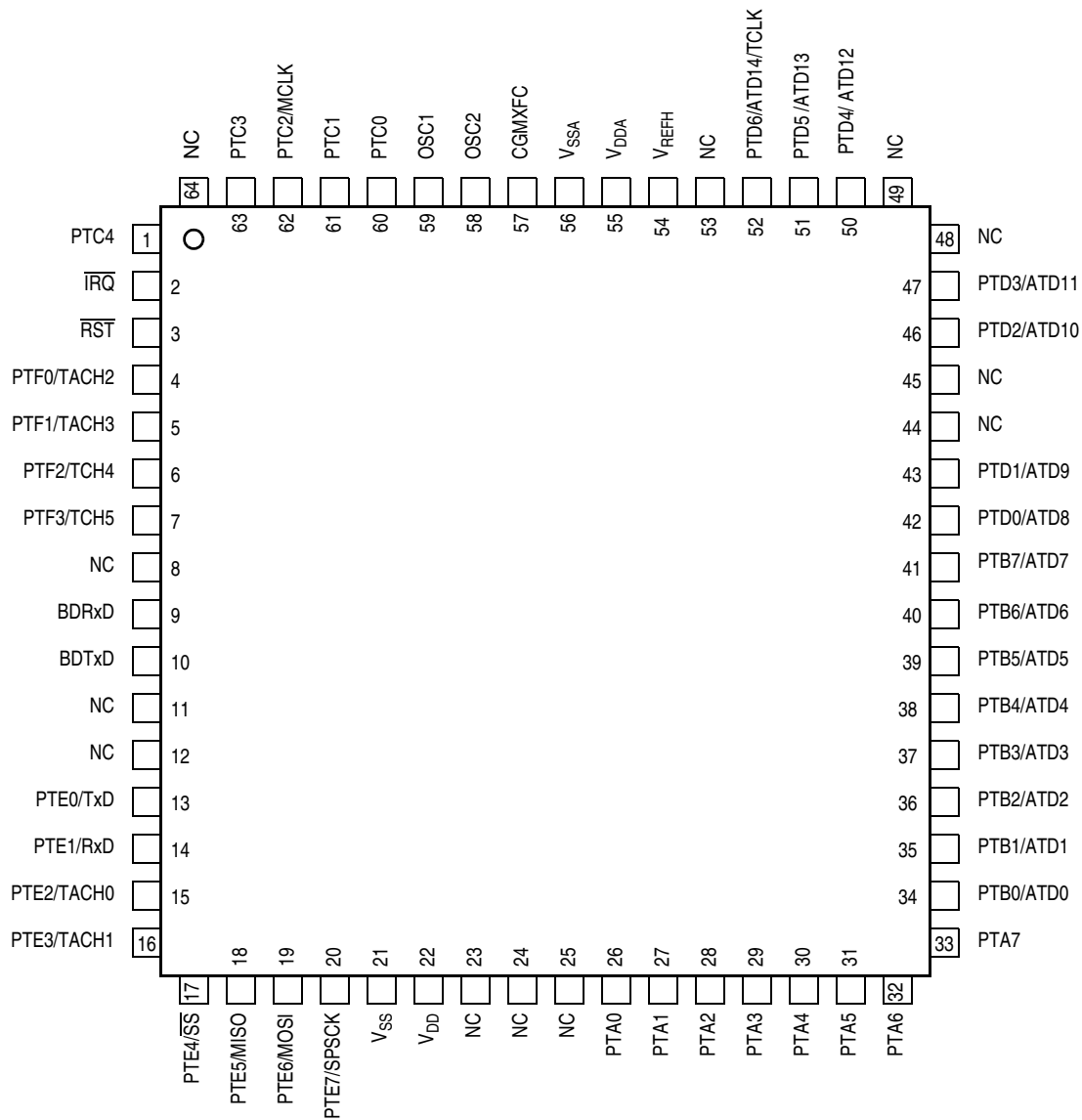


Figure 1-2. 52-Pin PLCC Assignments (Top View)



**Figure 1-3. 64-Pin QFP Assignments (Top View)**

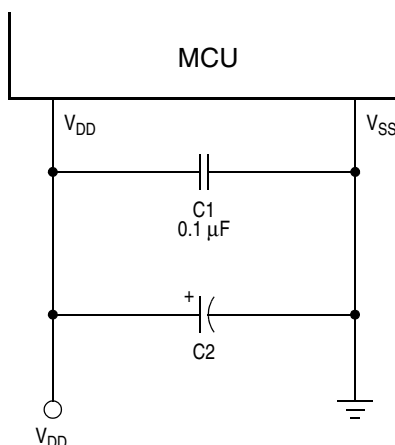
**NOTE**

The following pin descriptions are just a quick reference. For a more detailed representation, see [Chapter 13 Input/Output Ports](#).

**1.4.1 Power Supply Pins ( $V_{DD}$  and  $V_{SS}$ )**

$V_{DD}$  and  $V_{SS}$  are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as shown in [Figure 1-4](#). Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.



NOTE: Component values shown represent typical applications.

**Figure 1-4. Power Supply Bypassing**

$V_{SS}$  is also the ground for the port output buffers and the ground return for the serial clock in the SPI. See [Chapter 16 Serial Peripheral Interface \(SPI\)](#) for more information.

**NOTE**

*$V_{SS}$  must be grounded for proper MCU operation.*

#### 1.4.2 Oscillator Pins (OSC1 and OSC2)

The OSC1 and OSC2 pins are the connections for the on-chip oscillator circuit. See [Chapter 5 Clock Generator Module \(CGM\)](#) for more information.

#### 1.4.3 External Reset Pin ( $\overline{RST}$ )

A 0 on the  $\overline{RST}$  pin forces the MCU to a known startup state.  $\overline{RST}$  is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. See [Chapter 15 System Integration Module \(SIM\)](#) for more information.

#### 1.4.4 External Interrupt Pin ( $\overline{IRQ}$ )

$\overline{IRQ}$  is an asynchronous external interrupt pin. See [Chapter 10 External Interrupt Module \(IRQ\)](#) for more information.

#### 1.4.5 External Filter Capacitor Pin (CGMXFC)

CGMXFC is an external filter capacitor connection for the clock generator module (CGM). See [Chapter 5 Clock Generator Module \(CGM\)](#) for more information.

#### 1.4.6 Analog Power Supply Pin ( $V_{DDA}/V_{DDAREF}$ )

$V_{DDA}/V_{DDAREF}$  is the power supply pin for the analog portion of the ADC and the CGM. See [Chapter 3 Analog-to-Digital Converter \(ADC\)](#) and [Chapter 5 Clock Generator Module \(CGM\)](#) for more information.

### 1.4.7 Analog Ground Pin ( $V_{SSA}/V_{REFL}$ )

The  $V_{SSA}/V_{REFL}$  pin provides both the analog ground connection and the reference low voltage for the ADC as well as the ground connection for the CGM. See [Chapter 3 Analog-to-Digital Converter \(ADC\)](#) and [Chapter 5 Clock Generator Module \(CGM\)](#) for more information.

### 1.4.8 ADC Reference High Voltage Pin ( $V_{REFH}$ )

$V_{REFH}$  provides the reference high voltage for the ADC. See [Chapter 3 Analog-to-Digital Converter \(ADC\)](#) for more information.

### 1.4.9 Port A Input/Output (I/O) Pins (PTA7–PTA0)

PTA7–PTA0 are general-purpose bidirectional input/output (I/O) port pins. See [Chapter 13 Input/Output Ports](#) for more information.

### 1.4.10 Port B I/O Pins (PTB7/ATD7–PTB0/ATD0)

Port B is an 8-bit special function port that shares all eight pins with the ADC. See [Chapter 3 Analog-to-Digital Converter \(ADC\)](#) and [Chapter 13 Input/Output Ports](#) for more information.

### 1.4.11 Port C I/O Pins (PTC4–PTC0)

PTC4–PTC3 and PTC1–PTC0 are general-purpose bidirectional I/O port pins. PTC2/MCLK is a special function port that shares its pin with the system clock which has a frequency equivalent to the system clock. See [Chapter 13 Input/Output Ports](#) for more information.

### 1.4.12 Port D I/O Pins (PTD6–PTD0/ATD8)

Port D is an 7-bit special-function port that shares seven of its pins with the ADC and one of its pins with the TIM. See [Chapter 17 Timer Interface Module \(TIM\)](#), [Chapter 3 Analog-to-Digital Converter \(ADC\)](#), and [Chapter 13 Input/Output Ports](#) for more information.

### 1.4.13 Port E I/O Pins (PTE7/SPSCK–PTE0/TxD)

Port E is an 8-bit special function port that shares two of its pins with the TIM, four of its pins with the SPI, and two of its pins with the SCI. See [Chapter 14 Serial Communications Interface \(SCI\)](#), [Chapter 16 Serial Peripheral Interface \(SPI\)](#), [Chapter 17 Timer Interface Module \(TIM\)](#), and [Chapter 13 Input/Output Ports](#) for more information.

### 1.4.14 Port F I/O Pins (PTF3–PTF0/TCH2)

Port F is a 4-bit special function port that shares four of its pins with the TIM. See [Chapter 17 Timer Interface Module \(TIM\)](#) and [Chapter 13 Input/Output Ports](#) for more information.

### 1.4.15 BDLC Transmit Pin (BDTxD)

This pin is the digital output from the BDLC module (BDTxD). See [Chapter 19 Electrical Specifications](#) for more information.