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Addendum to MC68HC908EY16A, rev. 2

This addendum introduces a change to this data sheet.

Chapter 19 Development Support, Section 19.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE

Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors.

Changes to:

Chapter 19 Development Support, Section 19.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE

Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors. An improved security function denies monitor mode entry if five or more of the eight security bytes are $00 (zero bytes).

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MC68HC908EY16A
MC68HC908EY8A

Data Sheet

M68HC08
Microcontrollers

MC68HC908EY16A
Rev. 2
09/2010

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MC68HC908EY16A
MC68HC908EY8A

Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com/

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
April, 2006	0	Initial release	N/A
September, 2006	1	21.2 Ordering Information — Separated automotive and consumer/industrial part numbers.	279
		A.4 Ordering Information — Separated automotive and consumer/industrial part numbers.	286

Revision History (Continued)

Date	Revision Level	Description	Page Number(s)
September 2010	2	20.3 Functional Operating Range — Changed maximum temperature specification from 135 °C to 125 °C.	262
		20.5 5V DC Electrical Characteristics — Changed maximum temperature specification from 135 °C to 125 °C.	262
		20.7 3V DC Electrical Characteristics — Changed maximum temperature specification from 135 °C to 125 °C.	265
		20.9 Internal Oscillator Characteristics — Changed maximum temperature specification from 135 °C to 125 °C.	266
		20.10 External Oscillator Characteristics — Changed maximum temperature specification from 135 °C to 125 °C.	267
		20.11 Trimmed Accuracy of the Internal Clock Generator — Changed maximum temperature specification from 135 °C to 125 °C.	268
		20.16 Memory Characteristics — Removed note referring to flash memory behavior between 125 °C to 135 °C.	275
		21.2 Ordering Information — Removed S908EY16AKFJE and MC908EY16AKFJE part numbers.	279
		A.4 Ordering Information — Removed S908EY16AKFJE and MC908EY16AKFJE part numbers.	286

List of Chapters

Table of Contents

Chapter 1
General Description

Chapter 2
Memory

Chapter 3

Analog-to-Digital Converter (ADC10) Module

Chapter 4
BEMF Counter Module (BEMF)

Chapter 5
Configuration Registers (CONFIG1, CONFIG2, CONFIG3)

Chapter 6
Computer Operating Properly

Chapter 7
Central Processor Unit (CPU)

Chapter 8
Internal Clock Generator (ICG) Module

Chapter 9
External Interrupt (IRQ)

Chapter 10
Keyboard Interrupt (KBI) Module

Chapter 11
Low-Voltage Inhibit (LVI) Module

Chapter 12
Input/Output (I/O) Ports (PORTS)

Chapter 13
Enhanced Serial Communications Interface (ESCI) Module

Chapter 14
System Integration Module (SIM)

Chapter 15
Serial Peripheral Interface (SPI) Module

Chapter 16
Timebase Module (TBM)

Chapter 17
Timer Interface A (TIMA) Module

Chapter 18
Timer Interface B (TIMB) Module

Chapter 19
Development Support

Chapter 20
Electrical Specifications

Chapter 21
Ordering Information and Mechanical Specifications

Appendix A
MC68HC908EY8A

Appendix B
Differences Between 908EY16A and 908EY16

Chapter 1
General Description

1.1 Introduction

The MC68HC908EY16A is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

The information contained in this document pertains to the MC68HC908EY8A with the exceptions noted in Appendix A MC68HC908EY8A.

1.2 Features

For convenience, features have been organized to reflect:

- Standard features of the MC68HC908EY16A
- Features of the CPU08

Standard features of the MC68HC908EY16A include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency at 5V
- Internal oscillator requiring no external components:
  - Software selectable bus frequencies
  - 25 percent accuracy with a trimming capability of better than 1 percent
  - Clock monitor
  - Option to allow use of external clock source or external crystal/ceramic resonator
- 15,872 bytes of on-chip FLASH memory with in-circuit programming
- FLASH program memory security[1]
- 512 bytes of on-chip random-access memory (RAM)
- Low voltage inhibit (LVI) module
- Internal clock generator module (ICG)
- Two 16-bit, 2-channel timer (TIMA and TIMB) interface modules with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- 8-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- Enhanced serial communications interface module (ESCI) for local interconnect network (LIN) connectivity
- Serial peripheral interface (SPI)

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

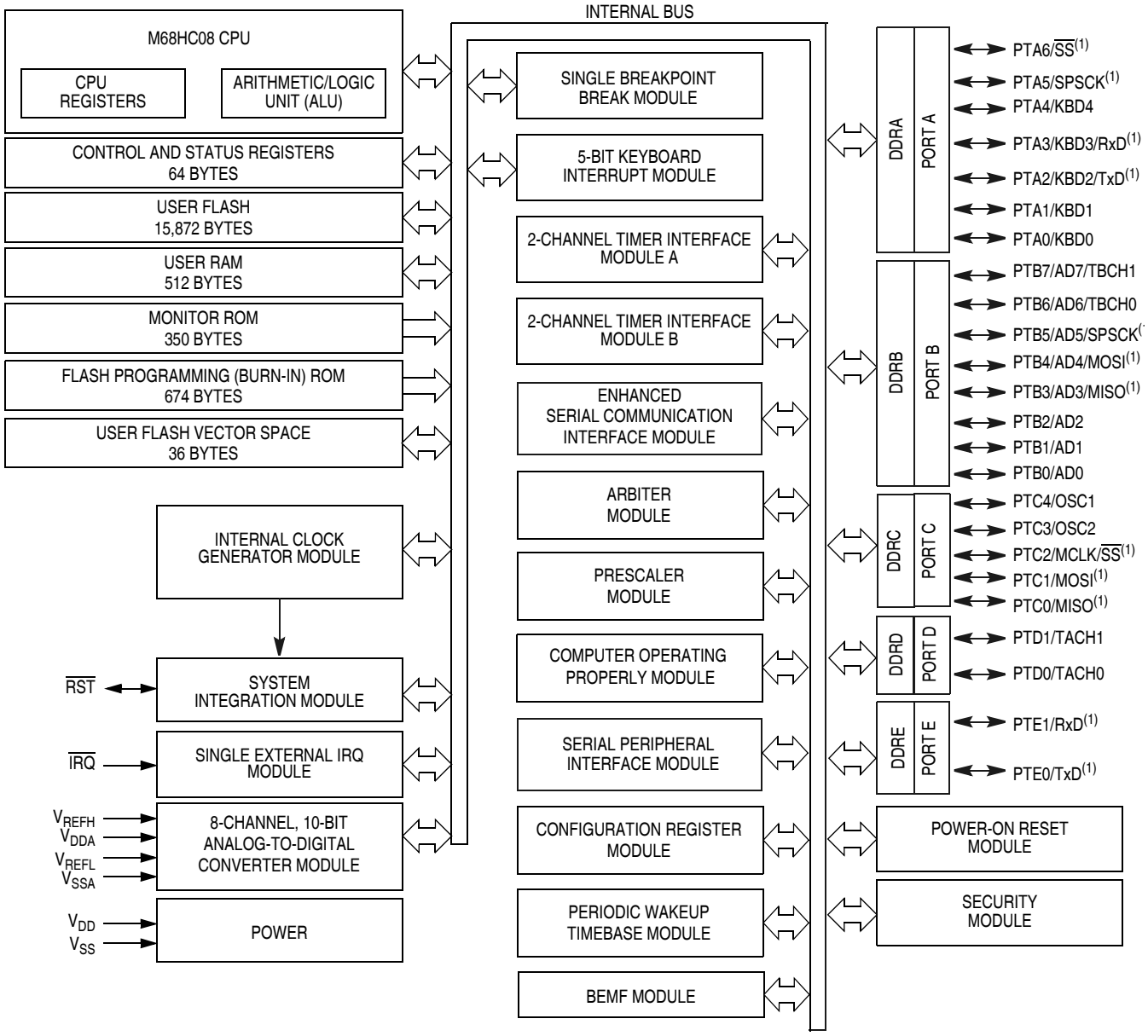
- Timebase Module (TBM)
- 5-bit keyboard wakeup port with software selectable rising or falling edge detect, as well as high- or low-level detection
  – Programmable for rising/falling edge or high/low level detection
- 24 general-purpose input/output (I/O) pins
- External asynchronous interrupt pin with internal pullup ($\overline{\text{IRQ}}$)
- System protection features:
  – Optional computer operating properly (COP) reset
  – Illegal opcode detection with reset
  – Illegal address detection with reset
- 32-pin quad flat pack (QFP) package
- Low-power design; fully static with stop and wait modes
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce customer system cost
- Standard low-power modes of operation:
  – Wait mode
  – Stop mode
- Master reset pin ($\overline{\text{RST}}$) and power-on reset (POR)
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Higher current source capability on nine port lines for LED drive (PTA6/$\overline{\text{SS}}$, PTA5/SPSCK, PTA4/KBD4, PTA3/KBD3/RxD, PTA2/KBD2/TxD, PTA1/KBD1, PTA0/KBD0, PTC1/MOSI, and PTC0/MISO)

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16 ÷ 8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Third party C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908EY16A.



NOTE:
1. The locations of the ESCI and SPI pins are user selectable using CONFIG3 option bits.

Figure 1-1. MCU Block Diagram

1.4 Pin Assignments

Figure 1-2 shows the pin assignments for the MC68HC908EY16A.

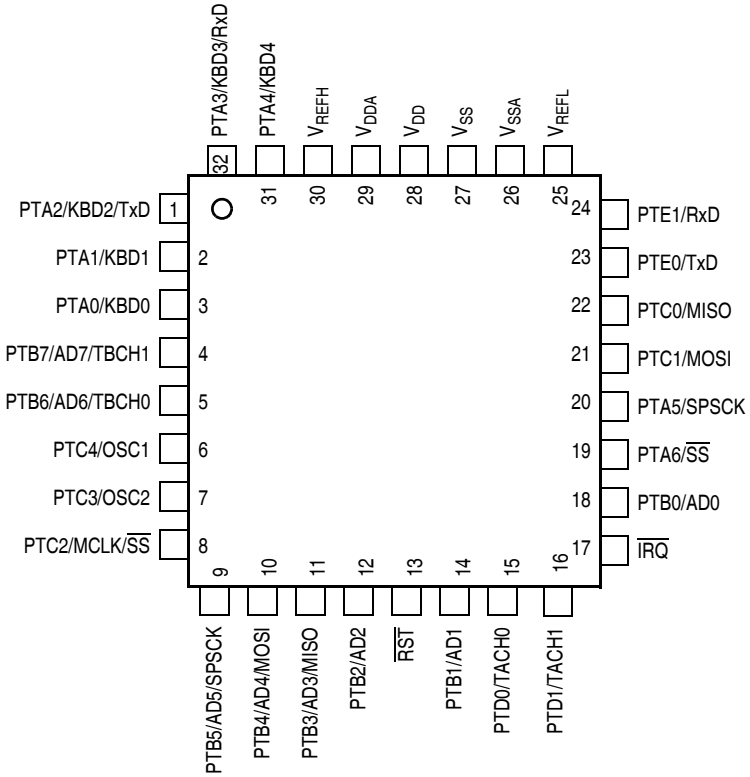


Figure 1-2. Pin Assignments

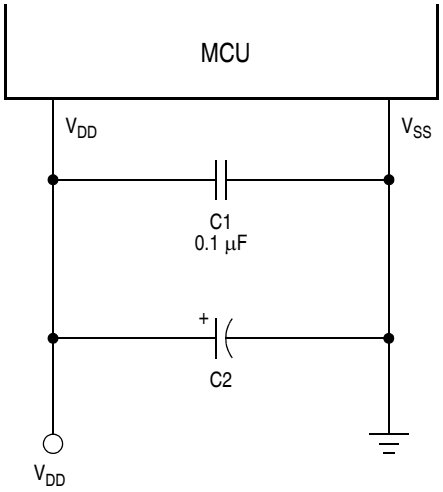
1.5 Pin Functions

Descriptions of the pin functions are provided here.

1.5.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as Figure 1-3 shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.



Note: Component values shown represent typical applications.

Figure 1-3. Power Supply Bypassing

1.5.2 Oscillator Pins (PTC4/OSC1 and PTC3/OSC2)

The OSC1 and OSC2 pins are available through programming options in the configuration register. These pins then become the connections to an external clock source or crystal/ceramic resonator.

When selecting PTC4 and PTC3 as I/O, OSC1 and OSC2 functions are not available.

1.5.3 External Reset Pin ($\overline{RST}$)

A logic 0 on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor that is always activated, even when the reset pin is pulled low. See Chapter 14 System Integration Module (SIM).

1.5.4 External Interrupt Pin ($\overline{IRQ}$)

$\overline{IRQ}$ is an asynchronous external interrupt pin. This pin contains an internal pullup resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled low. See Chapter 9 External Interrupt (IRQ).

1.5.5 Analog Power Supply/Reference Pins (V_{DDA}, V_{REFH}, V_{SSA}, and V_{REFL})

V_{DDA} and V_{SSA} are the power supply pins for the analog-to-digital converter (ADC). Decoupling of these pins should be as per the digital supply.

NOTE

V_{REFH} is the high reference supply for the ADC. V_{DDA} should be tied to the same potential as V_{DD} via separate traces.

V_{REFL} is the low reference supply for the ADC. V_{SSA} should be tied to the same potential as V_{SS} via separate traces.

See Chapter 3 Analog-to-Digital Converter (ADC10) Module.