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Addendum to MC68HC908EY16A, rev. 2

This addendum introduces a change to this data sheet.

Chapter 19 Development Support, Section 19.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations \$FFF6–\$FFFD. Locations \$FFF6–\$FFFD contain user-defined data.

NOTE

Do not leave locations \$FFF6–\$FFFD blank. For security reasons, program locations \$FFF6–\$FFFD even if they are not used for vectors.

Changes to:

Chapter 19 Development Support, Section 19.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations \$FFF6–\$FFFD. Locations \$FFF6–\$FFFD contain user-defined data.

NOTE

Do not leave locations \$FFF6–\$FFFD blank. For security reasons, program locations \$FFF6–\$FFFD even if they are not used for vectors. An improved security function denies monitor mode entry if five or more of the eight security bytes are \$00 (zero bytes).

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MC68HC908EY16A MC68HC908EY8A

Data Sheet

***M68HC08
Microcontrollers***

MC68HC908EY16A
Rev. 2
09/2010

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MC68HC908EY16A

MC68HC908EY8A

Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

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September, 2006	1	21.2 Ordering Information — Separated automotive and consumer/industrial part numbers.	279
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		20.5 5V DC Electrical Characteristics — Changed maximum temperature specification from 135 °C to 125 °C.	262
		20.7 3V DC Electrical Characteristics — Changed maximum temperature specification from 135 °C to 125 °C.	265
		20.9 Internal Oscillator Characteristics — Changed maximum temperature specification from 135 °C to 125 °C.	266
		20.10 External Oscillator Characteristics — Changed maximum temperature specification from 135 °C to 125 °C.	267
		20.11 Trimmed Accuracy of the Internal Clock Generator — Changed maximum temperature specification from 135 °C to 125 °C.	268
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List of Chapters

Chapter 1	General Description	19
Chapter 2	Memory	29
Chapter 3	Analog-to-Digital Converter (ADC10) Module	47
Chapter 4	BEMF Counter Module (BEMF)	61
Chapter 5	Configuration Registers (CONFIG1, CONFIG2, CONFIG3)	63
Chapter 6	Computer Operating Properly	69
Chapter 7	Central Processor Unit (CPU)	73
Chapter 8	Internal Clock Generator (ICG) Module	85
Chapter 9	External Interrupt (IRQ)	109
Chapter 10	Keyboard Interrupt (KBI) Module	113
Chapter 11	Low-Voltage Inhibit (LVI) Module	119
Chapter 12	Input/Output (I/O) Ports (PORTS)	123
Chapter 13	Enhanced Serial Communications Interface (ESCI) Module	133
Chapter 14	System Integration Module (SIM)	163
Chapter 15	Serial Peripheral Interface (SPI) Module	179
Chapter 16		

	Timebase Module (TBM)	199
Chapter 17	Timer Interface A (TIMA) Module	203
Chapter 18	Timer Interface B (TIMB) Module	219
Chapter 19	Development Support	235
Chapter 20	Electrical Specifications	261
Chapter 21	Ordering Information and Mechanical Specifications	279
Appendix A	MC68HC908EY8A	283
Appendix B	Differences Between 908EY16A and 908EY16	287

Table of Contents

Chapter 1 General Description

1.1	Introduction	19
1.2	Features	19
1.3	MCU Block Diagram	20
1.4	Pin Assignments	22
1.5	Pin Functions	22
1.5.1	Power Supply Pins (V_{DD} and V_{SS})	22
1.5.2	Oscillator Pins (PTC4/OSC1 and PTC3/OSC2)	23
1.5.3	External Reset Pin (\overline{RST})	23
1.5.4	External Interrupt Pin (\overline{IRQ})	23
1.5.5	Analog Power Supply/Reference Pins (V_{DDA} , V_{REFH} , V_{SSA} , and V_{REFL})	23
1.5.6	Port A I/O Pins (PTA6/ \overline{SS} , PTA5/SPSCK, PTA4/KBD4, PTA3/KBD3/RxD, PTA2/KBD2/TxD, PTA1/KBD1, and PTA0/KBD0)	24
1.5.7	Port B I/O Pins (PTB7/AD7/TBCH1, PTB6/AD6/TBCH0, PTB5/AD5/SPSCK, PTB4/AD4/MO-SI, PTB3/AD3/MISO, PTB2/AD2–PTB0/AD0)	24
1.5.8	Port C I/O Pins (PTC4/OSC1, PTC3/OSC2, PTC2/MCLK/ \overline{SS} , PTC1/MOSI, PTC0/MISO)	24
1.5.9	Port D I/O Pins (PTD1/TACH1–PTD0/TACH0)	24
1.5.10	Port E I/O Pins (PTE1/RxD–PTE0/TxD)	24
1.6	Pin Summary	25
1.7	Priority of Shared Pins	27

Chapter 2 Memory

2.1	Introduction	29
2.2	Unimplemented Memory Locations	29
2.3	Reserved Memory Locations	29
2.4	Input/Output (I/O) Section	29
2.5	Random Access Memory (RAM)	39
2.6	FLASH Memory (FLASH)	39
2.6.1	FLASH Control Register	40
2.6.2	FLASH Page Erase Operation	41
2.6.3	FLASH Mass Erase Operation	42
2.6.4	FLASH Program/Read Operation	43
2.6.5	FLASH Block Protection	45
2.6.6	FLASH Block Protect Register	45
2.6.7	Wait Mode	46
2.6.8	Stop Mode	46

Chapter 3

Analog-to-Digital Converter (ADC10) Module

3.1	Introduction	47
3.2	Features	47
3.3	Functional Description	47
3.3.1	Clock Select and Divide Circuit	49
3.3.2	Input Select and Pin Control	50
3.3.3	Conversion Control	50
3.3.3.1	Initiating Conversions	50
3.3.3.2	Completing Conversions	50
3.3.3.3	Aborting Conversions	50
3.3.3.4	Total Conversion Time	51
3.3.4	Sources of Error	52
3.3.4.1	Sampling Error	52
3.3.4.2	Pin Leakage Error	52
3.3.4.3	Noise-Induced Errors	52
3.3.4.4	Code Width and Quantization Error	53
3.3.4.5	Linearity Errors	53
3.3.4.6	Code Jitter, Non-Monotonicity and Missing Codes	53
3.4	Interrupts	54
3.5	Low-Power Modes	54
3.5.1	Wait Mode	54
3.5.2	Stop Mode	54
3.6	ADC10 During Break Interrupts	54
3.7	I/O Signals	55
3.7.1	ADC10 Analog Power Pin (VDDA)	55
3.7.2	ADC10 Analog Ground Pin (VSSA)	55
3.7.3	ADC10 Voltage Reference High Pin (VREFH)	55
3.7.4	ADC10 Voltage Reference Low Pin (VREFL)	55
3.7.5	ADC10 Channel Pins (ADn)	56
3.8	Registers	56
3.8.1	ADC10 Status and Control Register	56
3.8.2	ADC10 Result High Register (ADRH)	58
3.8.3	ADC10 Result Low Register (ADRL)	58
3.8.4	ADC10 Clock Register (ADCLK)	59

Chapter 4

BEMF Counter Module (BEMF)

4.1	Introduction	61
4.2	Functional Description	61
4.3	BEMF Register	61
4.4	Input Signal	61
4.5	Low Power Modes	61
4.5.1	Wait Mode	61
4.5.2	Stop Mode	62

Chapter 5

Configuration Registers (CONFIG1, CONFIG2, CONFIG3)

5.1	Introduction	63
5.2	Functional Description	63

Chapter 6 Computer Operating Properly

6.1	Introduction	69
6.2	Functional Description	69
6.3	I/O Signals	70
6.3.1	CGMXCLK	70
6.3.2	STOP Instruction	70
6.3.3	COPCTL Write	70
6.3.4	Power-On Reset	70
6.3.5	Internal Reset	70
6.3.6	Reset Vector Fetch	70
6.3.7	COPD	70
6.3.8	COPRS	71
6.4	COP Control Register	71
6.5	Interrupts	71
6.6	Monitor Mode	71
6.7	Low-Power Modes	71
6.7.1	Wait Mode	71
6.7.2	Stop Mode	71
6.8	COP Module During Break Interrupts	71

Chapter 7 Central Processor Unit (CPU)

7.1	Introduction	73
7.2	Features	73
7.3	CPU Registers	73
7.3.1	Accumulator	74
7.3.2	Index Register	74
7.3.3	Stack Pointer	75
7.3.4	Program Counter	75
7.3.5	Condition Code Register	76
7.4	Arithmetic/Logic Unit (ALU)	77
7.5	Low-Power Modes	77
7.5.1	Wait Mode	77
7.5.2	Stop Mode	77
7.6	CPU During Break Interrupts	77
7.7	Instruction Set Summary	78
7.8	Opcode Map	83

Chapter 8 Internal Clock Generator (ICG) Module

8.1	Introduction	85
8.2	Features	85

8.3	Functional Description	85
8.3.1	Clock Enable Circuit	88
8.3.2	Internal Clock Generator	88
8.3.2.1	Digitally Controlled Oscillator	89
8.3.2.2	Modulo N Divider	89
8.3.2.3	Frequency Comparator	90
8.3.2.4	Digital Loop Filter	90
8.3.3	External Clock Generator	90
8.3.3.1	External Oscillator Amplifier	91
8.3.3.2	External Clock Input Path	92
8.3.4	Clock Monitor Circuit	92
8.3.4.1	Clock Monitor Reference Generator	93
8.3.4.2	Internal Clock Activity Detector	93
8.3.4.3	External Clock Activity Detector	93
8.3.5	Clock Selection Circuit	95
8.3.5.1	Clock Selection Switches	95
8.3.5.2	Clock Switching Circuit	95
8.4	Usage Notes	96
8.4.1	Switching Clock Sources	96
8.4.2	Enabling the Clock Monitor	96
8.4.3	Using Clock Monitor Interrupts	97
8.4.4	Quantization Error in DCO Output	97
8.4.4.1	Digitally Controlled Oscillator	98
8.4.4.2	Binary Weighted Divider	98
8.4.4.3	Variable-Delay Ring Oscillator	98
8.4.4.4	Ring Oscillator Fine-Adjust Circuit	99
8.4.5	Switching Internal Clock Frequencies	99
8.4.6	Nominal Frequency Settling Time	99
8.4.6.1	Settling to Within 15 Percent	100
8.4.6.2	Settling to Within 5 Percent	100
8.4.6.3	Total Settling Time	100
8.4.7	Trimming Frequency on the Internal Clock Generator	101
8.5	Low-Power Modes	101
8.5.1	Wait Mode	101
8.5.2	Stop Mode	102
8.6	CONFIG Options	102
8.6.1	External Clock Enable (EXTCLKEN)	102
8.6.2	External Crystal Enable (EXTXTALEN)	102
8.6.3	Slow External Clock (EXTSLOW)	103
8.6.4	Oscillator Enable In Stop (OSCENINSTOP)	103
8.7	Input/Output (I/O) Registers	103
8.7.1	ICG Control Register	104
8.7.2	ICG Multiplier Register	106
8.7.3	ICG Trim Register	106
8.7.4	ICG 5-Volt Trim Value	107
8.7.5	ICG 3-Volt Trim Value	107
8.7.6	ICG DCO Divider Register	107
8.7.7	ICG DCO Stage Register	108

Chapter 9 External Interrupt (IRQ)

9.1	Introduction	109
9.2	Features	109
9.3	Functional Description	109
9.4	$\overline{\text{IRQ}}$ Pin	110
9.5	IRQ Module During Break Interrupts	112
9.6	IRQ Status and Control Register	112

Chapter 10 Keyboard Interrupt (KBI) Module

10.1	Introduction	113
10.2	Features	113
10.3	Functional Description	113
10.3.1	Keyboard Operation	113
10.3.1.1	MODEK = 1	115
10.3.1.2	MODEK = 0	115
10.3.2	Keyboard Initialization	116
10.4	Interrupts	116
10.5	Low-Power Modes	116
10.5.1	Wait Mode	116
10.5.2	Stop Mode	116
10.6	KBI During Break Interrupts	116
10.7	I/O Signals	117
10.7.1	KBI Input Pins (KBI7:KBI0)	117
10.8	Registers	117
10.8.1	Keyboard Status and Control Register (KBSCR)	117
10.8.2	Keyboard Interrupt Enable Register (KBIER)	118
10.8.3	Keyboard Interrupt Polarity Register (KBIPR)	118

Chapter 11 Low-Voltage Inhibit (LVI) Module

11.1	Introduction	119
11.2	Features	119
11.3	Functional Description	119
11.3.1	Polled LVI Operation	120
11.3.2	Forced Reset Operation	120
11.3.3	False Reset Protection	120
11.3.4	LVI Status Register	120
11.4	LVI Interrupts	121
11.5	Low-Power Modes	121
11.5.1	Wait Mode	121
11.5.2	Stop Mode	121

Chapter 12 Input/Output (I/O) Ports (PORTS)

12.1	Introduction	123
12.2	Port A	123
12.2.1	Port A Data Register	123
12.2.2	Data Direction Register A	123
12.3	Port B	125
12.3.1	Port B Data Register	125
12.3.2	Data Direction Register B	125
12.4	Port C	126
12.4.1	Port C Data Register	126
12.4.2	Data Direction Register C	127
12.5	Port D	128
12.5.1	Port D Data Register	128
12.5.2	Data Direction Register D	128
12.6	Port E	130
12.6.1	Port E Data Register	130
12.6.2	Data Direction Register E	130

Chapter 13

Enhanced Serial Communications Interface (ESCI) Module

13.1	Introduction	133
13.2	Features	133
13.3	Pin Name Conventions	133
13.4	Functional Description	135
13.4.1	Data Format	136
13.4.2	Transmitter	136
13.4.2.1	Character Length	137
13.4.2.2	Character Transmission	137
13.4.2.3	Break Characters	137
13.4.2.4	Idle Characters	138
13.4.2.5	Inversion of Transmitted Output	138
13.4.2.6	Transmitter Interrupts	138
13.4.3	Receiver	138
13.4.3.1	Character Length	138
13.4.3.2	Character Reception	139
13.4.3.3	Data Sampling	140
13.4.3.4	Framing Errors	141
13.4.3.5	Baud Rate Tolerance	141
13.4.3.6	Receiver Wakeup	143
13.4.3.7	Receiver Interrupts	144
13.4.3.8	Error Interrupts	144
13.5	Low-Power Modes	144
13.5.1	Wait Mode	144
13.5.2	Stop Mode	145
13.6	ESCI During Break Module Interrupts	145
13.7	I/O Signals	145
13.7.1	PTE0/TxD (Transmit Data)	145
13.7.2	PTE1/RxD (Receive Data)	145

13.8	I/O Registers	146
13.8.1	ESCI Control Register 1	146
13.8.2	ESCI Control Register 2	148
13.8.3	ESCI Control Register 3	150
13.8.4	ESCI Status Register 1	151
13.8.5	ESCI Status Register 2	153
13.8.6	ESCI Data Register	154
13.8.7	ESCI Baud Rate Register	154
13.8.8	ESCI Prescaler Register	156
13.9	ESCI Arbiter	159
13.9.1	ESCI Arbiter Control Register	159
13.9.2	ESCI Arbiter Data Register	160
13.9.3	Bit Time Measurement	161
13.9.4	Arbitration Mode	162

Chapter 14 System Integration Module (SIM)

14.1	Introduction	163
14.2	SIM Bus Clock Control and Generation	163
14.2.1	Bus Timing	165
14.2.2	Clock Startup from POR or LVI Reset	165
14.2.3	Clocks in Stop Mode and Wait Mode	165
14.3	Reset and System Initialization	165
14.3.1	External Pin Reset	165
14.3.2	Active Resets from Internal Sources	166
14.3.2.1	Power-On Reset	166
14.3.2.2	Computer Operating Properly (COP) Reset	167
14.3.2.3	Illegal Opcode Reset	167
14.3.2.4	Illegal Address Reset	167
14.3.2.5	Forced Monitor Mode Entry Reset (MENRST)	167
14.3.2.6	Low-Voltage Inhibit (LVI) Reset	168
14.4	SIM Counter	168
14.4.1	SIM Counter During Power-On Reset	168
14.4.2	SIM Counter During Stop Mode Recovery	168
14.4.3	SIM Counter and Reset States	168
14.5	Program Exception Control	168
14.5.1	Interrupts	169
14.5.1.1	Hardware Interrupts	170
14.5.1.2	SWI Instruction	171
14.6	Interrupt Status Registers	172
14.6.1	Interrupt Status Register 1	172
14.6.2	Interrupt Status Register 2	173
14.6.3	Interrupt Status Register 3	173
14.6.4	Reset	173
14.6.5	Break Interrupts	173
14.6.6	Status Flag Protection in Break Mode	174
14.7	Low-Power Modes	174

14.7.1	Wait Mode	174
14.7.2	Stop Mode	175
14.8	SIM Registers	176
14.8.1	SIM Break Status Register	176
14.8.2	SIM Reset Status Register	177
14.8.3	SIM Break Flag Control Register	178

Chapter 15 Serial Peripheral Interface (SPI) Module

15.1	Introduction	179
15.2	Features	179
15.3	Pin Name and Register Name Conventions	179
15.4	Functional Description	181
15.4.1	Master Mode	182
15.4.2	Slave Mode	182
15.5	Transmission Formats	183
15.5.1	Clock Phase and Polarity Controls	183
15.5.2	Transmission Format When CPHA = 0	183
15.5.3	Transmission Format When CPHA = 1	184
15.5.4	Transmission Initiation Latency	185
15.6	Error Conditions	185
15.6.1	Overflow Error	186
15.6.2	Mode Fault Error	187
15.7	Interrupts	189
15.8	Queuing Transmission Data	190
15.9	Resetting the SPI	191
15.10	Low-Power Modes	191
15.10.1	Wait Mode	191
15.10.2	Stop Mode	191
15.11	SPI During Break Interrupts	191
15.12	SPI I/O Signals	192
15.12.1	MISO (Master In/Slave Out)	192
15.12.2	MOSI (Master Out/Slave In)	192
15.12.3	SPSCK (Serial Clock)	193
15.12.4	\overline{SS} (Slave Select)	193
15.12.5	V_{SS} (Clock Ground)	193
15.13	I/O Registers	194
15.13.1	SPI Control Register	194
15.13.2	SPI Status and Control Register	195
15.13.3	SPI Data Register	197

Chapter 16 Timebase Module (TBM)

16.1	Introduction	199
16.2	Features	199
16.3	Functional Description	199

16.4	Interrupts	199
16.5	TBM Interrupt Rate	200
16.6	Low-Power Modes	201
16.6.1	Wait Mode	201
16.6.2	Stop Mode	201
16.7	Timebase Control Register	202

Chapter 17 Timer Interface A (TIMA) Module

17.1	Introduction	203
17.2	Features	203
17.3	Functional Description	203
17.3.1	TIMA Counter Prescaler	203
17.3.2	Input Capture	205
17.3.3	Output Compare	206
17.3.3.1	Unbuffered Output Compare	206
17.3.3.2	Buffered Output Compare	206
17.3.4	Pulse Width Modulation (PWM)	207
17.3.4.1	Unbuffered PWM Signal Generation	208
17.3.4.2	Buffered PWM Signal Generation	208
17.3.4.3	PWM Initialization	209
17.4	Interrupts	209
17.5	Low-Power Modes	210
17.5.1	Wait Mode	210
17.5.2	Stop Mode	210
17.6	TIMA During Break Interrupts	210
17.7	I/O Signals	210
17.7.1	TIMA Channel I/O Pins (PTD0/TACH0, PTD1/TACH1)	210
17.8	I/O Registers	211
17.8.1	TIMA Status and Control Register	211
17.8.2	TIMA Counter Registers	213
17.8.3	TIMA Counter Modulo Registers	213
17.8.4	TIMA Channel Status and Control Registers	214
17.8.5	TIMA Channel Registers	217

Chapter 18 Timer Interface B (TIMB) Module

18.1	Introduction	219
18.2	Features	219
18.3	Functional Description	219
18.3.1	TIMB Counter Prescaler	219
18.3.2	Input Capture	221
18.3.3	Output Compare	222
18.3.3.1	Unbuffered Output Compare	222
18.3.3.2	Buffered Output Compare	223
18.3.4	Pulse Width Modulation (PWM)	223
18.3.4.1	Unbuffered PWM Signal Generation	224

18.3.4.2	Buffered PWM Signal Generation	224
18.3.4.3	PWM Initialization	225
18.4	Interrupts	225
18.5	Low-Power Modes	226
18.5.1	Wait Mode	226
18.5.2	Stop Mode	226
18.6	TIMB During Break Interrupts	226
18.7	I/O Signals	226
18.7.1	TIMB Channel I/O Pins (PTB7/AD7/TBCH1–PTB6/AD6/TBCH0)	226
18.8	I/O Registers	227
18.8.1	TIMB Status and Control Register	227
18.8.2	TIMB Counter Registers	229
18.8.3	TIMB Counter Modulo Registers	229
18.8.4	TIMB Channel Status and Control Registers	230
18.8.5	TIMB Channel Registers	233

Chapter 19 Development Support

19.1	Introduction	235
19.2	Break Module (BRK)	235
19.2.1	Functional Description	235
19.2.1.1	Flag Protection During Break Interrupts	237
19.2.1.2	TIM During Break Interrupts	237
19.2.1.3	COP During Break Interrupts	237
19.2.2	Break Module Registers	237
19.2.2.1	Break Status and Control Register	238
19.2.2.2	Break Address Registers	238
19.2.2.3	Break Status Register	239
19.2.2.4	Break Flag Control Register	239
19.2.3	Low-Power Modes	239
19.3	Monitor Module (MON)	240
19.3.1	Functional Description	240
19.3.1.1	Normal Monitor Mode	243
19.3.1.2	Forced Monitor Mode	244
19.3.1.3	Monitor Vectors	245
19.3.1.4	Data Format	245
19.3.1.5	Break Signal	245
19.3.1.6	Baud Rate	246
19.3.1.7	Commands	246
19.3.2	Security	249
19.3.3	Extended Security	250
19.4	Routines Supported in ROM	250
19.4.1	Variables Used in the Routines	251
19.4.2	How to Use the Routines	251
19.4.2.1	GetByte	253
19.4.2.2	PutByte	254
19.4.2.3	Verify	254

19.4.2.4	fProgram	257
19.4.2.5	fErase	259

Chapter 20 Electrical Specifications

20.1	Introduction	261
20.2	Absolute Maximum Ratings	261
20.3	Functional Operating Range	262
20.4	Thermal Characteristics	262
20.5	5V DC Electrical Characteristics	262
20.6	5V Control Timing	264
20.7	3V DC Electrical Characteristics	265
20.8	3V Control Timing	266
20.9	Internal Oscillator Characteristics	266
20.10	External Oscillator Characteristics	267
20.11	Trimmed Accuracy of the Internal Clock Generator	268
20.11.1	Trimmed Internal Clock Generator Characteristics	268
20.12	ADC10 Characteristics	268
20.13	5V SPI Characteristics	270
20.14	3V SPI Characteristics	271
20.15	Timer Interface Module Characteristics	274
20.16	Memory Characteristics	275
20.17	EMC Performance	276
20.17.1	Radiated Emissions	276
20.17.2	Conducted Transient Susceptibility	277

Chapter 21 Ordering Information and Mechanical Specifications

21.1	Introduction	279
21.2	Ordering Information	279
21.3	Package Dimensions	279

Appendix A MC68HC908EY8A

A.1	Introduction	283
A.2	Block Diagram	283
A.3	Memory	283
A.4	Ordering Information	286

Appendix B Differences Between 908EY16A and 908EY16

B.1	Introduction	287
B.2	Configuration	287
B.2.1	Enhanced Serial Communications Interface Module (ESCI)	287
B.2.2	Serial Peripheral Interface Module (SPI)	288

B.2.3	Internal Clock Generator Module (ICG)	288
B.2.4	Keyboard Interface Module (KBI)	288
B.2.5	Analog-to-Digital Converter Module (ADC)	288
B.3	Monitor Mode	289
B.3.1	Monitor Extended Security	289
B.3.2	Zeros in Security Bytes	289
B.3.3	Forced Monitor Mode Baud Rate	289
B.4	Monitor ROM FLASH Programming Routines	289
B.4.1	Erase	289
B.4.2	Program	290

Chapter 1

General Description

1.1 Introduction

The MC68HC908EY16A is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

The information contained in this document pertains to the MC68HC908EY8A with the exceptions noted in [Appendix A MC68HC908EY8A](#).

1.2 Features

For convenience, features have been organized to reflect:

- Standard features of the MC68HC908EY16A
- Features of the CPU08

Standard features of the MC68HC908EY16A include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency at 5V
- Internal oscillator requiring no external components:
 - Software selectable bus frequencies
 - 25 percent accuracy with a trimming capability of better than 1 percent
 - Clock monitor
 - Option to allow use of external clock source or external crystal/ceramic resonator
- 15,872 bytes of on-chip FLASH memory with in-circuit programming
- FLASH program memory security⁽¹⁾
- 512 bytes of on-chip random-access memory (RAM)
- Low voltage inhibit (LVI) module
- Internal clock generator module (ICG)
- Two 16-bit, 2-channel timer (TIMA and TIMB) interface modules with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- 8-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- Enhanced serial communications interface module (ESCI) for local interconnect network (LIN) connectivity
- Serial peripheral interface (SPI)

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

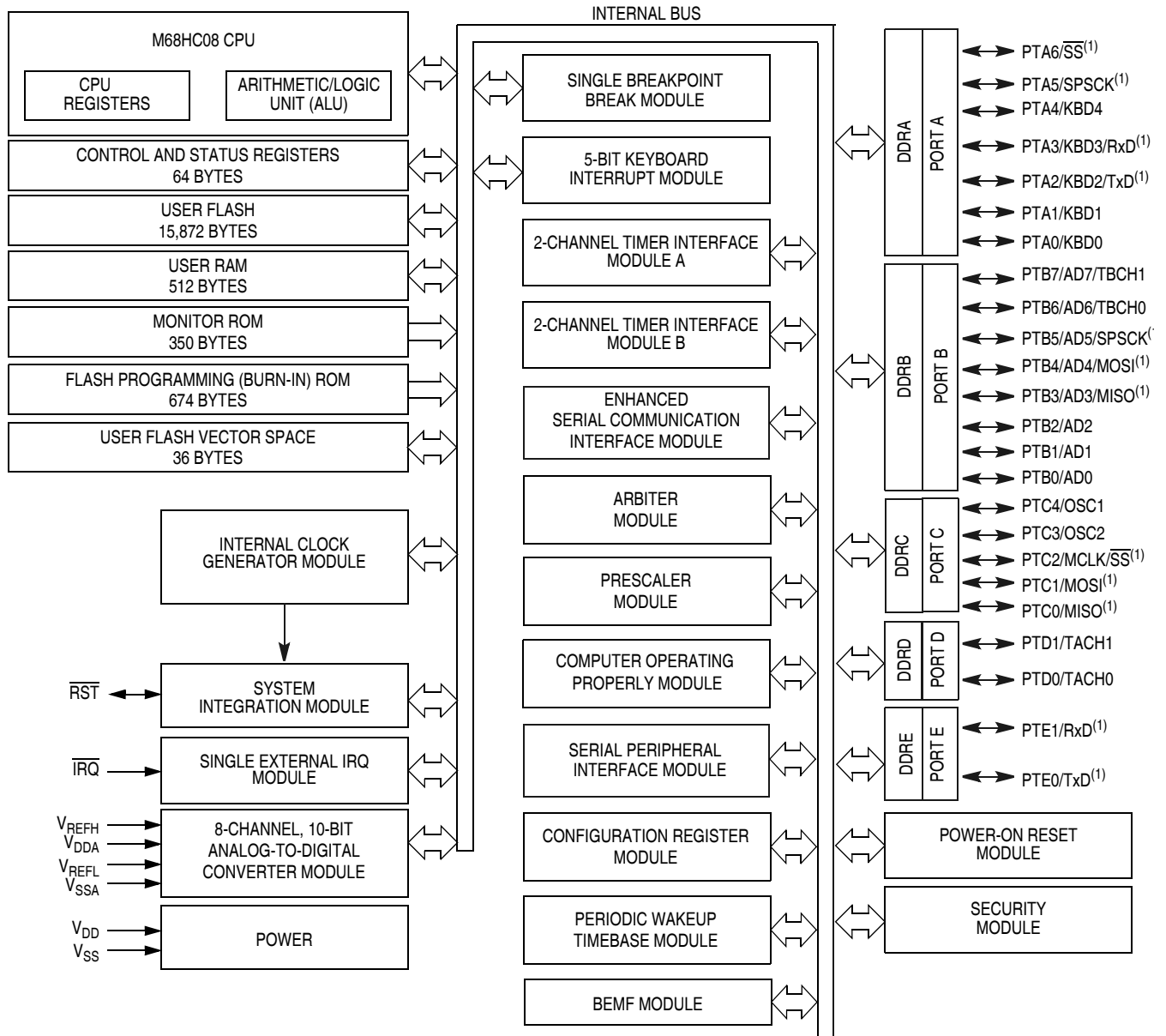
- Timebase Module (TBM)
- 5-bit keyboard wakeup port with software selectable rising or falling edge detect, as well as high- or low-level detection
 - Programmable for rising/falling edge or high/low level detection
- 24 general-purpose input/output (I/O) pins
- External asynchronous interrupt pin with internal pullup ($\overline{\text{IRQ}}$)
- System protection features:
 - Optional computer operating properly (COP) reset
 - Illegal opcode detection with reset
 - Illegal address detection with reset
- 32-pin quad flat pack (QFP) package
- Low-power design; fully static with stop and wait modes
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce customer system cost
- Standard low-power modes of operation:
 - Wait mode
 - Stop mode
- Master reset pin ($\overline{\text{RST}}$) and power-on reset (POR)
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Higher current source capability on nine port lines for LED drive (PTA6/ $\overline{\text{SS}}$, PTA5/SPSCK, PTA4/KBD4, PTA3/KBD3/RxD, PTA2/KBD2/TxD, PTA1/KBD1, PTA0/KBD0, PTC1/MOSI, and PTC0/MISO)

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8×8 multiply instruction
- Fast $16 \div 8$ divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Third party C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908EY16A.



NOTE:

1. The locations of the ESCI and SPI pins are user selectable using CONFIG3 option bits.

Figure 1-1. MCU Block Diagram

1.4 Pin Assignments

Figure 1-2 shows the pin assignments for the MC68HC908EY16A.

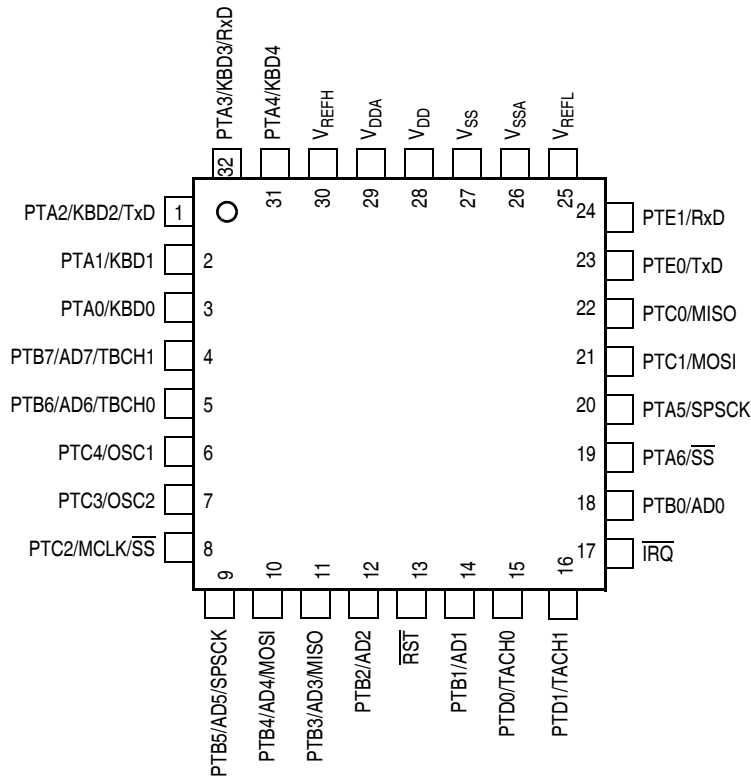


Figure 1-2. Pin Assignments

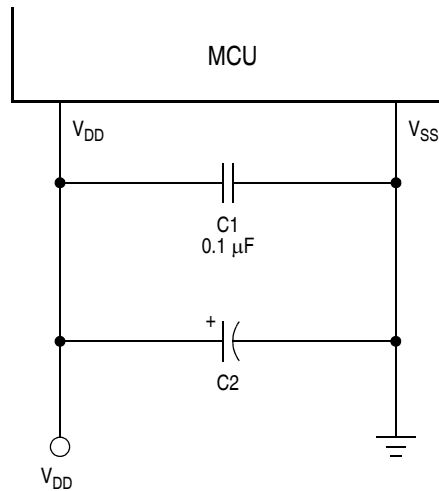
1.5 Pin Functions

Descriptions of the pin functions are provided here.

1.5.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as Figure 1-3 shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.



Note: Component values shown represent typical applications.

Figure 1-3. Power Supply Bypassing

1.5.2 Oscillator Pins (PTC4/OSC1 and PTC3/OSC2)

The OSC1 and OSC2 pins are available through programming options in the configuration register. These pins then become the connections to an external clock source or crystal/ceramic resonator.

When selecting PTC4 and PTC3 as I/O, OSC1 and OSC2 functions are not available.

1.5.3 External Reset Pin ($\overline{\text{RST}}$)

A logic 0 on the $\overline{\text{RST}}$ pin forces the MCU to a known startup state. $\overline{\text{RST}}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor that is always activated, even when the reset pin is pulled low. See [Chapter 14 System Integration Module \(SIM\)](#).

1.5.4 External Interrupt Pin ($\overline{\text{IRQ}}$)

$\overline{\text{IRQ}}$ is an asynchronous external interrupt pin. This pin contains an internal pullup resistor that is always activated, even when the $\overline{\text{IRQ}}$ pin is pulled low. See [Chapter 9 External Interrupt \(IRQ\)](#).

1.5.5 Analog Power Supply/Reference Pins (V_{DDA} , V_{REFH} , V_{SSA} , and V_{REFL})

V_{DDA} and V_{SSA} are the power supply pins for the analog-to-digital converter (ADC). Decoupling of these pins should be as per the digital supply.

NOTE

V_{REFH} is the high reference supply for the ADC. V_{DDA} should be tied to the same potential as V_{DD} via separate traces.

V_{REFL} is the low reference supply for the ADC. V_{SSA} should be tied to the same potential as V_{SS} via separate traces.

See [Chapter 3 Analog-to-Digital Converter \(ADC10\) Module](#).