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MC68HC908EY16
MC68HC908EY8

Data Sheet

M68HC08
Microcontrollers

MC68HC908EY16
Rev. 10
10/2005

freescale.com

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MC68HC908EY16
MC68HC908EY8

Data Sheet

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Refer to the Revision History for a summary of changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

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MC68HC908EY8

Glossary

Revision History

Chapter 1
General Description

1.1 Introduction

The MC68HC908EY16 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

The information contained in this document pertains to the MC68HC908EY8 with the exceptions noted in Appendix A MC68HC908EY8.

1.2 Features

For convenience, features have been organized to reflect:

- Standard features of the MC68HC908EY16
- Features of the CPU08

Standard features of the MC68HC908EY16 include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency at 5V
- Internal oscillator requiring no external components:
  - Software selectable bus frequencies
  - 25 percent accuracy with a trimming capability of better than 1 percent
  - Clock monitor
  - Option to allow use of external clock source or external crystal/ceramic resonator
- 15,872 bytes of on-chip FLASH memory with in-circuit programming
- FLASH program memory security[1]
- 512 bytes of on-chip random-access memory (RAM)
- Low voltage inhibit (LVI) module
- Internal clock generator module (ICG)
- Two 16-bit, 2-channel timer (TIMA and TIMB) interface modules with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- 8-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- Enhanced serial communications interface module (ESCI) for local interconnect network (LIN) connectivity
- Serial peripheral interface (SPI)

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

- Timebase Module (TBM)
- 5-bit keyboard interrupt (KBI) with wakeup feature
- 24 general-purpose input/output (I/O) pins
- External asynchronous interrupt pin with internal pullup ($\overline{IRQ}$)
- System protection features:
  - Optional computer operating properly (COP) reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- 32-pin quad flat pack (QFP) package
- Low-power design; fully static with stop and wait modes
- Internal pullups on $\overline{IRQ}$ and $\overline{RST}$ to reduce customer system cost
- Standard low-power modes of operation:
  - Wait mode
  - Stop mode
- Master reset pin ($\overline{RST}$) and power-on reset (POR)
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Higher current source capability on nine port lines for LED drive (PTA6/$\overline{SS}$, PTA5/SPSCK, PTA4/$\overline{KBD4}$, PTA3/$\overline{KBD3}$, PTA2/$\overline{KBD2}$, PTA1/$\overline{KBD1}$, PTA0/$\overline{KBD0}$, PTC1/MOSI, and PTC0/MISO)

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16 ÷ 8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Third party C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908EY16.

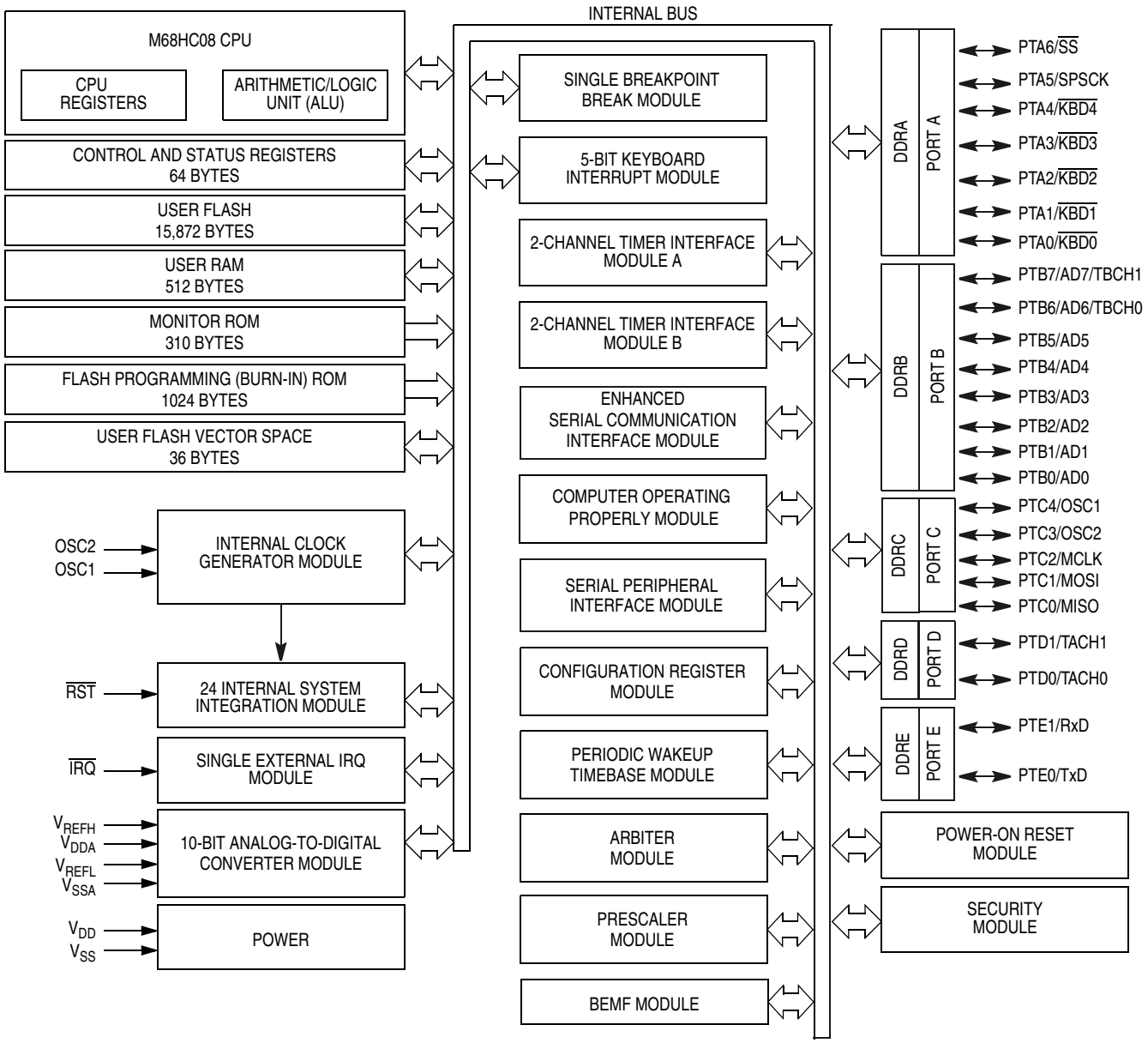


Figure 1-1. MCU Block Diagram

1.4 Pin Assignments

Figure 1-2 shows the pin assignments for the MC68HC908EY16.

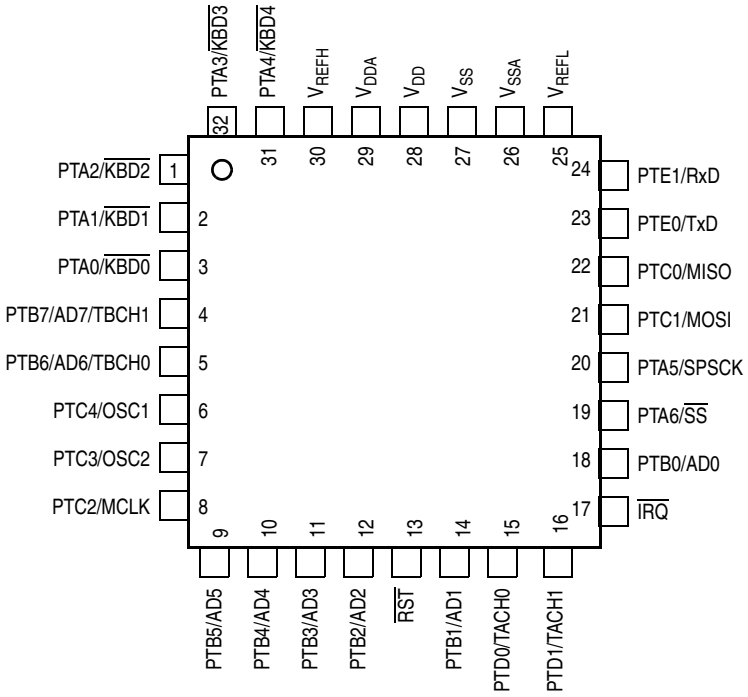


Figure 1-2. Pin Assignments

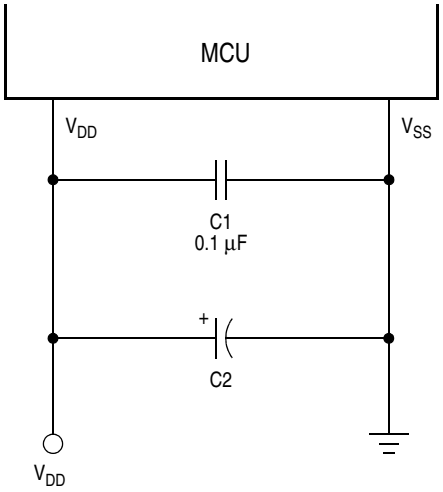
1.5 Pin Functions

Descriptions of the pin functions are provided here.

1.5.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as Figure 1-3 shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.



Note: Component values shown represent typical applications.

Figure 1-3. Power Supply Bypassing

1.5.2 Oscillator Pins (PTC4/OSC1 and PTC3/OSC2)

The OSC1 and OSC2 pins are available through programming options in the configuration register. These pins then become the connections to an external clock source or crystal/ceramic resonator.

When selecting PTC4 and PTC3 as I/O, OSC1 and OSC2 functions are not available.

1.5.3 External Reset Pin ($\overline{RST}$)

A logic 0 on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor that is always activated, even when the reset pin is pulled low. See Chapter 14 System Integration Module (SIM).

1.5.4 External Interrupt Pin ($\overline{IRQ}$)

$\overline{IRQ}$ is an asynchronous external interrupt pin. This pin contains an internal pullup resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled low. See Chapter 9 External Interrupt (IRQ).

1.5.5 Analog Power Supply/Reference Pins (V_{DDA}, V_{REFH}, V_{SSA} and V_{REFL})

V_{DDA} and V_{SSA} are the power supply pins for the analog-to-digital converter (ADC). Decoupling of these pins should be as per the digital supply.

NOTE

V_{REFH} is the high reference supply for the ADC. V_{DDA} should be tied to the same potential as V_{DD} via separate traces.

V_{REFL} is the low reference supply for the ADC. V_{SSA} should be tied to the same potential as V_{SS} via separate traces.

See Chapter 3 Analog-to-Digital Converter (ADC) Module.

1.5.6 Port A I/O Pins (PTA6/$\overline{SS}$, PTA5/SPSCK, PTA4/$\overline{KBD4}$–PTA0/$\overline{KBD0}$)

Port A input/output (I/O) pins (PTA6/$\overline{SS}$, PTA5/SPSCK, PTA4/$\overline{KBD4}$, PTA3/$\overline{KBD3}$, PTA2/$\overline{KBD2}$, PTA1/$\overline{KBD1}$, and PTA0/$\overline{KBD0}$) are special-function, bidirectional I/O port pins. PTA5 and PTA6 are shared with the serial peripheral interface (SPI). PTA4-PTA0 can be programmed to serve as keyboard interrupt pins.

See Chapter 12 Input/Output (I/O) Ports (PORTS) and Chapter 9 External Interrupt (IRQ).

1.5.7 Port B I/O Pins (PTB7/AD7/TBCH1, PTB6/AD6/TBCH0, PTB5/AD5–PTB0/AD0)

PTB7/AD7/TBCH1, PTB6/AD6/TBCH0, and PTB5/AD5–PTB0/AD0 are special-function, bidirectional I/O port pins that can also be used for ADC inputs. PTB7/AD7/TBCH1 and PTB6/AD6/TBCH0 are special function bidirectional I/O port pins that can also be used for timer interface pins.

See and Chapter 3 Analog-to-Digital Converter (ADC) Module and Chapter 17 Timer Interface A (TIMA) Module.

1.5.8 Port C I/O Pins (PTC4/OSC1, PTC3/OSC2, PTC2/MCLK, PTC1/MOSI, PTC0/MISO)

PTC4/OSC1–PTC0/MISO are special-function, bidirectional I/O port pins. See Chapter 12 Input/Output (I/O) Ports (PORTS). PTC3/OSC2 and PTC4/OSC1 are shared with the on-chip oscillator circuit through configuration options. See Chapter 8 Internal Clock Generator (ICG) Module.

When applications require:

- PTC3/OSC2 can be programmed to be OSC2
- PTC4/OSC1 can be programmed to be OSC1

PTC2/MCLK is software selectable to be MCLK, or bus clock out. PTC1/MOSI can be programmed to be the MOSI signal for the SPI. PTC0/MISO can be programmed to be the MISO signal for the SPI.

1.5.9 Port D I/O Pins (PTD1/TACH1–PTD0/TACH0)

PTD1/TACH1–PTD0/TACH0 are special-function, bidirectional I/O port pins that can also be programmed to be timer pins.

See Chapter 17 Timer Interface A (TIMA) Module and Chapter 12 Input/Output (I/O) Ports (PORTS).

1.5.10 Port E I/O Pins (PTE1/RxD–PTE0/TxD)

PTE1/RxD–PTE0/TxD are special-function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication interface (ESCI) pins.

See Chapter 13 Enhanced Serial Communications Interface (ESCI) Module and Chapter 12 Input/Output (I/O) Ports (PORTS).

NOTE

Any unused inputs and I/O ports should be tied to an appropriate logic level (either V_{DD} or V_{SS}). Although the I/O ports of the MC68HC908EY16 do not require termination, termination is recommended to reduce the possibility of electro-static discharge damage.

Chapter 2
Memory

2.1 Introduction

The M68HC08 central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in Figure 2-1, includes:

- 16 Kbytes of FLASH memory, 15, 872 bytes of user space
- 512 bytes of random-access memory (RAM)
- 36 bytes of user-defined vectors
- 310 bytes of monitor routines in read-only memory (ROM)
- 1024 bytes of integrated FLASH burn-in routines in ROM

2.2 Unimplemented Memory Locations

Accessing an unimplemented location can cause an illegal address reset. In the memory map (Figure 2-1) and in register figures in this document, unimplemented locations are shaded.

2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on microcontroller unit (MCU) operation. In the Figure 2-1 and in register figures in this document, reserved locations are marked with the word reserved or with the letter R.

2.4 Input/Output (I/O) Section

Most of the control, status, and data registers are in the zero page area of $0000–$003F. Additional I/O registers have these addresses:

- $FE00; SIM break status register, SBSR
- $FE01; SIM reset status register, SRSR
- $FE03; SIM break flag control register, SBFCR
- $FE08; FLASH control register, FLCR
- $FE09; break address register high, BRKH
- $FE0A; break address register low, BRKL
- $FE0B; break status and control register, BRKSCR
- $FE0C; LVI status register, LVISR
- $FF7E; FLASH block protect register, FLBPR
- $FF80; ICG trim value (optional), ICGT

Data registers are shown in Figure 2-2. and Table 2-1 is a list of vector locations.