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# MC68HC908GP32

Data Sheet

***M68HC08***  
***Microcontrollers***

MC68HC908GP32  
Rev. 10  
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# MC68HC908GP32

## Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

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# Revision History

Date	Revision Level	Description	Page Number(s)
July, 2001	5	In Table 15-1, second cell in "Comment" column, corrected PTC to PTC1.	199
		In Figure 21-2, Timebase control register, bit 0 is a reserved bit.	337
		Updated crystal oscillator component values in 23.17.1 CGM Component Specifications.	387
		Added appendix A: MC68HC08GP32 — ROM part.	397
August, 2002	6	Section 22. Timer Interface Module (TIM) — Timer discrepancies corrected throughout this section.	341
		Section 24. Mechanical Specifications — Replaced incorrect 44-pin QFP drawing, case 824E to case 824A.	393
August, 2005	6.1	Updated to meet Freescale identity guidelines.	Throughout
March, 2006	7	3.5 Clock Generator Module (CGM) — Updated description to remove erroneous information.	46
		19.16.1 CGM Component Specifications — Updated to reflect correct values.	250
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		<a href="#">Chapter 2 Memory</a> — Integrated RAM and FLASH sections	N/A
		<a href="#">2.6 FLASH Memory</a> — Updated FLASH erase, programming, and block protect information	38
		<a href="#">4.7.1 ADC Status and Control Register</a> — Corrected COCO bit description	56
		<a href="#">9.4 Interrupts</a> — Updated External Interrupt Module information	103
		<a href="#">Chapter 10 Keyboard Interrupt (KBI) Module</a> — Updated KBI module information	105
		<a href="#">Chapter 12 Input/Output (I/O) Ports</a> — Added unused pins note	115
		<a href="#">Chapter 13 Serial Communications Interface Module (SCI)</a> — Removed DMA references	131
		<a href="#">Figure 13-1. SCI Module Block Diagram</a> — Replaced SCI block diagram	133
<a href="#">Figure 13-4. SCI Transmitter Block Diagram</a> — Replaced SCI transmitter block diagram	135		

# Revision History

Date	Revision Level	Description	Page Number(s)
January, 2008	10	Figure 13-5. SCI Receiver Block Diagram — Replaced SCI receiver block diagram	138
		Chapter 14 System Integration Module (SIM) — Corrected Break interrupt and SBSW bit descriptions	157
		14.7.2 SIM Reset Status Register — Updated SIM reset status register information	172
		Chapter 15 Serial Peripheral Interface Module (SPI) — Deleted IIC reference	175
		Chapter 15 Serial Peripheral Interface Module (SPI) — Removed DMA references	175
		Figure 15-2. SPI Module Block Diagram — Replaced SPI module block diagram	177
		Table 17-3. Mode, Edge, and Level Selection — Added software output compare to mode table	212
		Chapter 18 Development Support — Integrated Break module and monitor mode chapters into Development Support Chapter	215



## Revision History

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# Chapter 1

## General Description

### 1.1 Introduction

The MC68HC908GP32 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

### 1.2 Features

For convenience, features have been organized to reflect:

- Standard features of the MC68HC908GP32
- Features of the CPU08

#### 1.2.1 Standard Features of the MC68HC908GP32

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- FLASH program memory security<sup>(1)</sup>
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- In-system programming
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with optional reset and selectable trip points for 3.0-V and 5.0-V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Low-power design; fully static with stop and wait modes
- Standard low-power modes of operation:
  - Wait mode
  - Stop mode
- Master reset pin and power-on reset (POR)
- 32 Kbytes of on-chip FLASH memory with in-circuit programming capabilities of FLASH program memory
- 512 bytes of on-chip random-access memory (RAM)
- Serial peripheral interface module (SPI)
- Serial communications interface module (SCI)

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1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

## General Description

- Two 16-bit, 2-channel timer interface modules (TIM1 and TIM2) with selectable input capture, output compare, and PWM capability on each channel
- 8-channel, 8-bit successive approximation analog-to-digital converter (ADC)
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Internal pullups on  $\overline{IRQ}$  and  $\overline{RST}$  to reduce customer system cost
- Clock generator module with on-chip 32-kHz crystal compatible PLL (phase-lock loop)
- Up to 33 general-purpose input/output (I/O) pins, including:
  - 26 shared-function I/O pins
  - Five or seven dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- High current 10-mA sink/10-mA source capability on all port pins
- Higher current 15-mA sink/source capability on PTC0–PTC4
- Timebase module with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external 32-kHz crystal
- Oscillator stop mode enable bit (OSCSTOPENB) in the CONFIG register to allow user selection of having the oscillator enabled or disabled during stop mode
- 8-bit keyboard wakeup port
- 40-pin plastic dual-in-line package (PDIP), 42-pin shrink dual-in-line package (SDIP), or 44-pin quad flat pack (QFP)
- Specific features of the MC68HC908GP32 in 40-pin PDIP are:
  - Port C is only 5 bits: PTC0–PTC4
  - Port D is only 6 bits: PTD0–PTD5; single 2-channel TIM module
- Specific features of the MC68HC908GP32 in 42-pin SDIP are:
  - Port C is only 5 bits: PTC0–PTC4
  - Port D is 8 bits: PTD0–PTD7; dual 2-channel TIM modules
- Specific features of the MC68HC908GP32 in 44-pin QFP are:
  - Port C is 7 bits: PTC0–PTC6
  - Port D is 8 bits: PTD0–PTD7; dual 2-channel TIM modules

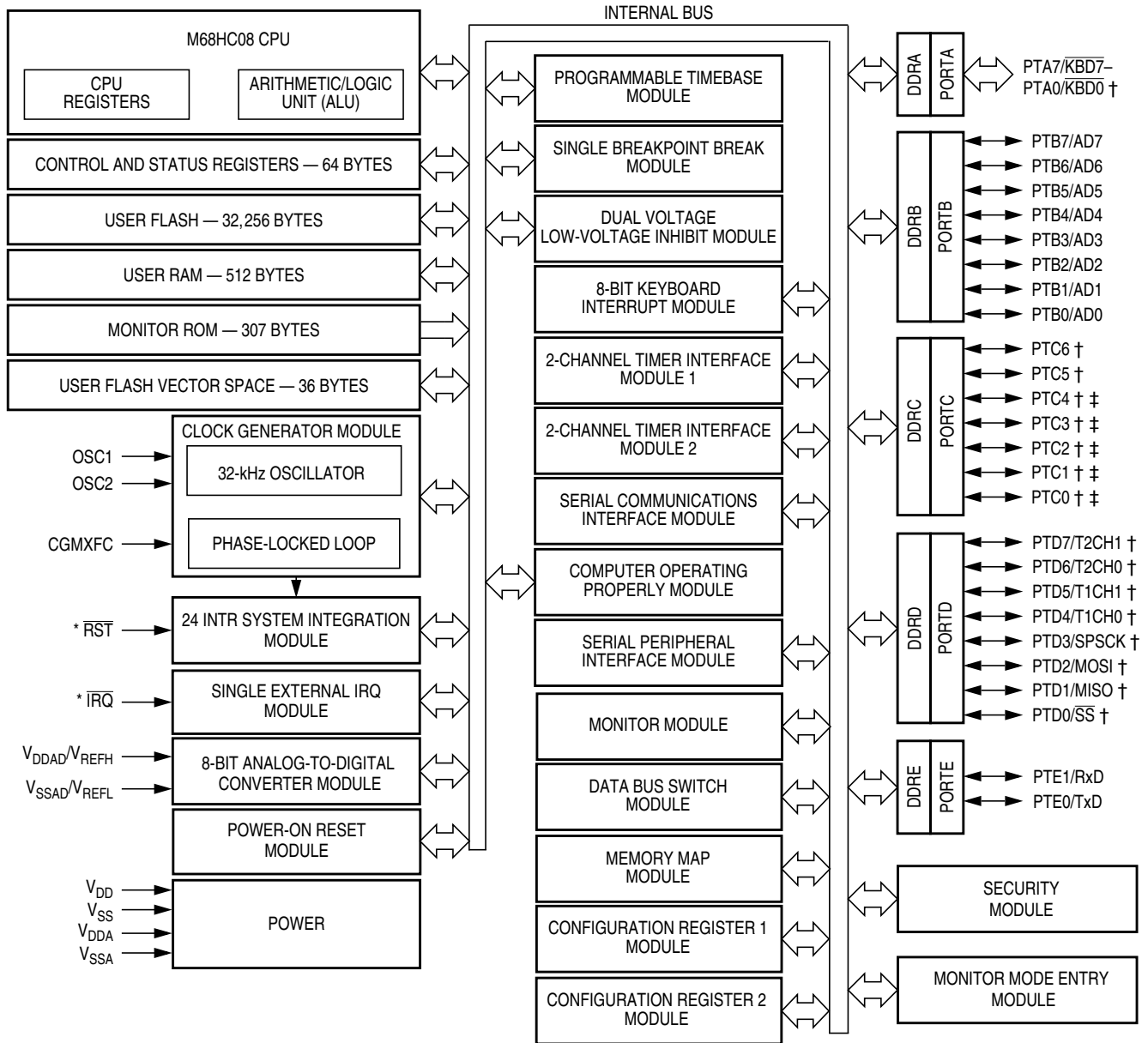
### 1.2.2 Features of the CPU08

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

### 1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908GP32. Text in parentheses within a module block indicates the module name. Text in parentheses next to a signal indicates the module which uses the signal.

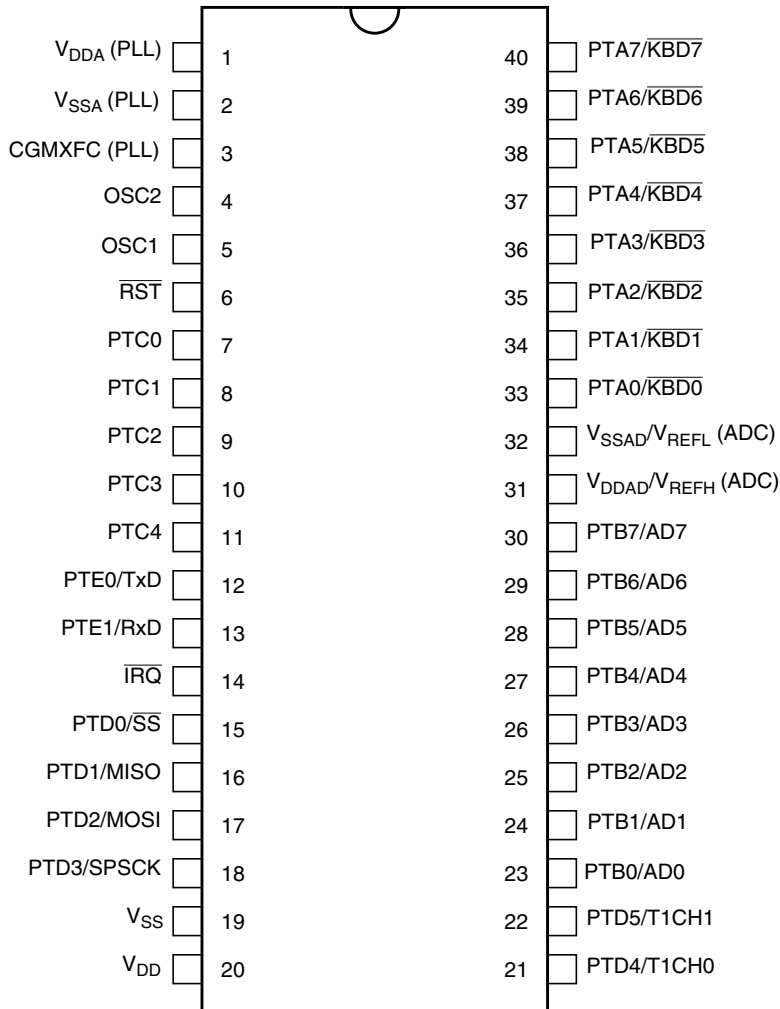


† Ports are software configurable with pullup device if input port.  
 ‡ Higher current drive port pins  
 \* Pin contains integrated pullup device

Figure 1-1. MCU Block Diagram

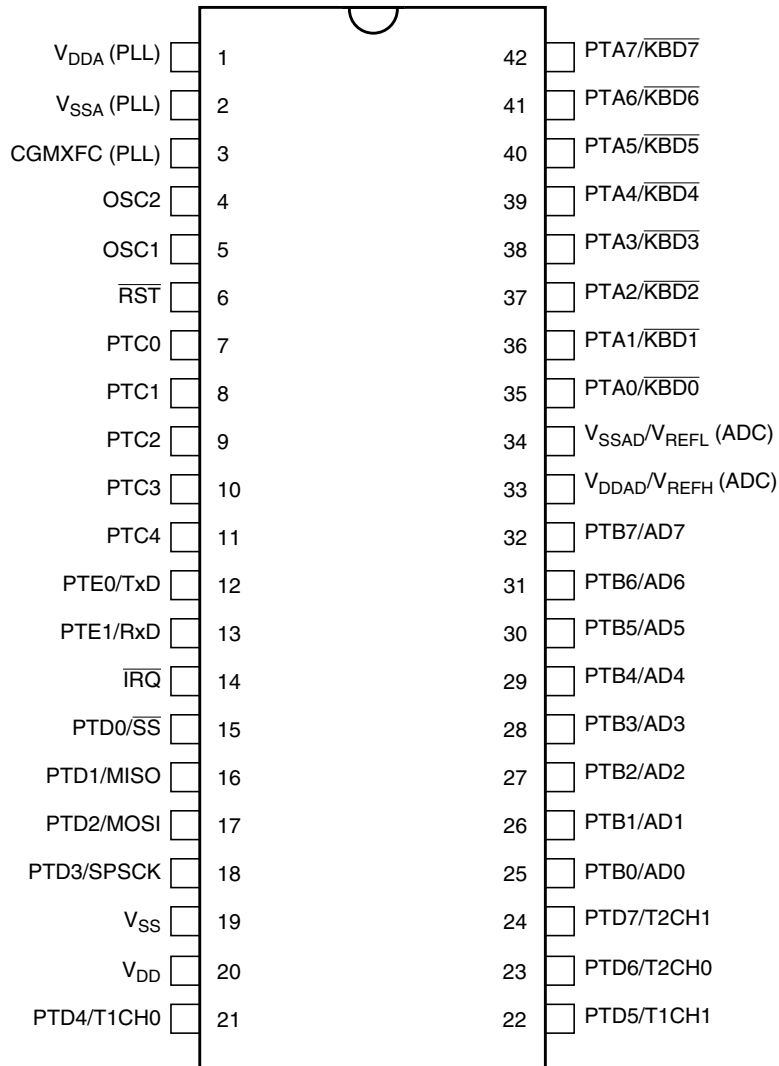


## 1.4 Pin Assignments



Pins Not Available on 40-Pin Package	Internal Connection
PTC5	Connected to ground
PTC6	Connected to ground
PTD6/T2CH0	Unconnected
PTD7/T2CH1	Unconnected

Figure 1-2. 40-Pin PDIP Pin Assignments



Pins Not Available on 42-Pin Package	Internal Connection
PTC5	Connected to ground
PTC6	Connected to ground

Figure 1-3. 42-Pin SDIP Pin Assignments