



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



MC68HC908GR60A MC68HC908GR48A MC68HC908GR32A

Data Sheet

*M68HC08
Microcontrollers*

MC68HC908GR60A
Rev. 5
04/2007

freescale.com

MC68HC908GR60A

MC68HC908GR48A

MC68HC908GR32A

Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.
This product incorporates SuperFlash® technology licensed from SST.

© Freescale Semiconductor, Inc., 2004, 2006, 2007. All rights reserved.

Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

| Date | Revision Level | Description | Page Number(s) |
|-------------|----------------|---|---|
| April, 2004 | N/A | Initial release | N/A |
| July, 2004 | 1 | 9.7.3 Keyboard Interrupt Polarity Register — Corrected description of KBIP7–KBIP0. | 119 |
| June, 2005 | 2 | Table 13-6. ESCI LIN Control Bits — Corrected Functionality definitions | 174 |
| | | 13.9.1 ESCI Arbiter Control Register — Corrected definition for ACLK bit. | 179 |
| | | 13.9.3 Bit Time Measurement — Corrected description of ACLK bit. | 180 |
| March, 2006 | 3 | 10.5 Clock Generator Module (CGM) — Updated description to remove erroneous information. | 122 |
| July, 2006 | 4 | Added 1.5.15 Unused Pin Termination | 28 |
| | | 12.1 Introduction — Replaced note | 131 |
| | | Table 13-6. ESCI LIN Control Bits — Corrected functionality column. | 174 |
| | | The following sections were updated to show that a break interrupt inhibits input captures: 17.6 TIM1 During Break Interrupts 18.6 TIM2 During Break Interrupts 19.2.1.2 TIM During Break Interrupts | 233 251 264 |
| | | Figure 19-10. Normal Monitor Mode Circuit and Figure 19-11. Forced Monitor Mode — Changed capacitor values | 269 |
| | | 20.5 5.0-Vdc Electrical Characteristics — Updated minimum value for low-voltage inhibit, trip rising voltage (V_{TRIPR}). | 279 |
| | | 20.9.1 CGM Component Specifications — Updated values for feedback bias resistor | 284 |
| April, 2007 | 5 | Figure 2-2. Control, Status, and Data Registers — Replaced TBMCLKSEL with TMBCLKSEL to be compatible with development tool nomenclature | 33 90 |
| | | Chapter 5 Configuration Register (CONFIG) — Replaced COPCLK with CGMXCLK | 89 91 |
| | | 10.6.2 Stop Mode — Replaced COPCLK with CGMXCLK | 122 |
| | | Figure 13-3. ESCI Module Block Diagram — Changed BUS_CLK to Bus Clock and deleted reference to 4x BUSCLK | 154 |
| | | 13.4.2 Transmitter — Changed ESCIBDSRC to SCIBDSRC | 156 |
| | | 13.9.1 ESCI Arbiter Control Register and 13.9.3 Bit Time Measurement — Replaced one quarter with one half in the definition for ACLK = 1 | 179 180 |
| | | Chapter 16 Timebase Module (TBM) — Replaced TBMCLKSEL with TMBCLKSEL to be compatible with development tool nomenclature | 222 223 |
| | | 20.5 5.0-Vdc Electrical Characteristics and 20.6 3.3-Vdc Electrical Characteristics — Updated tables | 279 281 |
| | | 20.9 Clock Generation Module (CGM) Characteristics — Updated section to include the following: 20.9.1 CGM Operating Conditions 20.9.2 CGM Component Information 20.9.3 CGM Acquisition/Lock Time Information | 284 284 285 |

List of Chapters

| | |
|---|-----|
| Chapter 1 General Description | 19 |
| Chapter 2 Memory | 29 |
| Chapter 3 Analog-to-Digital Converter (ADC) | 59 |
| Chapter 4 Clock Generator Module (CGM) | 71 |
| Chapter 5 Configuration Register (CONFIG) | 89 |
| Chapter 6 Computer Operating Properly (COP) Module | 93 |
| Chapter 7 Central Processor Unit (CPU) | 97 |
| Chapter 8 External Interrupt (IRQ) | 109 |
| Chapter 9 Keyboard Interrupt Module (KBI) | 113 |
| Chapter 10 Low-Power Modes | 121 |
| Chapter 11 Low-Voltage Inhibit (LVI) | 127 |
| Chapter 12 Input/Output (I/O) Ports | 131 |
| Chapter 13 Enhanced Serial Communications Interface (ESCI) Module | 151 |
| Chapter 14 System Integration Module (SIM) | 183 |
| Chapter 15 Serial Peripheral Interface (SPI) Module | 201 |
| Chapter 16 Timebase Module (TBM) | 221 |
| Chapter 17 Timer Interface Module (TIM1) | 225 |
| Chapter 18 Timer Interface Module (TIM2) | 241 |
| Chapter 19 Development Support | 261 |
| Chapter 20 Electrical Specifications | 277 |
| Chapter 21 Ordering Information and Mechanical Specifications | 295 |
| Appendix A MC68HC908GR48A | 305 |
| Appendix B MC68HC908GR32A | 309 |



List of Chapters

Table of Contents

Chapter 1 General Description

| | | |
|--------|---|----|
| 1.1 | Introduction | 19 |
| 1.2 | Features | 19 |
| 1.2.1 | Standard Features | 19 |
| 1.2.2 | Features of the CPU08 | 21 |
| 1.3 | MCU Block Diagram | 21 |
| 1.4 | Pin Assignments | 23 |
| 1.5 | Pin Functions | 25 |
| 1.5.1 | Power Supply Pins (V_{DD} and V_{SS}) | 25 |
| 1.5.2 | Oscillator Pins (OSC1 and OSC2) | 26 |
| 1.5.3 | External Reset Pin (\overline{RST}) | 26 |
| 1.5.4 | External Interrupt Pin (\overline{IRQ}) | 26 |
| 1.5.5 | CGM Power Supply Pins (V_{DDA} and V_{SSA}) | 26 |
| 1.5.6 | External Filter Capacitor Pin (CGMXFC) | 26 |
| 1.5.7 | ADC Power Supply/Reference Pins (V_{DDAD}/V_{REFH} and V_{SSAD}/V_{REFL}) | 26 |
| 1.5.8 | Port A Input/Output (I/O) Pins (PTA7/KBD7/AD15–PTA0/KBD0/AD8) | 27 |
| 1.5.9 | Port B I/O Pins (PTB7/AD7–PTB0/AD0) | 27 |
| 1.5.10 | Port C I/O Pins (PTC6–PTC0) | 27 |
| 1.5.11 | Port D I/O Pins (PTD7/T2CH1–PTD0/ \overline{SS}) | 27 |
| 1.5.12 | Port E I/O Pins (PTE5–PTE2, PTE1/RxD, and PTE0/TxD) | 27 |
| 1.5.13 | Port F I/O Pins (PTF7/T2CH5–PTF0) | 27 |
| 1.5.14 | Port G I/O Pins (PTG7/AD23–PTBG0/AD16) | 28 |
| 1.5.15 | Unused Pin Termination | 28 |

Chapter 2 Memory

| | | |
|---------|---|----|
| 2.1 | Introduction | 29 |
| 2.2 | Unimplemented Memory Locations | 29 |
| 2.3 | Reserved Memory Locations | 29 |
| 2.4 | Input/Output (I/O) Section | 29 |
| 2.5 | Random-Access Memory (RAM) | 41 |
| 2.6 | FLASH-1 Memory (FLASH-1) | 41 |
| 2.6.1 | Functional Description | 41 |
| 2.6.2 | FLASH-1 Control and Block Protect Registers | 42 |
| 2.6.2.1 | FLASH-1 Control Register | 42 |
| 2.6.2.2 | FLASH-1 Block Protect Register | 43 |
| 2.6.3 | FLASH-1 Block Protection | 44 |
| 2.6.4 | FLASH-1 Mass Erase Operation | 45 |
| 2.6.5 | FLASH-1 Page Erase Operation | 46 |

Table of Contents

| | | |
|---------|---|----|
| 2.6.6 | FLASH-1 Program Operation | 47 |
| 2.6.7 | Low-Power Modes | 48 |
| 2.6.7.1 | Wait Mode | 48 |
| 2.6.7.2 | Stop Mode | 48 |
| 2.7 | FLASH-2 Memory (FLASH-2) | 50 |
| 2.7.1 | Functional Description | 50 |
| 2.7.2 | FLASH-2 Control and Block Protect Registers | 50 |
| 2.7.2.1 | FLASH-2 Control Register | 50 |
| 2.7.2.2 | FLASH-2 Block Protect Register | 51 |
| 2.7.3 | FLASH-2 Block Protection | 52 |
| 2.7.4 | FLASH-2 Mass Erase Operation | 53 |
| 2.7.5 | FLASH-2 Page Erase Operation | 54 |
| 2.7.6 | FLASH-2 Program Operation | 55 |
| 2.7.7 | Low-Power Modes | 56 |
| 2.7.7.1 | Wait Mode | 56 |
| 2.7.7.2 | Stop Mode | 56 |

Chapter 3 Analog-to-Digital Converter (ADC)

| | | |
|---------|---|----|
| 3.1 | Introduction | 59 |
| 3.2 | Features | 59 |
| 3.3 | Functional Description | 59 |
| 3.3.1 | ADC Port I/O Pins | 59 |
| 3.3.2 | Voltage Conversion | 61 |
| 3.3.3 | Conversion Time | 62 |
| 3.3.4 | Conversion | 62 |
| 3.3.5 | Accuracy and Precision | 62 |
| 3.3.6 | Result Justification | 62 |
| 3.4 | Monotonicity | 63 |
| 3.5 | Interrupts | 63 |
| 3.6 | Low-Power Modes | 63 |
| 3.6.1 | Wait Mode | 63 |
| 3.6.2 | Stop Mode | 64 |
| 3.7 | I/O Signals | 64 |
| 3.7.1 | ADC Analog Power Pin (V_{DDAD}) | 64 |
| 3.7.2 | ADC Analog Ground Pin (V_{SSAD}) | 64 |
| 3.7.3 | ADC Voltage Reference High Pin (V_{REFH}) | 64 |
| 3.7.4 | ADC Voltage Reference Low Pin (V_{REFL}) | 65 |
| 3.7.5 | ADC Voltage In (V_{ADIN}) | 65 |
| 3.8 | I/O Registers | 65 |
| 3.8.1 | ADC Status and Control Register | 65 |
| 3.8.2 | ADC Data Register High and Data Register Low | 67 |
| 3.8.2.1 | Left Justified Mode | 67 |
| 3.8.2.2 | Right Justified Mode | 68 |
| 3.8.2.3 | Left Justified Signed Data Mode | 68 |
| 3.8.2.4 | Eight Bit Truncation Mode | 69 |
| 3.8.3 | ADC Clock Register | 69 |

Chapter 4 Clock Generator Module (CGM)

| | | |
|--------|--|----|
| 4.1 | Introduction | 71 |
| 4.2 | Features | 71 |
| 4.3 | Functional Description | 71 |
| 4.3.1 | Crystal Oscillator Circuit | 73 |
| 4.3.2 | Phase-Locked Loop Circuit (PLL) | 73 |
| 4.3.3 | PLL Circuits | 73 |
| 4.3.4 | Acquisition and Tracking Modes | 74 |
| 4.3.5 | Manual and Automatic PLL Bandwidth Modes | 74 |
| 4.3.6 | Programming the PLL | 75 |
| 4.3.7 | Special Programming Exceptions | 77 |
| 4.3.8 | Base Clock Selector Circuit | 77 |
| 4.3.9 | CGM External Connections | 78 |
| 4.4 | I/O Signals | 78 |
| 4.4.1 | Crystal Amplifier Input Pin (OSC1) | 79 |
| 4.4.2 | Crystal Amplifier Output Pin (OSC2) | 79 |
| 4.4.3 | External Filter Capacitor Pin (CGMXFC) | 79 |
| 4.4.4 | PLL Analog Power Pin (V_{DDA}) | 79 |
| 4.4.5 | PLL Analog Ground Pin (V_{SSA}) | 79 |
| 4.4.6 | Oscillator Enable Signal (SIMOSCEN) | 79 |
| 4.4.7 | Oscillator Enable in Stop Mode Bit (OSCENINSTOP) | 79 |
| 4.4.8 | Crystal Output Frequency Signal (CGMXCLK) | 79 |
| 4.4.9 | CGM Base Clock Output (CGMOUT) | 80 |
| 4.4.10 | CGM CPU Interrupt (CGMINT) | 80 |
| 4.5 | CGM Registers | 80 |
| 4.5.1 | PLL Control Register | 81 |
| 4.5.2 | PLL Bandwidth Control Register | 82 |
| 4.5.3 | PLL Multiplier Select Register High | 83 |
| 4.5.4 | PLL Multiplier Select Register Low | 84 |
| 4.5.5 | PLL VCO Range Select Register | 84 |
| 4.6 | Interrupts | 85 |
| 4.7 | Special Modes | 85 |
| 4.7.1 | Wait Mode | 85 |
| 4.7.2 | Stop Mode | 86 |
| 4.7.3 | CGM During Break Interrupts | 86 |
| 4.8 | Acquisition/Lock Time Specifications | 86 |
| 4.8.1 | Acquisition/Lock Time Definitions | 86 |
| 4.8.2 | Parametric Influences on Reaction Time | 86 |
| 4.8.3 | Choosing a Filter | 87 |

Chapter 5 Configuration Register (CONFIG)

| | | |
|-----|------------------------|----|
| 5.1 | Introduction | 89 |
| 5.2 | Functional Description | 89 |

Chapter 6 Computer Operating Properly (COP) Module

| | | |
|-------|--|----|
| 6.1 | Introduction | 93 |
| 6.2 | Functional Description | 93 |
| 6.3 | I/O Signals | 94 |
| 6.3.1 | CGMXCLK | 94 |
| 6.3.2 | STOP Instruction | 94 |
| 6.3.3 | COPCTL Write | 94 |
| 6.3.4 | Power-On Reset. | 94 |
| 6.3.5 | Internal Reset. | 94 |
| 6.3.6 | COPD (COP Disable). | 95 |
| 6.3.7 | COPRS (COP Rate Select) | 95 |
| 6.4 | COP Control Register | 95 |
| 6.5 | Interrupts | 95 |
| 6.6 | Monitor Mode | 95 |
| 6.7 | Low-Power Modes | 95 |
| 6.7.1 | Wait Mode | 95 |
| 6.7.2 | Stop Mode | 95 |
| 6.8 | COP Module During Break Mode | 96 |

Chapter 7 Central Processor Unit (CPU)

| | | |
|-------|---------------------------------------|-----|
| 7.1 | Introduction | 97 |
| 7.2 | Features. | 97 |
| 7.3 | CPU Registers | 97 |
| 7.3.1 | Accumulator | 98 |
| 7.3.2 | Index Register | 98 |
| 7.3.3 | Stack Pointer | 99 |
| 7.3.4 | Program Counter | 99 |
| 7.3.5 | Condition Code Register | 100 |
| 7.4 | Arithmetic/Logic Unit (ALU) | 101 |
| 7.5 | Low-Power Modes | 101 |
| 7.5.1 | Wait Mode | 101 |
| 7.5.2 | Stop Mode | 101 |
| 7.6 | CPU During Break Interrupts | 101 |
| 7.7 | Instruction Set Summary | 102 |
| 7.8 | Opcode Map | 107 |

Chapter 8 External Interrupt (IRQ)

| | | |
|-----|--|-----|
| 8.1 | Introduction | 109 |
| 8.2 | Features. | 109 |
| 8.3 | Functional Description | 109 |
| 8.4 | IRQ Pin | 111 |
| 8.5 | IRQ Module During Break Interrupts | 111 |
| 8.6 | IRQ Status and Control Register | 112 |

Chapter 9 Keyboard Interrupt Module (KBI)

| | | |
|-------|---|-----|
| 9.1 | Introduction | 113 |
| 9.2 | Features | 113 |
| 9.3 | Functional Description | 113 |
| 9.4 | Keyboard Initialization | 116 |
| 9.5 | Low-Power Modes | 117 |
| 9.5.1 | Wait Mode | 117 |
| 9.5.2 | Stop Mode | 117 |
| 9.6 | Keyboard Module During Break Interrupts | 117 |
| 9.7 | I/O Registers | 117 |
| 9.7.1 | Keyboard Status and Control Register | 118 |
| 9.7.2 | Keyboard Interrupt Enable Register | 119 |
| 9.7.3 | Keyboard Interrupt Polarity Register | 119 |

Chapter 10 Low-Power Modes

| | | |
|--------|--|-----|
| 10.1 | Introduction | 121 |
| 10.1.1 | Wait Mode | 121 |
| 10.1.2 | Stop Mode | 121 |
| 10.2 | Analog-to-Digital Converter (ADC) | 121 |
| 10.2.1 | Wait Mode | 121 |
| 10.2.2 | Stop Mode | 121 |
| 10.3 | Break Module (BRK) | 121 |
| 10.3.1 | Wait Mode | 121 |
| 10.3.2 | Stop Mode | 121 |
| 10.4 | Central Processor Unit (CPU) | 122 |
| 10.4.1 | Wait Mode | 122 |
| 10.4.2 | Stop Mode | 122 |
| 10.5 | Clock Generator Module (CGM) | 122 |
| 10.5.1 | Wait Mode | 122 |
| 10.5.2 | Stop Mode | 122 |
| 10.6 | Computer Operating Properly Module (COP) | 122 |
| 10.6.1 | Wait Mode | 122 |
| 10.6.2 | Stop Mode | 122 |
| 10.7 | External Interrupt Module (IRQ) | 123 |
| 10.7.1 | Wait Mode | 123 |
| 10.7.2 | Stop Mode | 123 |
| 10.8 | Keyboard Interrupt Module (KBI) | 123 |
| 10.8.1 | Wait Mode | 123 |
| 10.8.2 | Stop Mode | 123 |
| 10.9 | Low-Voltage Inhibit Module (LVI) | 123 |
| 10.9.1 | Wait Mode | 123 |
| 10.9.2 | Stop Mode | 123 |

Table of Contents

| | | |
|---------|--|-----|
| 10.10 | Enhanced Serial Communications Interface Module (ESCI) | 123 |
| 10.10.1 | Wait Mode | 123 |
| 10.10.2 | Stop Mode | 123 |
| 10.11 | Serial Peripheral Interface Module (SPI) | 124 |
| 10.11.1 | Wait Mode | 124 |
| 10.11.2 | Stop Mode | 124 |
| 10.12 | Timer Interface Module (TIM1 and TIM2) | 124 |
| 10.12.1 | Wait Mode | 124 |
| 10.12.2 | Stop Mode | 124 |
| 10.13 | Timebase Module (TBM) | 124 |
| 10.13.1 | Wait Mode | 124 |
| 10.13.2 | Stop Mode | 124 |
| 10.14 | Exiting Wait Mode | 125 |
| 10.15 | Exiting Stop Mode | 126 |

Chapter 11 Low-Voltage Inhibit (LVI)

| | | |
|--------|-------------------------------------|-----|
| 11.1 | Introduction | 127 |
| 11.2 | Features | 127 |
| 11.3 | Functional Description | 127 |
| 11.3.1 | Polled LVI Operation | 128 |
| 11.3.2 | Forced Reset Operation | 128 |
| 11.3.3 | Voltage Hysteresis Protection | 129 |
| 11.3.4 | LVI Trip Selection | 129 |
| 11.4 | LVI Status Register | 129 |
| 11.5 | LVI Interrupts | 129 |
| 11.6 | Low-Power Modes | 130 |
| 11.6.1 | Wait Mode | 130 |
| 11.6.2 | Stop Mode | 130 |

Chapter 12 Input/Output (I/O) Ports

| | | |
|--------|---|-----|
| 12.1 | Introduction | 131 |
| 12.2 | Unused Pin Termination | 131 |
| 12.3 | Port A | 135 |
| 12.3.1 | Port A Data Register | 135 |
| 12.3.2 | Data Direction Register A | 136 |
| 12.3.3 | Port A Input Pullup Enable Register | 137 |
| 12.4 | Port B | 138 |
| 12.4.1 | Port B Data Register | 138 |
| 12.4.2 | Data Direction Register B | 138 |
| 12.5 | Port C | 140 |
| 12.5.1 | Port C Data Register | 140 |
| 12.5.2 | Data Direction Register C | 140 |
| 12.5.3 | Port C Input Pullup Enable Register | 142 |

| | | |
|--------|-------------------------------------|-----|
| 12.6 | Port D | 142 |
| 12.6.1 | Port D Data Register | 142 |
| 12.6.2 | Data Direction Register D | 143 |
| 12.6.3 | Port D Input Pullup Enable Register | 145 |
| 12.7 | Port E | 145 |
| 12.7.1 | Port E Data Register | 145 |
| 12.7.2 | Data Direction Register E | 146 |
| 12.8 | Port F | 147 |
| 12.8.1 | Port F Data Register | 147 |
| 12.8.2 | Data Direction Register F | 148 |
| 12.9 | Port G | 149 |
| 12.9.1 | Port G Data Register | 149 |
| 12.9.2 | Data Direction Register G | 150 |

Chapter 13

Enhanced Serial Communications Interface (ESCI) Module

| | | |
|----------|-------------------------------------|-----|
| 13.1 | Introduction | 151 |
| 13.2 | Features | 151 |
| 13.3 | Pin Name Conventions | 153 |
| 13.4 | Functional Description | 153 |
| 13.4.1 | Data Format | 153 |
| 13.4.2 | Transmitter | 156 |
| 13.4.2.1 | Character Length | 156 |
| 13.4.2.2 | Character Transmission | 156 |
| 13.4.2.3 | Break Characters | 157 |
| 13.4.2.4 | Idle Characters | 158 |
| 13.4.2.5 | Inversion of Transmitted Output | 158 |
| 13.4.2.6 | Transmitter Interrupts | 158 |
| 13.4.3 | Receiver | 158 |
| 13.4.3.1 | Character Length | 159 |
| 13.4.3.2 | Character Reception | 160 |
| 13.4.3.3 | Data Sampling | 160 |
| 13.4.3.4 | Framing Errors | 161 |
| 13.4.3.5 | Baud Rate Tolerance | 161 |
| 13.4.3.6 | Receiver Wakeup | 163 |
| 13.4.3.7 | Receiver Interrupts | 164 |
| 13.4.3.8 | Error Interrupts | 164 |
| 13.5 | Low-Power Modes | 164 |
| 13.5.1 | Wait Mode | 164 |
| 13.5.2 | Stop Mode | 164 |
| 13.6 | ESCI During Break Module Interrupts | 165 |
| 13.7 | I/O Signals | 165 |
| 13.7.1 | PTE0/TxD (Transmit Data) | 165 |
| 13.7.2 | PTE1/RxD (Receive Data) | 165 |
| 13.8 | I/O Registers | 165 |
| 13.8.1 | ESCI Control Register 1 | 166 |
| 13.8.2 | ESCI Control Register 2 | 167 |

Table of Contents

| | | |
|--------|-------------------------------|-----|
| 13.8.3 | ESCI Control Register 3 | 169 |
| 13.8.4 | ESCI Status Register 1 | 170 |
| 13.8.5 | ESCI Status Register 2 | 173 |
| 13.8.6 | ESCI Data Register | 173 |
| 13.8.7 | ESCI Baud Rate Register | 174 |
| 13.8.8 | ESCI Prescaler Register | 175 |
| 13.9 | ESCI Arbiter | 177 |
| 13.9.1 | ESCI Arbiter Control Register | 179 |
| 13.9.2 | ESCI Arbiter Data Register | 180 |
| 13.9.3 | Bit Time Measurement | 180 |
| 13.9.4 | Arbitration Mode | 180 |

Chapter 14 System Integration Module (SIM)

| | | |
|----------|--|-----|
| 14.1 | Introduction | 183 |
| 14.2 | SIM Bus Clock Control and Generation | 186 |
| 14.2.1 | Bus Timing | 186 |
| 14.2.2 | Clock Startup from POR or LVI Reset | 186 |
| 14.2.3 | Clocks in Stop Mode and Wait Mode | 186 |
| 14.3 | Reset and System Initialization | 187 |
| 14.3.1 | External Pin Reset | 187 |
| 14.3.2 | Active Resets from Internal Sources | 187 |
| 14.3.2.1 | Power-On Reset | 188 |
| 14.3.2.2 | Computer Operating Properly (COP) Reset | 188 |
| 14.3.2.3 | Illegal Opcode Reset | 189 |
| 14.3.2.4 | Illegal Address Reset | 189 |
| 14.3.2.5 | Low-Voltage Inhibit (LVI) Reset | 189 |
| 14.3.2.6 | Monitor Mode Entry Module Reset (MODRST) | 189 |
| 14.4 | SIM Counter | 190 |
| 14.4.1 | SIM Counter During Power-On Reset | 190 |
| 14.4.2 | SIM Counter During Stop Mode Recovery | 190 |
| 14.4.3 | SIM Counter and Reset States | 190 |
| 14.5 | Exception Control | 190 |
| 14.5.1 | Interrupts | 190 |
| 14.5.1.1 | Hardware Interrupts | 191 |
| 14.5.1.2 | SWI Instruction | 193 |
| 14.5.1.3 | Interrupt Status Registers | 193 |
| 14.5.2 | Reset | 196 |
| 14.5.3 | Break Interrupts | 196 |
| 14.5.4 | Status Flag Protection in Break Mode | 196 |
| 14.6 | Low-Power Modes | 196 |
| 14.6.1 | Wait Mode | 197 |
| 14.6.2 | Stop Mode | 198 |
| 14.7 | SIM Registers | 199 |
| 14.7.1 | Break Status Register | 199 |
| 14.7.2 | SIM Reset Status Register | 199 |
| 14.7.3 | Break Flag Control Register | 200 |

Chapter 15 Serial Peripheral Interface (SPI) Module

| | | |
|---------|---|-----|
| 15.1 | Introduction | 201 |
| 15.2 | Features | 201 |
| 15.3 | Functional Description | 201 |
| 15.3.1 | Master Mode | 204 |
| 15.3.2 | Slave Mode | 204 |
| 15.4 | Transmission Formats | 205 |
| 15.4.1 | Clock Phase and Polarity Controls | 205 |
| 15.4.2 | Transmission Format When CPHA = 0 | 205 |
| 15.4.3 | Transmission Format When CPHA = 1 | 206 |
| 15.4.4 | Transmission Initiation Latency | 207 |
| 15.5 | Queuing Transmission Data | 209 |
| 15.6 | Error Conditions | 210 |
| 15.6.1 | Overflow Error | 210 |
| 15.6.2 | Mode Fault Error | 212 |
| 15.7 | Interrupts | 213 |
| 15.8 | Resetting the SPI | 214 |
| 15.9 | Low-Power Modes | 214 |
| 15.9.1 | Wait Mode | 214 |
| 15.9.2 | Stop Mode | 215 |
| 15.10 | SPI During Break Interrupts | 215 |
| 15.11 | I/O Signals | 215 |
| 15.11.1 | MISO (Master In/Slave Out) | 215 |
| 15.11.2 | MOSI (Master Out/Slave In) | 215 |
| 15.11.3 | SPSCK (Serial Clock) | 216 |
| 15.11.4 | \overline{SS} (Slave Select) | 216 |
| 15.12 | I/O Registers | 217 |
| 15.12.1 | SPI Control Register | 217 |
| 15.12.2 | SPI Status and Control Register | 218 |
| 15.12.3 | SPI Data Register | 220 |

Chapter 16 Timebase Module (TBM)

| | | |
|--------|---------------------------------|-----|
| 16.1 | Introduction | 221 |
| 16.2 | Features | 221 |
| 16.3 | Functional Description | 221 |
| 16.4 | Interrupts | 221 |
| 16.5 | TBM Interrupt Rate | 222 |
| 16.6 | Low-Power Modes | 223 |
| 16.6.1 | Wait Mode | 223 |
| 16.6.2 | Stop Mode | 223 |
| 16.7 | Timebase Control Register | 224 |

Chapter 17 Timer Interface Module (TIM1)

| | | |
|----------|---|-----|
| 17.1 | Introduction | 225 |
| 17.2 | Features | 225 |
| 17.3 | Functional Description | 225 |
| 17.3.1 | TIM1 Counter Prescaler | 228 |
| 17.3.2 | Input Capture | 228 |
| 17.3.3 | Output Compare | 229 |
| 17.3.3.1 | Unbuffered Output Compare | 229 |
| 17.3.3.2 | Buffered Output Compare | 229 |
| 17.3.4 | Pulse Width Modulation (PWM) | 230 |
| 17.3.4.1 | Unbuffered PWM Signal Generation | 230 |
| 17.3.4.2 | Buffered PWM Signal Generation | 231 |
| 17.3.4.3 | PWM Initialization | 231 |
| 17.4 | Interrupts | 232 |
| 17.5 | Wait Mode | 232 |
| 17.6 | TIM1 During Break Interrupts | 233 |
| 17.7 | Input/Output Signals | 233 |
| 17.8 | Input/Output Registers | 233 |
| 17.8.1 | TIM1 Status and Control Register | 233 |
| 17.8.2 | TIM1 Counter Registers | 235 |
| 17.8.3 | TIM1 Counter Modulo Registers | 236 |
| 17.8.4 | TIM1 Channel Status and Control Registers | 236 |
| 17.8.5 | TIM1 Channel Registers | 239 |

Chapter 18 Timer Interface Module (TIM2)

| | | |
|----------|--|-----|
| 18.1 | Introduction | 241 |
| 18.2 | Features | 241 |
| 18.3 | Functional Description | 241 |
| 18.3.1 | TIM2 Counter Prescaler | 245 |
| 18.3.2 | Input Capture | 246 |
| 18.3.3 | Output Compare | 246 |
| 18.3.3.1 | Unbuffered Output Compare | 246 |
| 18.3.3.2 | Buffered Output Compare | 247 |
| 18.3.4 | Pulse Width Modulation (PWM) | 248 |
| 18.3.4.1 | Unbuffered PWM Signal Generation | 248 |
| 18.3.4.2 | Buffered PWM Signal Generation | 249 |
| 18.3.4.3 | PWM Initialization | 250 |
| 18.4 | Interrupts | 251 |
| 18.5 | Low-Power Modes | 251 |
| 18.5.1 | Wait Mode | 251 |
| 18.5.2 | Stop Mode | 251 |
| 18.6 | TIM2 During Break Interrupts | 251 |

| | | |
|--------|---|-----|
| 18.7 | I/O Signals | 252 |
| 18.7.1 | TIM2 Clock Pin (T2CH0) | 252 |
| 18.7.2 | TIM2 Channel I/O Pins (T2CH5:T2CH2 and T2CH1:T2CH0) | 252 |
| 18.8 | I/O Registers | 252 |
| 18.8.1 | TIM2 Status and Control Register | 252 |
| 18.8.2 | TIM2 Counter Registers | 254 |
| 18.8.3 | TIM2 Counter Modulo Registers | 254 |
| 18.8.4 | TIM2 Channel Status and Control Registers | 255 |
| 18.8.5 | TIM2 Channel Registers | 258 |

Chapter 19 Development Support

| | | |
|----------|---|-----|
| 19.1 | Introduction | 261 |
| 19.2 | Break Module (BRK) | 261 |
| 19.2.1 | Functional Description | 261 |
| 19.2.1.1 | Flag Protection During Break Interrupts | 264 |
| 19.2.1.2 | TIM During Break Interrupts | 264 |
| 19.2.1.3 | COP During Break Interrupts | 264 |
| 19.2.2 | Break Module Registers | 264 |
| 19.2.2.1 | Break Status and Control Register | 265 |
| 19.2.2.2 | Break Address Registers | 265 |
| 19.2.2.3 | Break Status Register | 266 |
| 19.2.2.4 | Break Flag Control Register | 266 |
| 19.2.3 | Low-Power Modes | 266 |
| 19.3 | Monitor Module (MON) | 267 |
| 19.3.1 | Functional Description | 267 |
| 19.3.1.1 | Normal Monitor Mode | 271 |
| 19.3.1.2 | Forced Monitor Mode | 271 |
| 19.3.1.3 | Monitor Vectors | 271 |
| 19.3.1.4 | Data Format | 272 |
| 19.3.1.5 | Break Signal | 272 |
| 19.3.1.6 | Baud Rate | 272 |
| 19.3.1.7 | Commands | 272 |
| 19.3.2 | Security | 276 |

Chapter 20 Electrical Specifications

| | | |
|------|------------------------------------|-----|
| 20.1 | Introduction | 277 |
| 20.2 | Absolute Maximum Ratings | 277 |
| 20.3 | Functional Operating Range | 278 |
| 20.4 | Thermal Characteristics | 278 |
| 20.5 | 5.0-Vdc Electrical Characteristics | 279 |
| 20.6 | 3.3-Vdc Electrical Characteristics | 281 |
| 20.7 | 5.0-Volt Control Timing | 283 |
| 20.8 | 3.3-Volt Control Timing | 283 |

Table of Contents

| | | |
|--------|---|-----|
| 20.9 | Clock Generation Module (CGM) Characteristics | 284 |
| 20.9.1 | CGM Operating Conditions | 284 |
| 20.9.2 | CGM Component Information | 284 |
| 20.9.3 | CGM Acquisition/Lock Time Information | 285 |
| 20.10 | 5.0-Volt ADC Characteristics | 286 |
| 20.11 | 3.3-Volt ADC Characteristics | 287 |
| 20.12 | 5.0-Volt SPI Characteristics | 288 |
| 20.13 | 3.3-Volt SPI Characteristics | 289 |
| 20.14 | Timer Interface Module Characteristics | 292 |
| 20.15 | Memory Characteristics | 293 |

Chapter 21

Ordering Information and Mechanical Specifications

| | | |
|------|--------------------------|-----|
| 21.1 | Introduction | 295 |
| 21.2 | MC Order Numbers | 295 |
| 21.3 | Package Dimensions | 295 |

**Appendix A
MC68HC908GR48A**

| | | |
|-----|----------------------------|-----|
| A.1 | Introduction | 305 |
| A.2 | Block Diagram | 305 |
| A.3 | Memory | 305 |
| A.4 | Ordering Information | 308 |

**Appendix B
MC68HC908GR32A**

| | | |
|-----|----------------------------|-----|
| B.1 | Introduction | 309 |
| B.2 | Block Diagram | 309 |
| B.3 | Memory | 309 |
| B.4 | Ordering Information | 312 |

Chapter 1

General Description

1.1 Introduction

The MC68HC908GR60A, MC68HC908GR48A, and MC68HC908GR32A are members of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

The information contained in this document pertains to all three devices with the exceptions noted in [Appendix A MC68HC908GR48A](#) and [Appendix B MC68HC908GR32A](#).

1.2 Features

For convenience, features have been organized to reflect:

- Standard features
- Features of the CPU08

1.2.1 Standard Features

Features of the MC68HC908GR60A include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- Clock generation module supporting 1-MHz to 8-MHz crystals
- FLASH program memory security⁽¹⁾
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- In-system programming (ISP)
- System protection features:
 - Optional computer operating properly (COP) reset
 - Low-voltage detection with optional reset and selectable trip points for 3.3-V and 5.0-V operation
 - Illegal opcode detection with reset
 - Illegal address detection with reset
- Low-power design; fully static with stop and wait modes
- Standard low-power modes of operation:
 - Wait mode
 - Stop mode

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

General Description

- Master reset pin and power-on reset (POR)
- On-chip FLASH memory:
 - MC68HC908GR60A — 60 Kbytes
 - MC68HC908GR48A — 48 Kbytes
 - MC68HC908GR32A — 32 Kbytes
- Random-access memory (RAM):
 - MC68HC908GR60A — 2048 bytes
 - MC68HC908GR48A — 1536 bytes
 - MC68HC908GR32A — 1536 bytes
- Serial peripheral interface (SPI) module
- Enhanced serial communications interface (ESCI) module
- One 16-bit, 2-channel timer interface module (TIM1) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- One 16-bit, 6-channel timer interface module (TIM2) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- Timebase module with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external crystal
- 24-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- 8-bit keyboard wakeup port with software selectable rising or falling edge detect, as well as high or low level detection
- Up to 53 general-purpose input/output (I/O) pins, including:
 - 40 shared-function I/O pins, depending on package choice
 - Up to 13 dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullups on \overline{IRQ} and \overline{RST} to reduce customer system cost
- High current 10-mA sink/source capability on all port pins
- Higher current 20-mA sink/source capability on PTC0–PTC4 and PTF0–PTF3
- User selectable clockout feature with divide by 1, 2, and 4 of the bus or crystal frequency
- User selection of having the oscillator enabled or disabled during stop mode
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Available packages:
 - 32-pin low-profile quad flat pack (LQFP)
 - 48-pin low-profile quad flat pack (LQFP)
 - 64-pin quad flat pack (QFP)
- Specific features in 32-pin LQFP are:
 - Port A is only 4 bits: PTA0–PTA3; shared with ADC and KBI modules
 - Port B is only 6 bits: PTB0–PTB5; shared with ADC module
 - Port C is only 2 bits: PTC0–PTC1
 - Port D is only 7 bits: PTD0–PTD6; shared with SPI, TIM1 and TIM2 modules
 - Port E is only 2 bits: PTE0–PTE1; shared with ESCI module

- Specific features in 48-pin LQFP are:
 - Port A is 8 bits: PTA0–PTA7; shared with ADC and KBI modules
 - Port B is 8 bits: PTB0–PTB7; shared with ADC module
 - Port C is only 7 bits: PTC0–PTC6
 - Port D is 8 bits: PTD0–PTD7; shared with SPI, TIM1, and TIM2 modules
 - Port E is only 6 bits: PTE0–PTE5; shared with ESCI module
- Specific features in 64-pin QFP are:
 - Port A is 8 bits: PTA0–PTA7; shared with ADC and KBI modules
 - Port B is 8 bits: PTB0–PTB7; shared with ADC module
 - Port C is only 7 bits: PTC0–PTC6
 - Port D is 8 bits: PTD0–PTD7; shared with SPI, TIM1, and TIM2 modules
 - Port E is only 6 bits: PTE0–PTE5; shared with ESCI module
 - Port F is 8 bits: PTF0–PTF7; shared with TIM2 module
 - Port G is 8 bits: PTG0–PTG7; shared with ADC module

1.2.2 Features of the CPU08

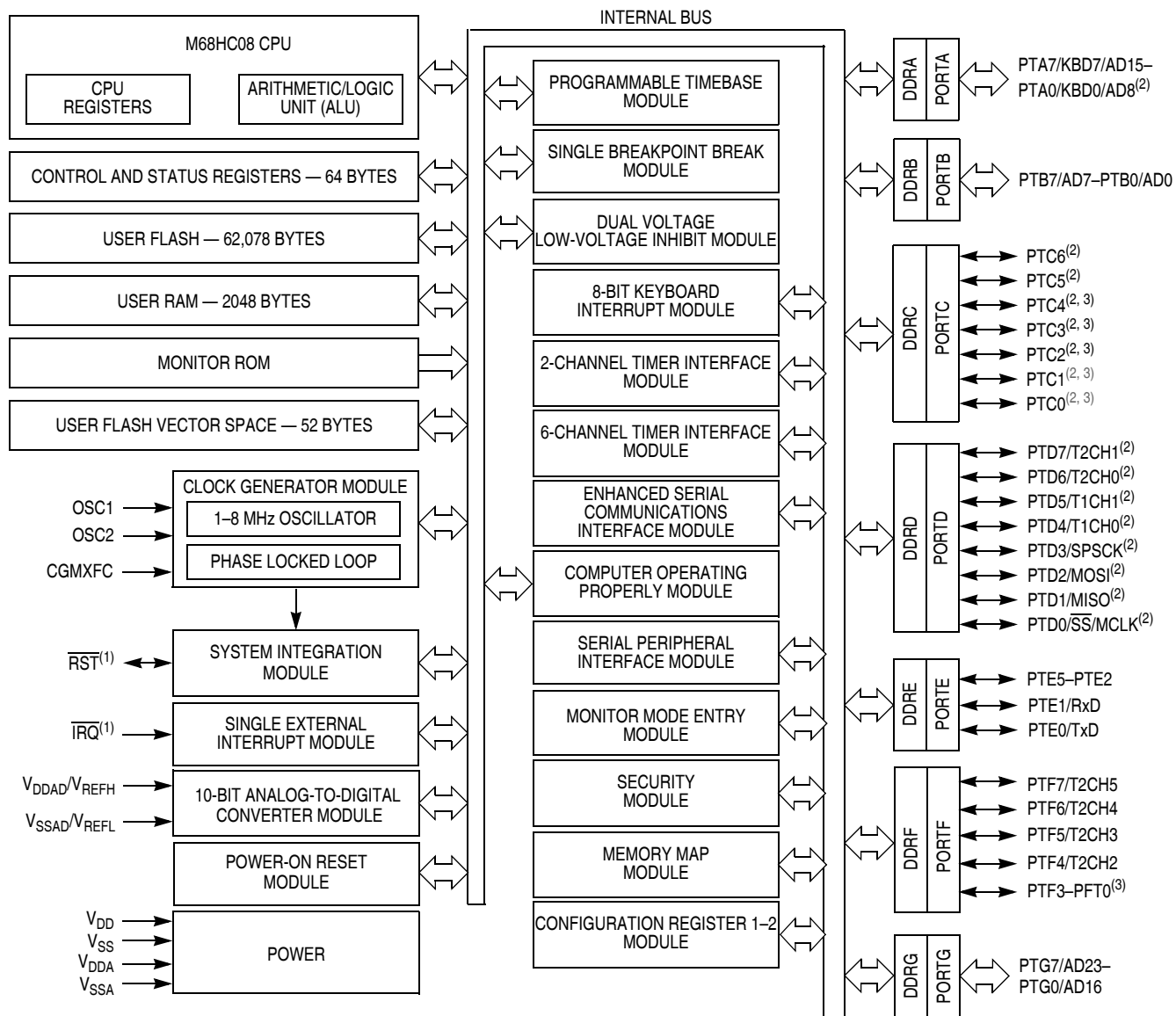
Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8×8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908GR60A. Refer to [Appendix A MC68HC908GR48A](#) and [Appendix B MC68HC908GR32A](#).

General Description



1. Pin contains integrated pullup device.
2. Ports are software configurable with pullup device if input port or pullup/pulldown device for keyboard input.
3. Higher current drive port pins

Figure 1-1. MC68HC908GR60A Block Diagram

1.4 Pin Assignments

Figure 1-2, Figure 1-3, and Figure 1-4 illustrate the pin assignments for the 32-pin LQFP, 48-pin LQFP, and 64-pin QFP respectively.

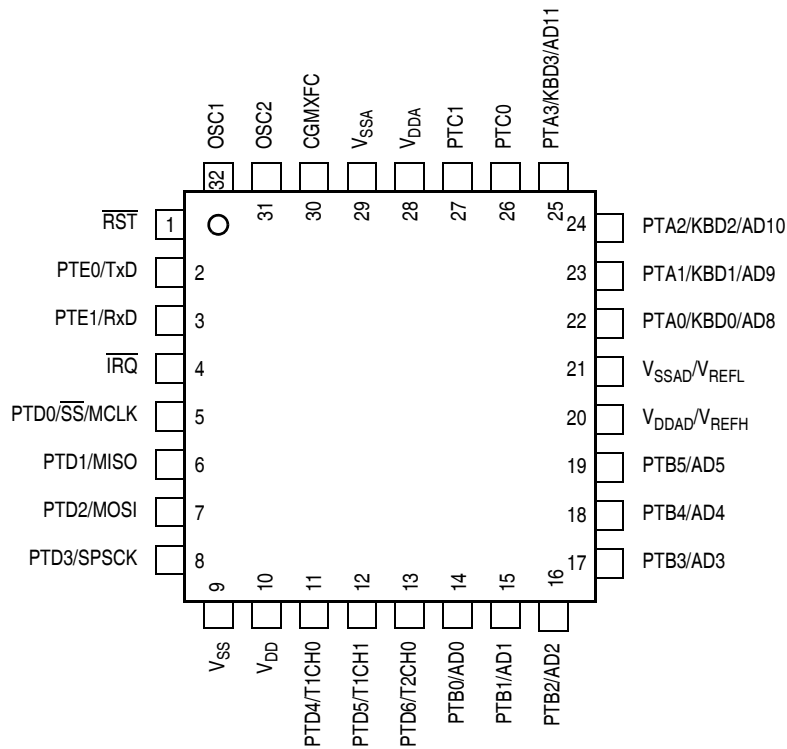


Figure 1-2. 32-Pin LQFP Pin Assignments

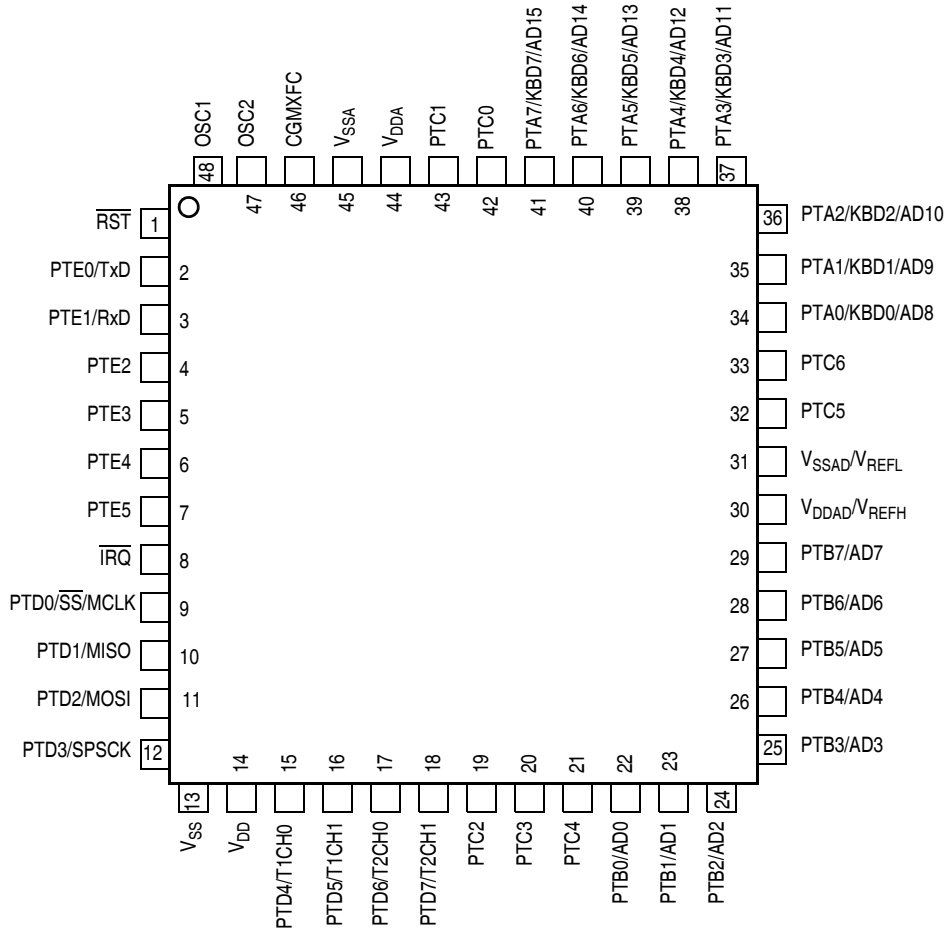


Figure 1-3. 48-Pin LQFP Pin Assignments

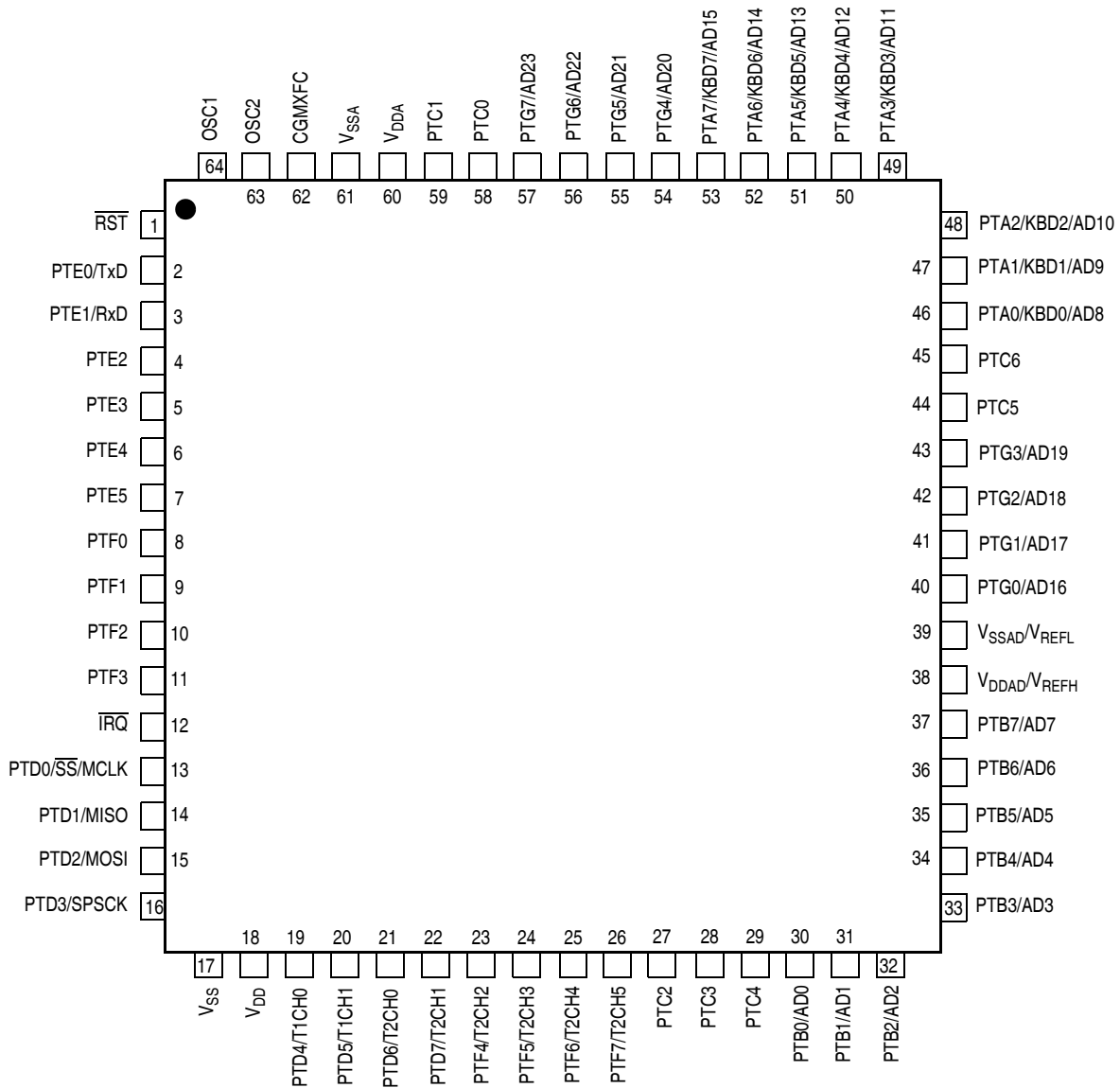


Figure 1-4. 64-Pin QFP Pin Assignments

1.5 Pin Functions

Descriptions of the pin functions are provided here.

1.5.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as [Figure 1-5](#) shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.