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MC68HC908GR60A
MC68HC908GR48A
MC68HC908GR32A

Data Sheet

M68HC08
Microcontrollers

MC68HC908GR60A
Rev. 5
04/2007

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MC68HC908GR60A
MC68HC908GR48A
MC68HC908GR32A

Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
April, 2004	N/A	Initial release	N/A
July, 2004	1	9.7.3 Keyboard Interrupt Polarity Register — Corrected description of KBIP7–KBIP0.	119
June, 2005	2	Table 13-6. ESCI LIN Control Bits — Corrected Functionality definitions	174
		13.9.1 ESCI Arbiter Control Register — Corrected definition for ACLK bit.	179
		13.9.3 Bit Time Measurement — Corrected description of ACLK bit.	180
March, 2006	3	10.5 Clock Generator Module (CGM) — Updated description to remove erroneous information.	122
July, 2006	4	Added 1.5.15 Unused Pin Termination	28
		12.1 Introduction — Replaced note	131
		Table 13-6. ESCI LIN Control Bits — Corrected functionality column.	174
		The following sections were updated to show that a break interrupt inhibits input captures: 17.6 TIM1 During Break Interrupts 18.6 TIM2 During Break Interrupts 19.2.1.2 TIM During Break Interrupts	 233 251 264
		Figure 19-10. Normal Monitor Mode Circuit and Figure 19-11. Forced Monitor Mode — Changed capacitor values	269
		20.5 5.0-Vdc Electrical Characteristics — Updated minimum value for low-voltage inhibit, trip rising voltage (V_{TRIPR}).	279
		20.9.1 CGM Component Specifications — Updated values for feedback bias resistor	284
April, 2007	5	Figure 2-2. Control, Status, and Data Registers — Replaced TBMCLKSEL with TMBCLKSEL to be compatible with development tool nomenclature	33 90
		Chapter 5 Configuration Register (CONFIG) — Replaced COPCLK with CGMXCLK	89 91
		10.6.2 Stop Mode — Replaced COPCLK with CGMXCLK	122
		Figure 13-3. ESCI Module Block Diagram — Changed BUS_CLK to Bus Clock and deleted reference to 4x BUSCLK	154
		13.4.2 Transmitter — Changed ESCIBDSRC to SCIBDSRC	156
		13.9.1 ESCI Arbiter Control Register and 13.9.3 Bit Time Measurement — Replaced one quarter with one half in the definition for ACLK = 1	179 180
		Chapter 16 Timebase Module (TBM) — Replaced TBMCLKSEL with TMBCLKSEL to be compatible with development tool nomenclature	222 223
		20.5 5.0-Vdc Electrical Characteristics and 20.6 3.3-Vdc Electrical Characteristics — Updated tables	279 281
		20.9 Clock Generation Module (CGM) Characteristics — Updated section to include the following: 20.9.1 CGM Operating Conditions 20.9.2 CGM Component Information 20.9.3 CGM Acquisition/Lock Time Information	 284 284 285

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Chapter 1
General Description

1.1 Introduction

The MC68HC908GR60A, MC68HC908GR48A, and MC68HC908GR32A are members of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

The information contained in this document pertains to all three devices with the exceptions noted in Appendix A MC68HC908GR48A and Appendix B MC68HC908GR32A.

1.2 Features

For convenience, features have been organized to reflect:

- Standard features
- Features of the CPU08

1.2.1 Standard Features

Features of the MC68HC908GR60A include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- Clock generation module supporting 1-MHz to 8-MHz crystals
- FLASH program memory security[1]
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- In-system programming (ISP)
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with optional reset and selectable trip points for 3.3-V and 5.0-V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Low-power design; fully static with stop and wait modes
- Standard low-power modes of operation:
  - Wait mode
  - Stop mode

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

- Master reset pin and power-on reset (POR)
- On-chip FLASH memory:
  - MC68HC908GR60A — 60 Kbytes
  - MC68HC908GR48A — 48 Kbytes
  - MC68HC908GR32A — 32 Kbytes
- Random-access memory (RAM):
  - MC68HC908GR60A — 2048 bytes
  - MC68HC908GR48A — 1536 bytes
  - MC68HC908GR32A — 1536 bytes
- Serial peripheral interface (SPI) module
- Enhanced serial communications interface (ESCI) module
- One 16-bit, 2-channel timer interface module (TIM1) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- One 16-bit, 6-channel timer interface module (TIM2) with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- Timebase module with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external crystal
- 24-channel, 10-bit successive approximation analog-to-digital converter (ADC)
- 8-bit keyboard wakeup port with software selectable rising or falling edge detect, as well as high or low level detection
- Up to 53 general-purpose input/output (I/O) pins, including:
  - 40 shared-function I/O pins, depending on package choice
  - Up to 13 dedicated I/O pins, depending on package choice
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce customer system cost
- High current 10-mA sink/source capability on all port pins
- Higher current 20-mA sink/source capability on PTC0–PTC4 and PTF0–PTF3
- User selectable clockout feature with divide by 1, 2, and 4 of the bus or crystal frequency
- User selection of having the oscillator enabled or disabled during stop mode
- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging
- Available packages:
  - 32-pin low-profile quad flat pack (LQFP)
  - 48-pin low-profile quad flat pack (LQFP)
  - 64-pin quad flat pack (QFP)
- Specific features in 32-pin LQFP are:
  - Port A is only 4 bits: PTA0–PTA3; shared with ADC and KBI modules
  - Port B is only 6 bits: PTB0–PTB5; shared with ADC module
  - Port C is only 2 bits: PTC0–PTC1
  - Port D is only 7 bits: PTD0–PTD6; shared with SPI, TIM1 and TIM2 modules
  - Port E is only 2 bits: PTE0–PTE1; shared with ESCI module

- Specific features in 48-pin LQFP are:
  - Port A is 8 bits: PTA0–PTA7; shared with ADC and KBI modules
  - Port B is 8 bits: PTB0–PTB7; shared with ADC module
  - Port C is only 7 bits: PTC0–PTC6
  - Port D is 8 bits: PTD0–PTD7; shared with SPI, TIM1, and TIM2 modules
  - Port E is only 6 bits: PTE0–PTE5; shared with ESCI module
- Specific features in 64-pin QFP are:
  - Port A is 8 bits: PTA0–PTA7; shared with ADC and KBI modules
  - Port B is 8 bits: PTB0–PTB7; shared with ADC module
  - Port C is only 7 bits: PTC0–PTC6
  - Port D is 8 bits: PTD0–PTD7; shared with SPI, TIM1, andTIM2 modules
  - Port E is only 6 bits: PTE0–PTE5; shared with ESCI module
  - Port F is 8 bits: PTF0–PTF7; shared with TIM2 module
  - Port G is 8 bits; PTG0–PTG7; shared with ADC module

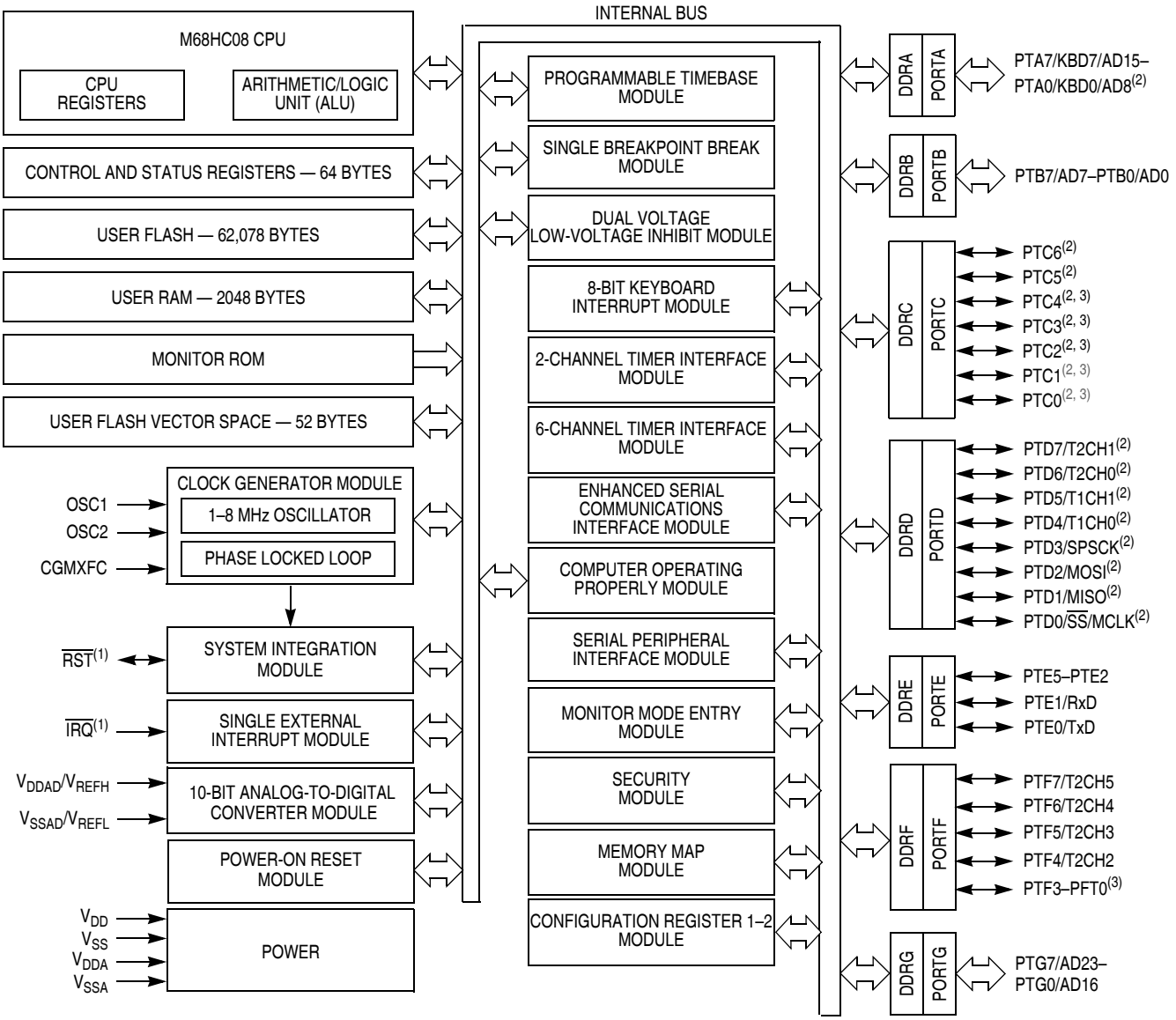
1.2.2 Features of the CPU08

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908GR60A. Refer to Appendix A MC68HC908GR48A and Appendix B MC68HC908GR32A.



1. Pin contains integrated pullup device.
2. Ports are software configurable with pullup device if input port or pullup/pulldown device for keyboard input.
3. Higher current drive port pins

Figure 1-1. MC68HC908GR60A Block Diagram

1.4 Pin Assignments

Figure 1-2, Figure 1-3, and Figure 1-4 illustrate the pin assignments for the 32-pin LQFP, 48-pin LQFP, and 64-pin QFP respectively.

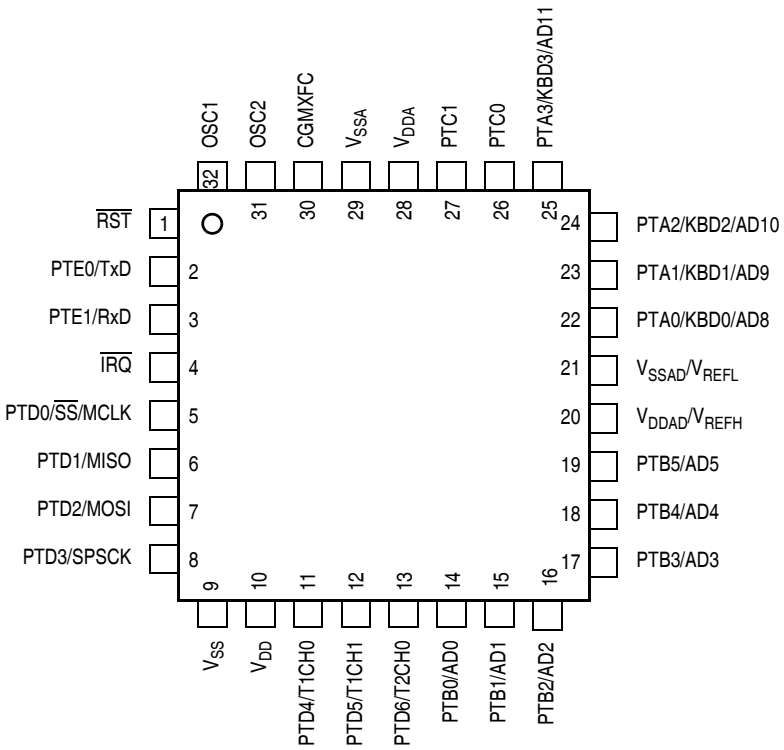


Figure 1-2. 32-Pin LQFP Pin Assignments

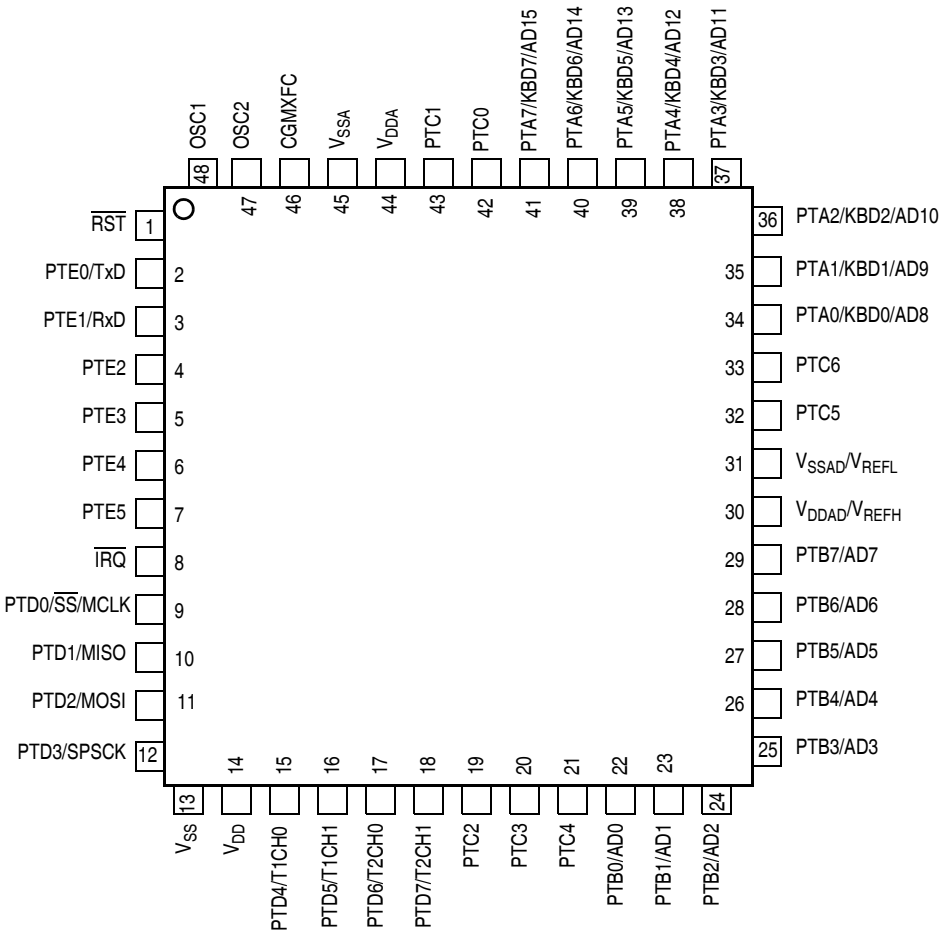


Figure 1-3. 48-Pin LQFP Pin Assignments

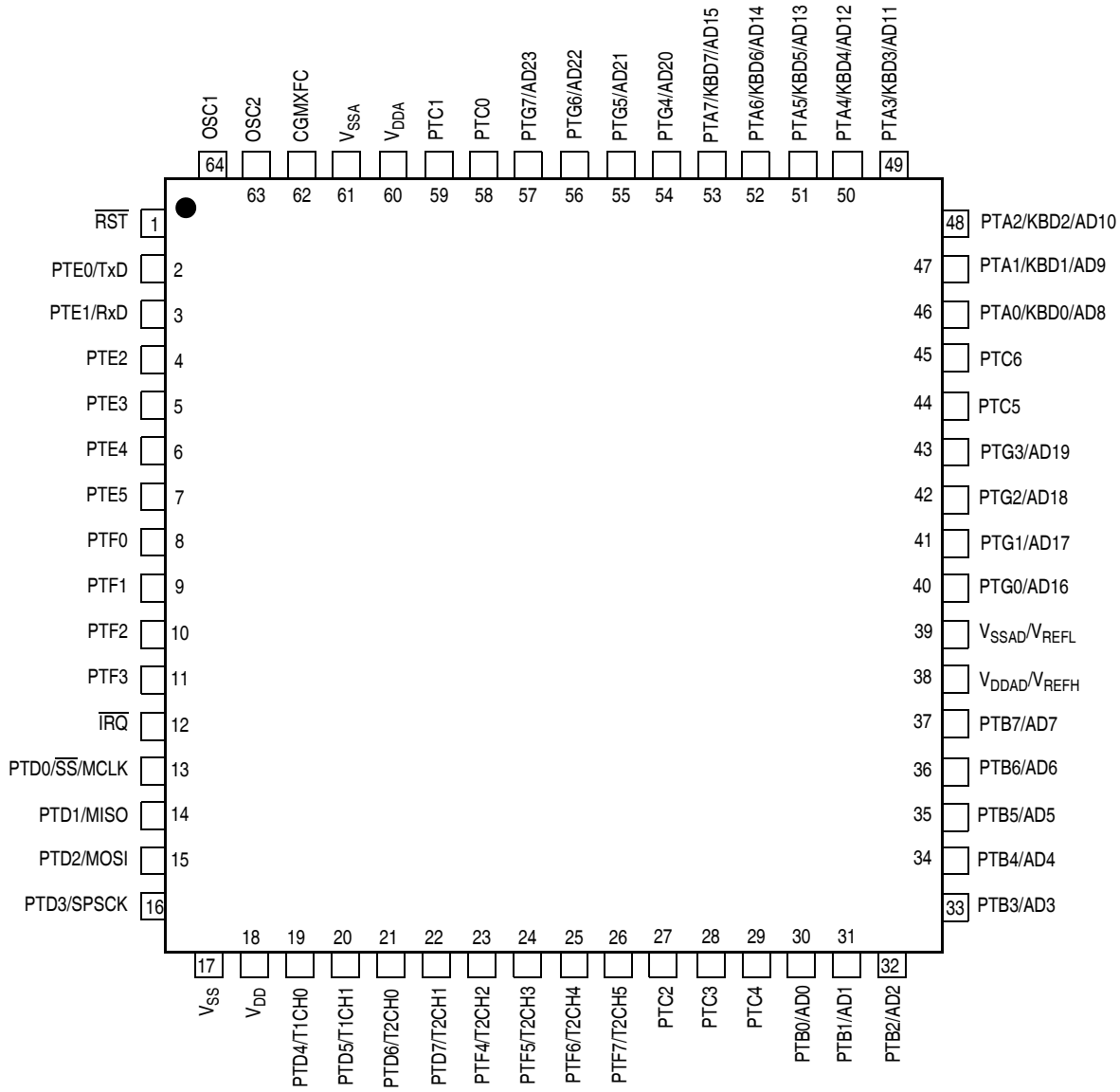


Figure 1-4. 64-Pin QFP Pin Assignments

1.5 Pin Functions

Descriptions of the pin functions are provided here.

1.5.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as Figure 1-5 shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.