



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





Freescale Semiconductor, Inc.

*MC68HC908GR8
MC68HC908GR4*

Technical Data

*M68HC08
Microcontrollers*

*MC68HC908GR8/D
Rev. 4, 6/2002*

WWW.MOTOROLA.COM/SEMICONDUCTORS

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.


**For More Information On This Product,
Go to: www.freescale.com**

MC68HC908GR8

MC68HC908GR4

Technical Data — Rev 4.0

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Motorola and  are registered trademarks of Motorola, Inc.
DigitalDNA is a trademark of Motorola, Inc.

© Motorola, Inc., 2002

MC68HC908GR8 — Rev 4.0

Technical Data

MOTOROLA

3

**For More Information On This Product,
Go to: www.freescale.com**



List of Paragraphs

List of Paragraphs	5
Table of Contents	7
List of Tables	17
List of Figures	19
Section 1. General Description	25
Section 2. Memory Map	35
Section 3. Low Power Modes	49
Section 4. Resets and Interrupts	61
Section 5. Analog-to-Digital Converter (ADC)	79
Section 6. Break Module (BRK)	91
Section 7. Clock Generator Module (CGMC)	99
Section 8. Configuration Register (CONFIG)	129
Section 9. Computer Operating Properly (COP)	133
Section 10. Central Processing Unit (CPU)	139
Section 11. Flash Memory	157
Section 12. External Interrupt (IRQ)	167
Section 13. Keyboard Interrupt (KBI)	175
Section 14. Low-Voltage Inhibit (LVI)	183
Section 15. Monitor ROM (MON)	189
Section 16. Input/Output Ports (I/O)	205

Section 17. RAM229
Section 18. Serial Communications Interface (SCI) . . .231
Section 19. System Integration Module (SIM)271
Section 20. Serial Peripheral Interface (SPI)297
Section 21. Timebase Module (TBM)329
Section 22. Timer Interface Module (TIM)335
Section 23. Electrical Specifications361
Section 24. Mechanical Specifications387
Section 25. Ordering Information391
Glossary395
Revision History405

Table of Contents

List of Paragraphs

Table of Contents

List of Tables

List of Figures

Section 1. General Description

1.1	Contents	25
1.2	Introduction	25
1.3	Features	26
1.4	MCU Block Diagram	28
1.5	Pin Assignments	30
1.6	Pin Functions	31

Section 2. Memory Map

2.1	Contents	35
2.2	Introduction	35
2.3	Unimplemented Memory Locations	35
2.4	Reserved Memory Locations	36
2.5	Input/Output (I/O) Section	36

Section 3. Low Power Modes

3.1 Contents49

3.2 Introduction49

3.3 Analog-to-Digital Converter (ADC)50

3.4 Break Module (BRK)51

3.5 Central Processor Unit (CPU)51

3.6 Clock Generator Module (CGM)52

3.7 Computer Operating Properly Module (COP)52

3.8 External Interrupt Module (IRQ)53

3.9 Keyboard Interrupt Module (KBI)53

3.10 Low-Voltage Inhibit Module (LVI)54

3.11 Serial Communications Interface Module (SCI)54

3.12 Serial Peripheral Interface Module (SPI)55

3.13 Timer Interface Module (TIM1 and TIM2)55

3.14 Timebase Module (TBM)56

3.15 Exiting Wait Mode57

3.16 Exiting Stop Mode58

Section 4. Resets and Interrupts

4.1 Contents61

4.2 Introduction61

4.3 Resets61

4.4 Interrupts66

Section 5. Analog-to-Digital Converter (ADC)

5.1 Contents79

5.2 Introduction79

5.3 Features80

5.4 Functional Description80

5.5 Interrupts.....83

5.6 Low-Power Modes83

5.7 I/O Signals83

5.8 I/O Registers.....85

Section 6. Break Module (BRK)

6.1 Contents91

6.2 Introduction.....91

6.3 Features91

6.4 Functional Description92

6.5 Low-Power Modes94

6.6 Break Module Registers94

Section 7. Clock Generator Module (CGMC)

7.1 Contents99

7.2 Introduction.....99

7.3 Features100

7.4 Functional Description100

7.5 I/O Signals112

7.6 CGMC Registers.....114

7.7 Interrupts.....123

7.8 Special Modes123

7.9 Acquisition/Lock Time Specifications125

Section 8. Configuration Register (CONFIG)

8.1 Contents 129
 8.2 Introduction 129
 8.3 Functional Description 129

Section 9. Computer Operating Properly (COP)

9.1 Contents 133
 9.2 Introduction 133
 9.3 Functional Description 133
 9.4 I/O Signals 135
 9.5 COP Control Register 136
 9.6 Interrupts 136
 9.7 Monitor Mode 137
 9.8 Low-Power Modes 137
 9.9 COP Module During Break Mode 137

Section 10. Central Processing Unit (CPU)

10.1 Contents 139
 10.2 Introduction 139
 10.3 Features 139
 10.4 CPU registers 140
 10.5 Arithmetic/logic unit (ALU) 145
 10.6 Low-power modes 145
 10.7 CPU during break interrupts 146
 10.8 Instruction Set Summary 147
 10.9 Opcode Map 154

Section 11. Flash Memory

11.1 Contents157
11.2 Introduction157
11.3 Functional Description157
11.4 FLASH Control Register159
11.5 FLASH Page Erase Operation160
11.6 FLASH Mass Erase Operation161
11.7 FLASH Program/Read Operation162
11.8 FLASH Block Protection163
11.9 Wait Mode166
11.10 STOP Mode166

Section 12. External Interrupt (IRQ)

12.1 Contents167
12.2 Introduction167
12.3 Features167
12.4 Functional Description168
12.5 $\overline{\text{IRQ1}}$ Pin170
12.6 IRQ Module During Break Interrupts171
12.7 IRQ Status and Control Register172

Section 13. Keyboard Interrupt (KBI)

13.1 Contents175
13.2 Introduction175
13.3 Features175
13.4 Functional Description176
13.5 Keyboard Initialization179

13.6 Low-Power Modes180
 13.7 Keyboard Module During Break Interrupts180
 13.8 I/O Registers.....181

Section 14. Low-Voltage Inhibit (LVI)

14.1 Contents183
 14.2 Introduction.....183
 14.3 Features183
 14.4 Functional Description184
 14.5 LVI Status Register.....187
 14.6 LVI Interrupts188
 14.7 Low-Power Modes188

Section 15. Monitor ROM (MON)

15.1 Contents189
 15.2 Introduction.....189
 15.3 Features189
 15.4 Functional Description190
 15.5 Security.....202

Section 16. Input/Output Ports (I/O)

16.1 Contents205
 16.2 Introduction.....205
 16.3 Port A209
 16.4 Port B213
 16.5 Port C216
 16.6 Port D220

16.7 Port E225

Section 17. RAM

17.1 Contents229
 17.2 Introduction229
 17.3 Functional Description229

Section 18. Serial Communications Interface (SCI)

18.1 Contents231
 18.2 Introduction231
 18.3 Features232
 18.4 Pin Name Conventions233
 18.5 Functional Description233
 18.6 Low-Power Modes250
 18.7 SCI During Break Module Interrupts251
 18.8 I/O Signals251
 18.9 I/O Registers252

Section 19. System Integration Module (SIM)

19.1 Contents271
 19.2 Introduction271
 19.3 SIM Bus Clock Control and Generation275
 19.4 Reset and System Initialization276
 19.5 SIM Counter281
 19.6 Exception Control282
 19.7 Low-Power Modes290
 19.8 SIM Registers293

Section 20. Serial Peripheral Interface (SPI)

20.1 Contents297

20.2 Introduction297

20.3 Features298

20.4 Pin Name Conventions and I/O Register Addresses298

20.5 Functional Description299

20.6 Transmission Formats303

20.7 Queuing Transmission Data309

20.8 Error Conditions310

20.9 Interrupts314

20.10 Resetting the SPI316

20.11 Low-Power Modes317

20.12 SPI During Break Interrupts318

20.13 I/O Signals318

20.14 I/O Registers322

Section 21. Timebase Module (TBM)

21.1 Contents329

21.2 Introduction329

21.3 Features329

21.4 Functional Description330

21.5 Timebase Register Description331

21.6 Interrupts332

21.7 Low-Power Modes333

Section 22. Timer Interface Module (TIM)

22.1 Contents335

22.2 Introduction335

22.3 Features336

22.4 Pin Name Conventions336

22.5 Functional Description337

22.6 Interrupts346

22.7 Low-Power Modes347

22.8 TIM During Break Interrupts348

22.9 I/O Signals348

22.10 I/O Registers349

Section 23. Electrical Specifications

23.1 Contents361

23.2 Absolute Maximum Ratings362

23.3 Functional Operating Range363

23.4 Thermal Characteristics363

23.5 5.0 V DC Electrical Characteristics364

23.6 3.0 V DC Electrical Characteristics366

23.7 5.0 V Control Timing368

23.8 3.0 V Control Timing369

23.9 Output High-Voltage Characteristics370

23.10 Output Low-Voltage Characteristics373

23.11 Typical Supply Currents376

23.12 ADC Characteristics378

23.13 5.0 V SPI Characteristics379

23.14 3.0 V SPI Characteristics380

23.15 Timer Interface Module Characteristics383

23.16 Clock Generation Module Characteristics383
23.17 Memory Characteristics385

Section 24. Mechanical Specifications

24.1 Contents387
24.2 Introduction387
24.3 32-Pin LQFP (Case #873A)388
24.4 28-Pin PDIP (Case #710)389
24.5 28-Pin SOIC (Case #751F)390

Section 25. Ordering Information

25.1 Contents391
25.2 Introduction391
25.3 MC Order Numbers392
25.4 Development Tools393

Glossary

Revision History

Contents405
Introduction405
Changes from Rev 3.0 published in February 2002 to Rev 4.0
published in June 2002405
Changes from Rev 2.0 published in January 2002 to Rev 3.0 pub-
lished in February 2002406
Changes from Rev 1.0 published in April 2001 to Rev 2.0 pub-
lished in December 2001406

List of Tables

Table	Title	Page
2-1	Vector Addresses	47
4-1	Interrupt Sources	70
4-2	Interrupt Source Flags	75
5-1	Mux Channel Select	86
5-2	ADC Clock Divide Ratio	88
7-1	Numeric Example	109
7-2	PRE 1 and PRE0 Programming	117
7-3	VPR1 and VPR0 Programming	117
10-1	Instruction Set Summary	147
10-2	Opcode Map	155
11-1	Examples of protect start address:	166
14-1	LVIOUT Bit Indication	187
15-1	Monitor Mode Signal Requirements and Options	193
15-2	Mode Differences	196
15-3	Monitor Baud Rate Selection	197
15-4	READ (Read Memory) Command	199
15-5	WRITE (Write Memory) Command	199
15-6	IREAD (Indexed Read) Command	200
15-7	IWRITE (Indexed Write) Command	200
15-8	READSP (Read Stack Pointer) Command	201
15-9	RUN (Run User Program) Command	201
16-1	Port Control Register Bits Summary	208
16-2	Port A Pin Functions	211
16-3	Port B Pin Functions	215
16-4	Port C Pin Functions	218
16-5	Port D Pin Functions	223
16-6	Port E Pin Functions	227
18-1	Pin Name Conventions	233
18-2	Start Bit Verification	244

List of Tables

18-3 Data Bit Recovery 244

18-4 Stop Bit Recovery 245

18-5 Character Format Selection 255

18-6 SCI Baud Rate Prescaling 266

18-7 SCI Baud Rate Selection 266

18-8 SCI Baud Rate Selection Examples 268

19-1 Signal Name Conventions 273

19-2 PIN Bit Set Timing 277

19-3 Interrupt Sources 286

19-4 SIM Registers 293

20-1 Pin Name Conventions 299

20-2 SPI Interrupts 314

20-3 SPI Configuration 321

20-4 SPI Master Baud Rate Selection 327

21-1 Timebase Rate Selection for OSC1 = 32.768 kHz 331

22-1 Pin Name Conventions 336

22-2 Prescaler Selection 351

22-3 Mode, Edge, and Level Selection 358

23-1 Absolute Maximum Ratings 362

23-2 Functional Operation Range 363

23-3 Thermal Characteristics 363

23-4 5.0V DC Electrical Characteristics 364

23-5 3.0 V DC Electrical Characteristics 366

23-6 5.0 V Control Timing 368

23-7 3.0 V Control Timing 369

23-8 Timer Interface Module Characteristics 383

23-9 CGM Component Specifications 383

25-1 MC Order Numbers 392

25-2 Development Tool Kits 393

25-3 Development Tool Components 393

List of Figures

Figure	Title	Page
1-1	MCU Block Diagram	29
1-2	QFP Pin Assignments	30
1-3	DIP And SOIC Pin Assignments	31
1-4	Power Supply Bypassing	32
2-1	Memory Map	37
2-2	Control, Status, and Data Registers	39
4-1	Internal Reset Timing	62
4-2	Power-On Reset Recovery	63
4-3	SIM Reset Status Register (SRSR)	65
4-4	Interrupt Stacking Order	67
4-5	Interrupt Recognition Example	68
4-6	Interrupt Processing	69
4-7	Interrupt Status Register 1 (INT1)	76
4-8	Interrupt Status Register 2 (INT2)	76
4-9	Interrupt Status Register 3 (INT3)	77
5-1	ADC Block Diagram	81
5-2	ADC Status and Control Register (ADSCR)	85
5-3	ADC Data Register (ADR)	87
5-4	ADC Clock Register (ADCLK)	88
6-1	Break Module Block Diagram	92
6-2	I/O Register Summary	93
6-3	Break Status and Control Register (BRKSCR)	95
6-4	Break Address Register High (BRKH)	96
6-5	Break Address Register Low (BRKL)	96
6-6	SIM Break Status Register (SBSR)	96
6-7	SIM Break Flag Control Register (SBFCR)	98
7-1	CGMC Block Diagram	101
7-2	CGMC External Connections	111
7-3	CGMC I/O Register Summary	114

List of Figures

7-4 PLL Control Register (PCTL)115

7-5 PLL Bandwidth Control Register (PBWC)118

7-6 PLL Multiplier Select Register High (PMSH)119

7-7 PLL Multiplier Select Register Low (PMSL)120

7-8 PLL VCO Range Select Register (PMRS)121

7-9 PLL Reference Divider Select Register (PMDS)122

7-10 PLL Filter127

8-1 Configuration Register 2 (CONFIG2)130

8-2 Configuration Register 1 (CONFIG1)130

9-1 COP Block Diagram134

9-2 COP Control Register (COPCTL)136

10-1 CPU registers140

10-2 Accumulator (A)141

10-3 Index register (H:X)141

10-4 Stack pointer (SP)142

10-5 Program counter (PC)143

10-6 Condition code register (CCR)143

11-1 FLASH Control Register (FLCR)159

11-2 FLASH Programming Flowchart164

11-3 FLASH Block Protect Register (FLBPR)165

11-4 FLASH Block Protect Start Address165

12-1 IRQ Module Block Diagram169

12-2 IRQ I/O Register Summary169

12-3 IRQ Status and Control Register (INTSCR)172

13-1 Keyboard Module Block Diagram177

13-2 I/O Register Summary177

13-3 Keyboard Status and Control Register (INTKBSCR)181

13-4 Keyboard Interrupt Enable Register (INTKBIER)182

14-1 LVI Module Block Diagram185

14-2 LVI I/O Register Summary186

14-3 LVI Status Register (LVISR)187

15-1 Monitor Mode Circuit191

15-2 Low-Voltage Monitor Mode Entry Flowchart195

15-3 Monitor Data Format196

15-4 Break Transaction196

15-5 Read Transaction198

15-6 Write Transaction198

15-7 Stack Pointer at Monitor Mode Entry202

15-8	Monitor Mode Entry Timing	203
16-1	I/O Port Register Summary	206
16-2	Port A Data Register (PTA)	209
16-3	Data Direction Register A (DDRA)	210
16-4	Port A I/O Circuit	211
16-5	Port A Input Pullup Enable Register (PTAPUE)	212
16-6	Port B Data Register (PTB)	213
16-7	Data Direction Register B (DDRB)	214
16-8	Port B I/O Circuit	215
16-9	Port C Data Register (PTC)	216
16-10	Data Direction Register C (DDRC)	217
16-11	Port C I/O Circuit	218
16-12	Port C Input Pullup Enable Register (PTCPUE)	219
16-13	Port D Data Register (PTD)	220
16-14	Data Direction Register D (DDRD)	222
16-15	Port D I/O Circuit	223
16-16	Port D Input Pullup Enable Register (PTDPUE)	224
16-17	Port E Data Register (PTE)	225
16-18	Data Direction Register E (DDRE)	226
16-19	Port E I/O Circuit	227
18-1	SCI Module Block Diagram	234
18-2	SCI I/O Register Summary	235
18-3	SCI Data Formats	236
18-4	SCI Transmitter	237
18-5	SCI Receiver Block Diagram	242
18-6	Receiver Data Sampling	243
18-7	Slow Data	246
18-8	Fast Data	247
18-9	SCI Control Register 1 (SCC1)	253
18-10	SCI Control Register 2 (SCC2)	256
18-11	SCI Control Register 3 (SCC3)	258
18-12	SCI Status Register 1 (SCS1)	260
18-13	Flag Clearing Sequence	263
18-14	SCI Status Register 2 (SCS2)	264
18-15	SCI Data Register (SCDR)	265
18-16	SCI Baud Rate Register (SCBR)	265
19-1	SIM Block Diagram	272
19-2	SIM I/O Register Summary	274

List of Figures

19-3 CGM Clock Signals275

19-4 External Reset Timing277

19-5 Internal Reset Timing278

19-6 Sources of Internal Reset278

19-7 POR Recovery279

19-8 Interrupt Entry Timing283

19-9 Interrupt Recovery Timing283

19-10 Interrupt Processing284

19-11 Interrupt Recognition Example285

19-12 Interrupt Status Register 1 (INT1)288

19-13 Interrupt Status Register 2 (INT2)288

19-14 Interrupt Status Register 3 (INT3)289

19-15 Wait Mode Entry Timing291

19-16 Wait Recovery from Interrupt or Break291

19-17 Wait Recovery from Internal Reset292

19-18 Stop Mode Entry Timing293

19-19 Stop Mode Recovery from Interrupt or Break293

19-20 SIM Break Status Register (SBSR)294

19-21 SIM Reset Status Register (SRSR)295

19-22 SIM Break Flag Control Register (SBFCR)296

20-1 SPI I/O Register Summary299

20-2 SPI Module Block Diagram300

20-3 Full-Duplex Master-Slave Connections301

20-4 Transmission Format (CPHA = 0)305

20-5 CPHA/ \overline{SS} Timing305

20-6 Transmission Format (CPHA = 1)306

20-7 Transmission Start Delay (Master)308

20-8 .SPRF/SPTE CPU Interrupt Timing309

20-9 Missed Read of Overflow Condition311

20-10 Clearing SPRF When OVRF Interrupt Is Not Enabled312

20-11 SPI Interrupt Request Generation315

20-12 CPHA/ \overline{SS} Timing320

20-13 SPI Control Register (SPCR)322

20-14 SPI Status and Control Register (SPSCR)325

20-15 SPI Data Register (SPDR)328

21-1 Timebase Block Diagram330

21-2 Timebase Control Register (TBCR)331

22-1 TIM Block Diagram338

22-2	TIM I/O Register Summary	339
22-3	PWM Period and Pulse Width	343
22-4	TIM Status and Control Register (TSC)	349
22-5	TIM Counter Registers High (TCNTH)	352
22-6	TIM Counter Registers Low (TCNTL)	352
22-7	TIM Counter Modulo Register High (TMODH)	353
22-8	TIM Counter Modulo Register Low (TMODL)	353
22-9	TIM Counter Register High (TCNTH)	354
22-10	TIM Counter Register Low (TCNTL)	354
22-11	TIM Channel 0 Status and Control Register (TSC0)	355
22-12	TIM Channel 1 Status and Control Register (TSC1)	355
22-13	CHxMAX Latency	359
22-14	TIM Channel 0 Register High (TCH0H)	360
22-15	TIM Channel 0 Register Low (TCH0L)	360
22-16	TIM Channel 1 Register High (TCH1H)	360
22-17	TIM Channel 1 Register Low (TCH1L)	360
23-1	Typical High-Side Driver Characteristics – Port PTA3–PTA0 ($V_{DD} = 4.5$ Vdc)	370
23-2	Typical High-Side Driver Characteristics – Port PTA3–PTA0 ($V_{DD} = 2.7$ Vdc)	370
23-3	Typical High-Side Driver Characteristics – Port PTC1–PTC0 ($V_{DD} = 4.5$ Vdc)	371
23-4	Typical High-Side Driver Characteristics – Port PTC1–PTC0 ($V_{DD} = 2.7$ Vdc)	371
23-5	Typical High-Side Driver Characteristics – Ports PTB5–PTB0, PTD6–PTD0, and PTE1–PTE0 ($V_{DD} = 5.5$ Vdc)	372
23-6	Typical High-Side Driver Characteristics – Ports PTB5–PTB0, PTD6–PTD0, and PTE1–PTE0 ($V_{DD} = 2.7$ Vdc)	372
23-7	Typical Low-Side Driver Characteristics – Port PTA3–PTA0 ($V_{DD} = 5.5$ Vdc)	373
23-8	Typical Low-Side Driver Characteristics – Port PTA3–PTA0 ($V_{DD} = 2.7$ Vdc)	373
23-9	Typical Low-Side Driver Characteristics – Port PTC1–PTC0 ($V_{DD} = 4.5$ Vdc)	374
23-10	Typical Low-Side Driver Characteristics – Port PTC1–PTC0 ($V_{DD} = 2.7$ Vdc)	374
23-11	Typical Low-Side Driver Characteristics – Ports PTB5–PTB0, PTD6–PTD0, and PTE1–PTE0 ($V_{DD} = 5.5$ Vdc)	375

List of Figures

23-12 Typical Low-Side Driver Characteristics – Ports PTB5–PTB0, PTD6–PTD0, and PTE1–PTE0 ($V_{DD} = 2.7 \text{ Vdc}$)375

23-13 Typical Operating I_{DD} , with All Modules Turned On (–40 °C to 125 °C)376

23-14 Typical Wait Mode I_{DD} , with all Modules Disabled (–40 °C to 125 °C)376

23-15 Typical Stop Mode I_{DD} , with all Modules Disabled (–40 °C to 125 °C)377

23-16 SPI Master Timing381

23-17 SPI Slave Timing382

Section 1. General Description

1.1 Contents

1.2	Introduction	25
1.3	Features	26
1.4	MCU Block Diagram	28
1.5	Pin Assignments	30
1.6	Pin Functions	31

1.2 Introduction

The MC68HC908GR8 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

This document also describes the MC68HC908GR4. The MC68HC908GR4 is a device identical to the MC68HC908GR8 except that it has less Flash memory. Only when there are differences from the MC68HC908GR8 is the MC68HC908GR4 specifically mentioned in the text.