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MC68HC908GR8A
MC68HC908GR4A

Data Sheet

M68HC08
Microcontrollers

MC68HC908GR8A
Rev. 5
04/2007

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MC68HC908GR8A
MC68HC908GR4A
Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
April, 2003	0	Initial release	N/A
October, 2004	1	Module construction and style updated to meet current publications standards.	Throughout
		IRQ1 changed to IRQ	Throughout
		Mask option register changed to configuration register	Throughout
		Deleted references to DMA module and bits	Throughout
		FLASH memory operation details updated	40—42
		3.3.4 Conversion — Clarified ADC details	50
		3.7.1 ADC Status and Control Register — Corrected COCO bit functionality	51
		Table 4-1. Numeric Example — Corrected and improved examples	61
		Table 4-4. Example Filter Component Values — Added more values	73
		Chapter 5 Configuration Register (CONFIG) — Updated COP timeout selections	75, 76
		6.2 Functional Description — Updated block diagram and timeout values	79, 80
		Table 7-1. Instruction Set Summary — Corrected STOP and added WAIT instruction	92, 93
		8.3 Functional Description — Updated IRQ description	95
		8.4 IRQ Pin — Updated IRQ description	97
		Chapter 12 Input/Output (I/O) Ports — Corrected Figures 12-4, 12-11, 12-15	118, 123, 126
		Figure 13-3. SCI Module Block Diagram — Corrected diagram	134
		Figure 13-5. SCI Transmitter — Updated diagram	136
		Figure 13-6. SCI Receiver Block Diagram — Updated Diagram	139
		Chapter 14 System Integration Module (SIM) — Clarified SIM features and functionality	157—173
		16.3 Functional Description — Updated TBM description	195
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		Chapter 18 Development Support — Combined Break and Monitor Mode modules	215—230
		18.2.1 Functional Description — Corrected Break description	215
		18.3 Monitor Module (MON) — Reworked for clarity	221
		19.5 5.0 V DC Electrical Characteristics — Changed V_{TST} max to 8.5 V	233
		19.6 3.0 V DC Electrical Characteristics — Changed V_{TST} max to 8.5 V	234
		19.15.1 CGM Component Specifications — Corrected and updated values	247
		19.15.2 CGM Electrical Specifications — Corrected and updated values	247
		19.17 Memory Characteristics — Updated memory characteristics table	248

Revision History

Date	Revision Level	Description	Page Number(s)
October, 2004	2	19.17 Memory Characteristics — Corrected values for FLASH read bus clock frequency.	248
June, 2005	3	19.2 Absolute Maximum Ratings — Corrected value for supply voltage	229
		19.5 5.0 V DC Electrical Characteristics — Corrected stop IDD and I/O ports Hi-Z leakage current values.	231
		19.6 3.0 V DC Electrical Characteristics — Corrected stop IDD and I/O ports Hi-Z leakage current values.	232
		20.3 Package Dimensions — Updated package information.	247
March, 2006	4	10.5 Clock Generator Module (CGM) — Updated description to remove erroneous information.	106
April, 2007	5	Chapter 5 Configuration Register (CONFIG) — Replaced COPCLK with CGMXCLK and corrected what set and cleared indicate for bit CONFIG1_COPRS	75
		10.6.2 Stop Mode — Replaced COPCLK with CGMXCLK	107

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Chapter 1
General Description

1.1 Introduction

The MC68HC908GR8A is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

This document also describes the MC68HC908GR4A. The MC68HC908GR4A is a device identical to the MC68HC908GR8A except that it has less FLASH memory. Only when there are differences from the MC68HC908GR8A is the MC68HC908GR4A specifically mentioned in the text.

1.2 Features

For convenience, features have been organized to reflect:

- Standard features
- Features of the CPU08

1.2.1 Standard Features

Features include:

- High-performance M68HC08 architecture optimized for C-compilers
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- Clock generation module supporting 1-MHz to 8-MHz crystals
- FLASH program memory security[1]
- On-chip programming firmware for use with host personal computer which does not require high voltage for entry
- In-system programming (ISP)
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with optional reset and selectable trip points for 3.0-V and 5.0-V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Low-power design; fully static with stop and wait modes
- Standard low-power modes of operation:
  - Wait mode
  - Stop mode

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

- Master reset pin and power-on reset (POR)
- 7680 bytes of on-chip FLASH memory on the MC68HC908GR8A and 4096 byes of on-chip FLASH memory on the MC68HC908GR4A with in-circuit programming capabilities of FLASH program memory.
- 384 bytes of on-chip random-access memory (RAM)
- 544 bytes of FLASH programming routines read-only memory (ROM)
- Serial peripheral interface (SPI) module
- Serial communications interface (SCI) module
- One 16-bit, 2-channel timer (TIM1) and one 16-bit, 1-channel timer (TIM2) interface modules with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel
- Up to 6-channel, 8-bit successive approximation analog-to-digital converter (ADC) depending on package choice
- BREAK (BRK) module to allow single breakpoint setting during in-circuit debugging
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce system cost
- Up to 21 general-purpose input/output (I/O) pins
- Selectable pullups on inputs only on ports A, C, and D. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- High current 10-mA sink/source capability on all port pins
- Higher current 15-mA sink/source capability on PTC0–PTC1
- Timebase module (TBM) with clock prescaler circuitry for eight user selectable periodic real-time interrupts with optional active clock source during stop mode for periodic wakeup from stop using an external crystal
- User selection of having the oscillator enabled or disabled during stop mode
- 4-bit keyboard wakeup port
- Available packages:
  - 32-pin low-profile quad flat pack (LQFP)
  - 28-pin plastic dual in-line package (DIP)
  - 28-pin small outline integrated circuit (SOIC)
- Specific features of the MC68HC908GR8A in 28-pin DIP and 28-pin SOIC are:
  - Port B is only 4 bits: PTB0–PTB3; 4-channel ADC module
  - No port C bits

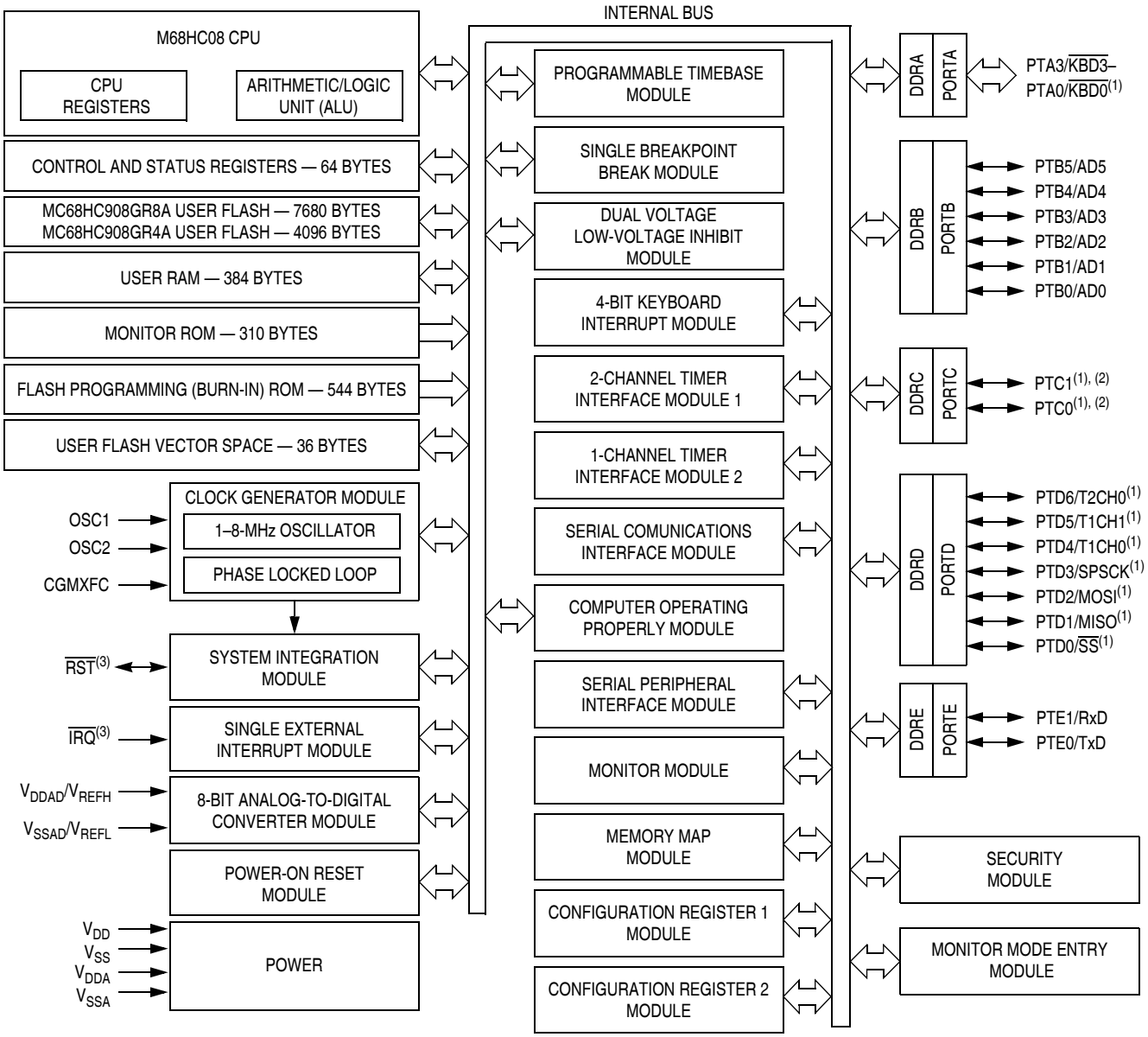
1.2.2 Features of the CPU08

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908GR8A.



1. Ports are software configurable with pullup device if input port.
2. Higher current drive port pins
3. Pin contains integrated pullup device

Figure 1-1. MCU Block Diagram

1.4 Pin Assignments

Figure 1-2 illustrations the pin assignments for the 32-pin LQFP. Figure 1-3 illustrate the pin assignments for the 28-pin DIP and 28-pin SOIC.

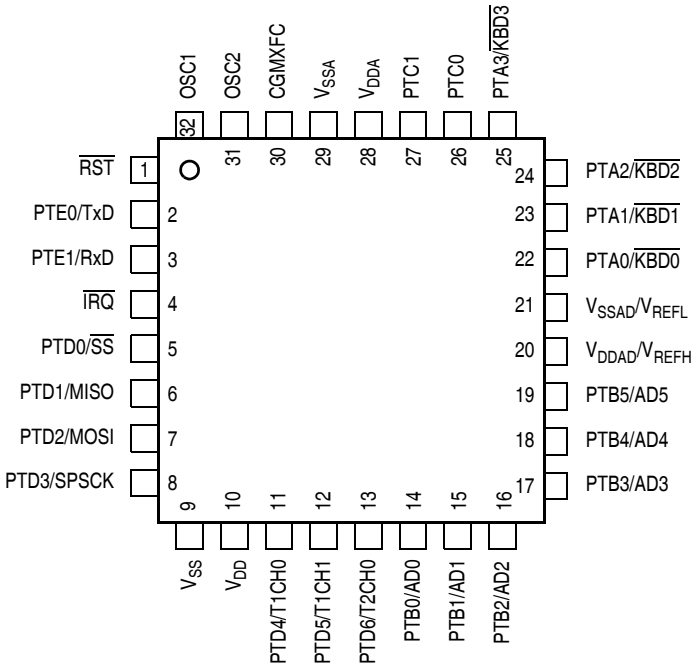
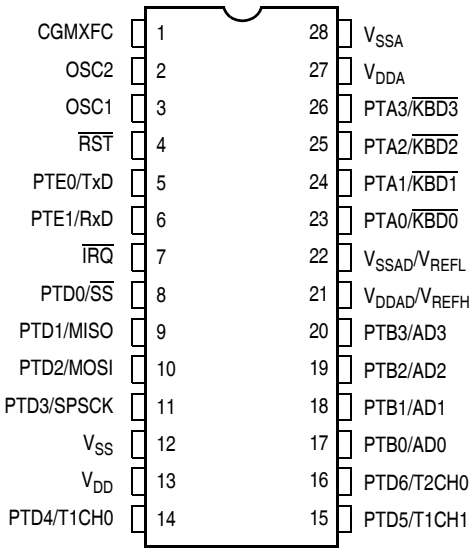


Figure 1-2. 32-Pin LQFP Pin Assignments



NOTE: Ports PTB4, PTB5, PTC0, and PTC1 are available only with the LQFP.

Figure 1-3. 28-Pin DIP and SOIC Pin Assignments

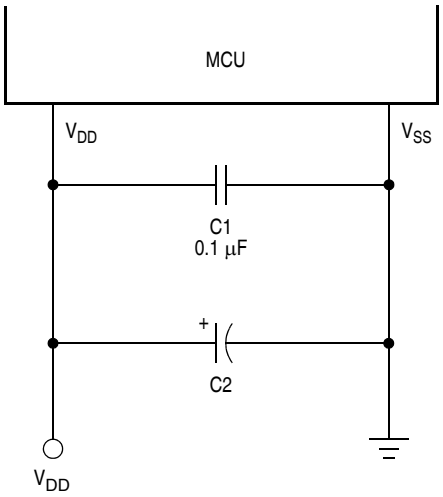
1.5 Pin Functions

Descriptions of the pin functions are provided here.

1.5.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as Figure 1-4 shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.



Note: Component values shown represent typical applications.

Figure 1-4. Power Supply Bypassing

1.5.2 Oscillator Pins (OSC1 and OSC2)

OSC1 and OSC2 are the connections for an external crystal, resonator, or clock circuit. See Chapter 4 Clock Generator Module (CGM).

1.5.3 External Reset Pin ($\overline{RST}$)

A 0 on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor. See Chapter 14 System Integration Module (SIM).

1.5.4 External Interrupt Pin ($\overline{IRQ}$)

$\overline{IRQ}$ is an asynchronous external interrupt pin. This pin contains an internal pullup resistor. See Chapter 8 External Interrupt (IRQ).

1.5.5 CGM Power Supply Pins (V_{DDA} and V_{SSA})

V_{DDA} and V_{SSA} are the power supply pins for the analog portion of the clock generator module (CGM). Decoupling of these pins should be as per the digital supply. See Chapter 4 Clock Generator Module (CGM).

1.5.6 External Filter Capacitor Pin (V_{CGMXFC})

CGMXFC is an external filter capacitor connection for the CGM. See Chapter 4 Clock Generator Module (CGM).

1.5.7 ADC Power Supply/Reference Pins (V_{DDAD}/V_{REFH} and V_{SSAD}/V_{REFL})

V_{DDAD} and V_{SSAD} are the power supply pins to the analog-to-digital converter (ADC). V_{REFH} and V_{REFL} are the reference voltage pins for the ADC. V_{REFH} is the high reference supply for the ADC, and by default the V_{DDAD}/V_{REFH} pin should be externally filtered and connected to the same voltage potential as V_{DD}. V_{REFL} is the low reference supply for the ADC, and by default the V_{SSAD}/V_{REFL} pin should be connected to the same voltage potential as V_{SS}. See Chapter 3 Analog-to-Digital Converter (ADC).

1.5.8 Port A Input/Output (I/O) Pins (PTA3/$\overline{\text{KBD3}}$–PTA0/$\overline{\text{KBD0}}$)

PTA3–PTA0 are special-function, bidirectional I/O port pins. Any or all of the port A pins can be programmed to serve as keyboard interrupt pins. See Chapter 12 Input/Output (I/O) Ports and Chapter 9 Keyboard Interrupt Module (KBI).

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.9 Port B I/O Pins (PTB5/AD5–PTB0/AD0)

PTB5–PTB0 are special-function, bidirectional I/O port pins that can also be used for analog-to-digital converter (ADC) inputs. See Chapter 12 Input/Output (I/O) Ports and Chapter 3 Analog-to-Digital Converter (ADC).

1.5.10 Port C I/O Pins (PTC1 and PTC0)

PTC1 and PTC0 are general-purpose, bidirectional I/O port pins. PTC1–PTC0 are only available on the 32-pin LQFP package. See Chapter 12 Input/Output (I/O) Ports.

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.11 Port D I/O Pins (PTD6/T2CH0–PTD0/$\overline{\text{SS}}$)

PTD6–PTD0 are special-function, bidirectional I/O port pins. PTD3–PTD0 can be programmed to be serial peripheral interface (SPI) pins, while PTD6–PTD4 can be individually programmed to be timer interface module (TIM1 and TIM2) pins. See Chapter 17 Timer Interface Module (TIM1 and TIM2), Chapter 15 Serial Peripheral Interface (SPI) Module, and Chapter 12 Input/Output (I/O) Ports.

These port pins also have selectable pullups when configured for input mode. The pullups are disengaged when configured for output mode. The pullups are selectable on an individual port bit basis.

1.5.12 Port E I/O Pins (PTE1/RxD and PTE0/TxD)

PTE1 and PTE0 are special-function, bidirectional I/O port pins. These pins can also be programmed to be serial communications interface (SCI) pins. See Chapter 13 Serial Communications Interface (SCI) Module and Chapter 12 Input/Output (I/O) Ports.

NOTE

Any unused inputs and I/O ports should be tied to an appropriate logic level (either V_{DD} or V_{SS}). Although the I/O ports of the MC68HC908GR8A do not require termination, termination is recommended to reduce the possibility of static damage.