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MC68HC908JL3/JK3E/JK1E
MC68HRC908JL3/JK3E/JK1E
MC68HLC908JL3/JK3E/JK1E
MC68HC903KL3E/KK3E
MC68HC08JL3E/JK3E
MC68HRC08JL3E/JK3E

Data Sheet

M68HC08
Microcontrollers

MC68HC908JL3E
Rev. 4
10/2006

freescale.com

MC68HC908JL3/JK3E/JK1E
MC68HRC908JL3/JK3E/JK1E
MC68HLC908JL3/JK3E/JK1E
MC68HC908KL3E/KK3E
MC68HC08JL3E/JK3E
MC68HRC08JL3E/JK3E

Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
October 2006	4	Table 4-1. Instruction Set Summary — Updated table to include the WAIT instruction.	42
		5.7.1 Break Status Register (BSR) — Updated for clarity.	63
		5.7.2 Reset Status Register (RSR) — Updated description for clarity.	64
		7.4 Security — Updated to reflect the correct RAM location (\$80) to determine if the security code has been entered correctly.	80
		8.9.1 TIM Status and Control Register (TSC) — Added note to definition of TSTOP bit.	89
		10.1 Introduction — Added note regarding 20-pin devices.	103
		15.4.3 Break Status Register — Updated for clarity.	132
		Chapter 17 Mechanical Specifications — Updated package drawings to the latest available.	147
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Chapter 1

General Description

1.1 Introduction

The MC68H(R)C908JL3E is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

A list of MC68H(R)C908JL3E device variations is shown in [Table 1-1](#).

Table 1-1. Summary of Device Variations

Device Type	Operating Voltage	LVI	ADC	Oscillator Option	Memory	Pin Count	Device
Flash	3V, 5V	Yes	Yes	XTAL	4,096 bytes Flash	28	MC68HC908JL3E
						20	MC68HC908JK3E
					20	MC68HC908JK1E	
				RC	4,096 bytes Flash	28	MC68HRC908JL3E
						20	MC68HRC908JK3E
					20	MC68HRC908JK1E	
Low Voltage Flash ⁽¹⁾	2.2 to 5.5V	No	Yes	XTAL	4,096 bytes Flash	28	MC68HLC908JL3E
						20	MC68HLC908JK3E
					20	MC68HLC908JK1E	
ROM ⁽²⁾	3V, 5V	Yes	Yes	XTAL	4,096 bytes ROM	28	MC68HC08JL3E
						20	MC68HC08JK3E
				RC		28	MC68HRC08JL3E
						20	MC68HRC08JK3E
Flash, ADC-less ⁽³⁾	3V, 5V	Yes	No	XTAL	4,096 bytes Flash	28	MC68HC908KL3E
						20	MC68HC908KK3E

1. Low-voltage Flash devices are documented in [Appendix A MC68HLC908JL3E/JK3E/JK1E](#).

2. ROM devices are documented in [Appendix B MC68H\(R\)C08JL3E/JK3E](#).

3. Flash, ADC-less devices are documented in [Appendix C MC68HC908KL3E/KK3E](#).

All references to the MC68H(R)C908JL3E in this data book apply equally to the MC68H(R)C908JK3E and MC68H(R)C908JK1E, unless otherwise stated.

1.2 Features

Features of the MC68H(R)C908JL3E include the following:

- EMC enhanced version of MC68H(R)C908JL3/JK3/JK1
- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- Low-power design; fully static with stop and wait modes
- Maximum internal bus frequency:
 - 8-MHz at 5V operating voltage
 - 4-MHz at 3V operating voltage
- Oscillator options:
 - Crystal oscillator for MC68HC908JL3E/JK3E/JK1E
 - RC oscillator for MC68HRC908JL3E/JK3E/JK1E
- User program Flash memory with security⁽¹⁾ feature
 - 4,096 bytes for MC68H(R)C908JL3E/JK3E
 - 1,536 bytes for MC68H(R)C908JK1E
- 128 bytes of on-chip RAM
- 2-channel, 16-bit timer interface module (TIM)
- 12-channel, 8-bit analog-to-digital converter (ADC)
- 23 general purpose I/O ports for MC68H(R)C908JL3E:
 - 7 keyboard interrupt with internal pull-up
(6 keyboard interrupt for MC68HC908JL3E)
 - 10 LED drivers (sink)
 - 2 × 25mA open-drain I/O with pull-up
- 15 general purpose I/O ports for MC68H(R)C908JK3E/JK1E:
 - 1 keyboard interrupt with internal pull-up
(MC68HRC908JK3E/JK1E only)
 - 4 LED drivers (sink)
 - 2 × 25mA open-drain I/O with pull-up
 - 10-channel ADC
- System protection features:
 - Optional computer operating properly (COP) reset
 - Optional low-voltage detection with reset and selectable trip points for 3V and 5V operation
 - Illegal opcode detection with reset
 - Illegal address detection with reset
- Master reset pin with internal pull-up and power-on reset
- $\overline{\text{IRQ}}$ with schmitt-trigger input and programmable pull-up
- 28-pin PDIP, 28-pin SOIC, and 48-pin LQFP packages for MC68H(R)C908JL3E
- 20-pin PDIP and 20-pin SOIC packages for MC68H(R)C908JK3E/JK1E

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the Flash difficult for unauthorized users.

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68H(R)C908JL3E.

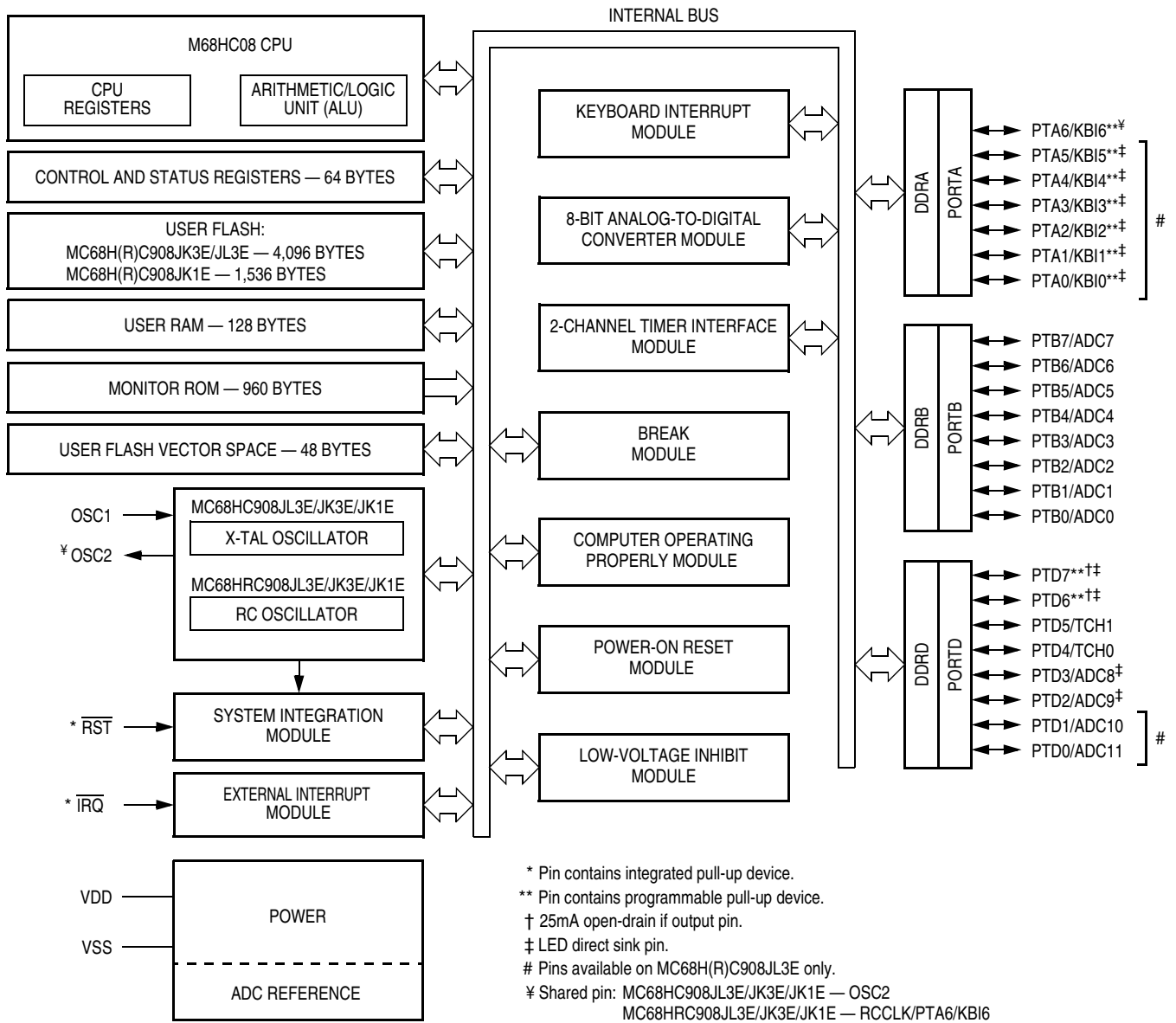
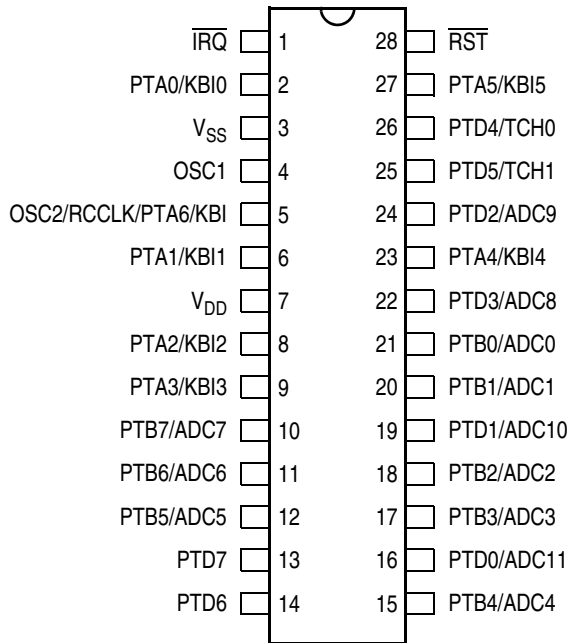


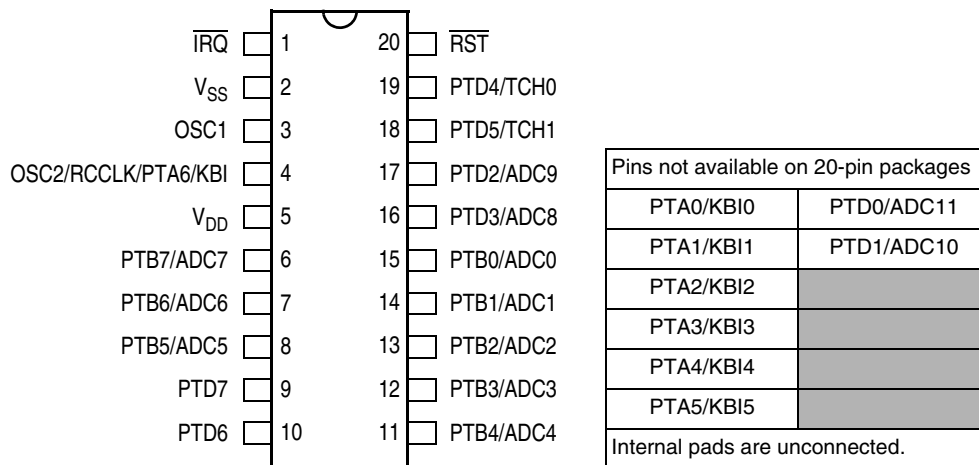
Figure 1-1. MCU Block Diagram

1.4 Pin Assignments



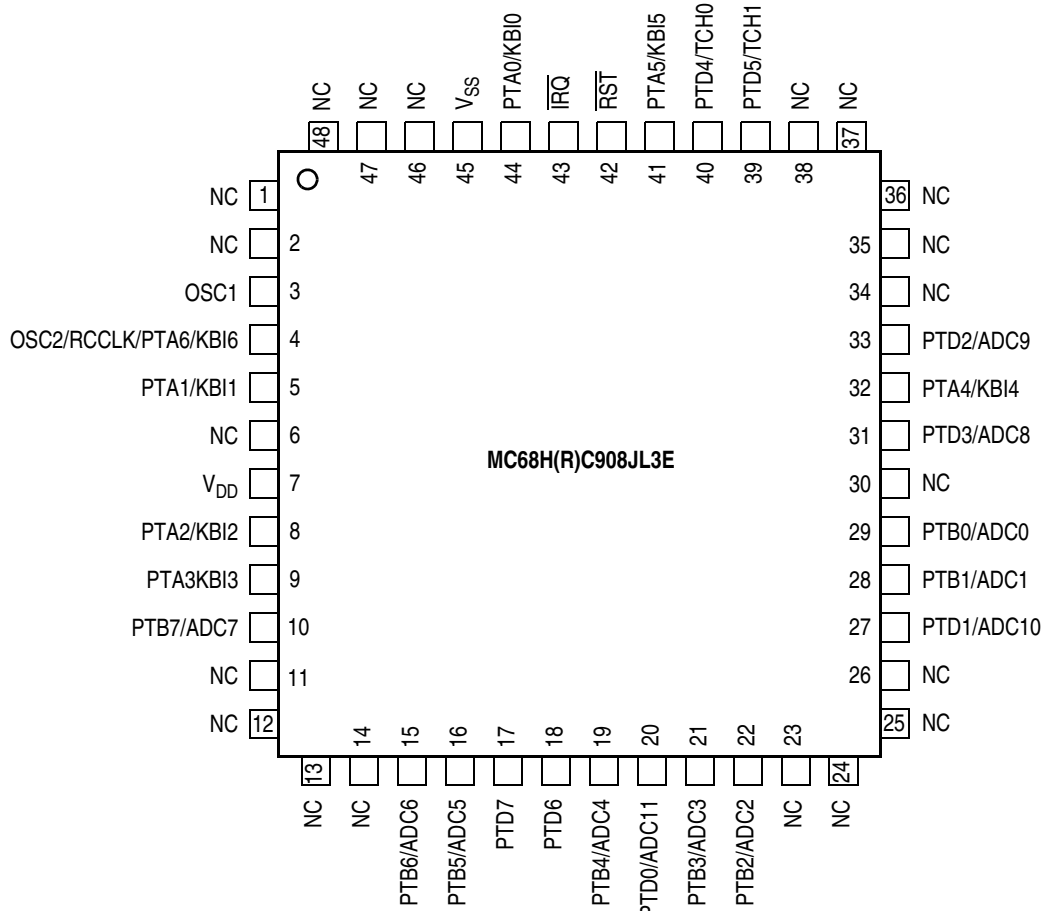
MC68H(R)C908JL3E

Figure 1-2. 28-Pin PDIP/SOIC Pin Assignment



MC68H(R)C908JK3E/JK1E

Figure 1-3. 20-Pin PDIP/SOIC Pin Assignment



NC: No connection

Figure 1-4. 48-Pin LQFP Pin Assignment

1.5 Pin Functions

Description of the pin functions are provided in [Table 1-2](#).

Table 1-2. Pin Functions

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
$V_{DDJL3JL3}$	Power supply.	In	5V or 3V
V_{SS}	Power supply ground	Out	0V
\overline{RST}	RESET input, active low. With Internal pull-up and Schmitt trigger input.	Input	V_{DD} to V_{TST}
\overline{IRQ}	External IRQ pin. With software programmable internal pull-up and schmitt trigger input. This pin is also used for mode entry selection.	Input	V_{DD} to V_{TST}
OSC1	X-tal or RC oscillator input.	In	Analog
OSC2	MC68HC908JL3E/JK3E/JK1E: X-tal oscillator output, this is the inverting OSC1 signal.	Out	Analog
	MC68HRC908JL3E/JK3E/JK1E: Default is RC oscillator clock output, RCCLK. Shared with PTA6/KBI6, with programmable pull-up.	In/Out	V_{DD}
PTA[0:6]	7-bit general purpose I/O port.	In/Out	V_{DD}
	Shared with 7 keyboard interrupts KBI[0:6].	In	V_{DD}
	Each pin has programmable internal pull-up device.	In	V_{DD}
	PTA[0:5] have LED direct sink capability	In	V_{SS}
PTB[0:7]	8-bit general purpose I/O port.	In/Out	V_{DD}
	Shared with 8 ADC inputs, ADC[0:7].	In	Analog
PTD[0:7]	8-bit general purpose I/O port.	In/Out	V_{DD}
	PTD[3:0] shared with 4 ADC inputs, ADC[8:11].	Input	Analog
	PTD[4:5] shared with TIM channels, TCH0 and TCH1.	In/Out	V_{DD}
	PTD[2:3], PTD[6:7] have LED direct sink capability	In	V_{SS}
	PTD[6:7] can be configured as 25mA open-drain output with pull-up.	In/Out	V_{DD}

NOTE

On the MC68H(R)C908JK3E/JK1E, the following pins are not available: PTA0, PTA1, PTA2, PTA3, PTA4, PTA5, PTD0, and PTD1.

Chapter 2

Memory

2.1 Introduction

The CPU08 can address 64 Kbytes of memory space. The memory map, shown in [Figure 2-1](#), includes:

- 4,096 bytes of user Flash — MC68H(R)C908JL3E/JK3E
- 1,536 bytes of user Flash — MC68H(R)C908JK1E
- 128 bytes of RAM
- 48 bytes of user-defined vectors
- 960 bytes of Monitor ROM

2.2 I/O Section

Addresses \$0000–\$003F, shown in [Figure 2-2](#), contain most of the control, status, and data registers. Additional I/O registers have the following addresses:

- \$FE00; Break Status Register, BSR
- \$FE01; Reset Status Register, RSR
- \$FE03; Break Flag Control Register, BFCR
- \$FE04; Interrupt Status Register 1, INT1
- \$FE05; Interrupt Status Register 2, INT2
- \$FE06; Interrupt Status Register 3, INT3
- \$FE08; Flash Control Register, FLCR
- \$FE09; Flash Block Protect Register, FLBPR
- \$FE0C; Break Address Register High, BRKH
- \$FE0D; Break Address Register Low, BRKL
- \$FE0E; Break Status and Control Register, BRKSCR
- \$FFFF; COP Control Register, COPCTL

2.3 Monitor ROM

The 960 bytes at addresses \$FC00–\$FDFF and \$FE10–\$FFCF are reserved ROM addresses that contain the instructions for the monitor functions. (See [Chapter 7 Monitor ROM \(MON\)](#).)

Memory

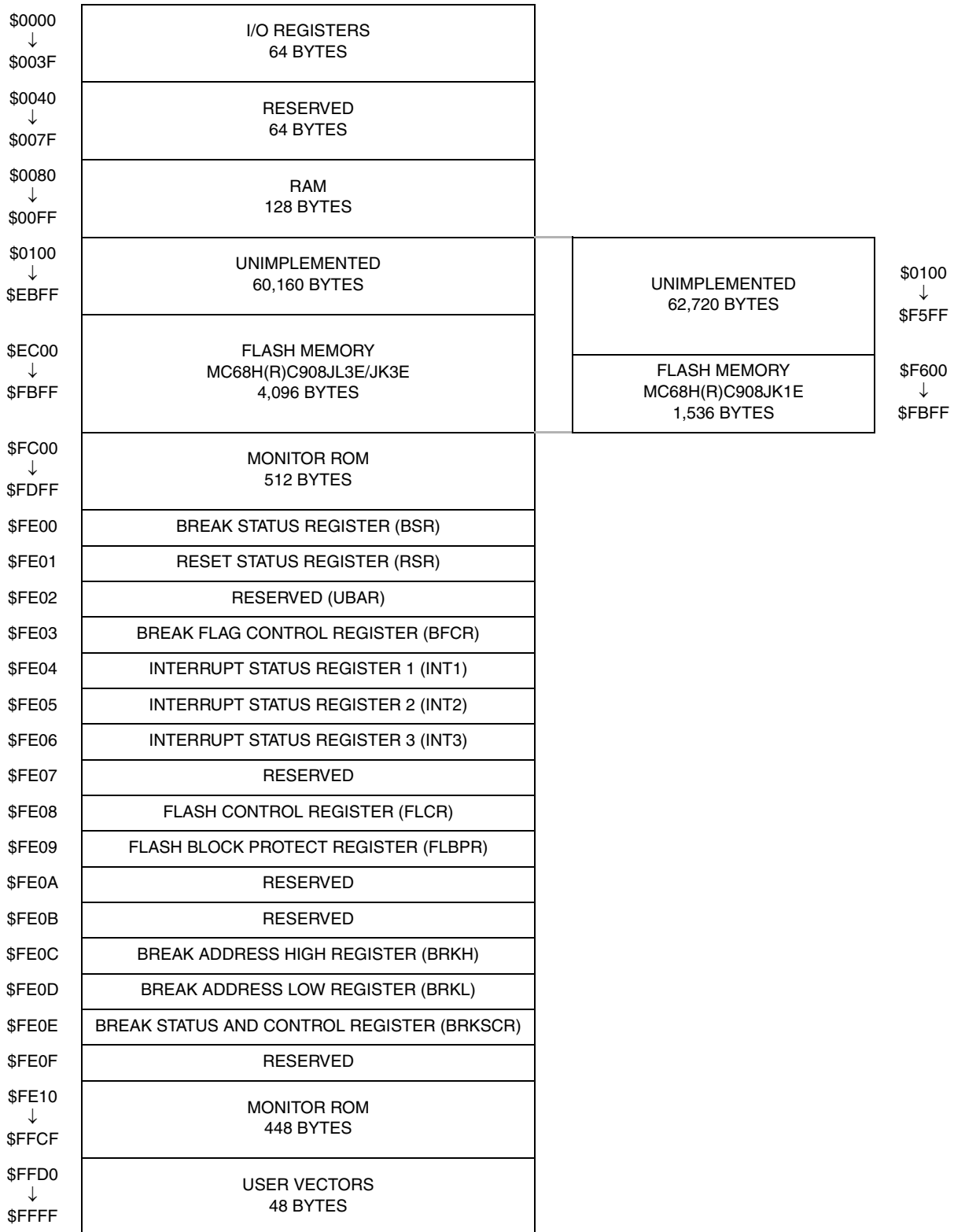


Figure 2-1. Memory Map

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$0000	Port A Data Register (PTA)	Read:	0	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	Unaffected by reset							
\$0001	Port B Data Register (PTB)	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
\$0002	Unimplemented	Read:								
		Write:								
\$0003	Port D Data Register (PTD)	Read:	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
		Write:								
		Reset:	Unaffected by reset							
\$0004	Data Direction Register A (DDRA)	Read:	0	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0005	Data Direction Register B (DDRB)	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0006	Unimplemented	Read:								
		Write:								
\$0007	Data Direction Register D (DDR D)	Read:	DDR D7	DDR D6	DDR D5	DDR D4	DDR D3	DDR D2	DDR D1	DDR D0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0008 ↓ \$0009	Unimplemented	Read:								
		Write:								
\$000A	Port D Control Register (PDCR)	Read:	0	0	0	0	SLOWD7	SLOWD6	PTDPU7	PTDPU6
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000B ↓ \$000C	Unimplemented	Read:								
		Write:								
\$000D	Port A Input Pull-up Enable Register (PTAPUE)	Read:	PTA6EN	PTAPUE6	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$000E ↓ \$0019	Unimplemented	Read:								
		Write:								

= Unimplemented = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 1 of 4)

Memory

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$001A	Keyboard Status and Control Register (KBSCR)	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:						ACKK		
		Reset:	0	0	0	0	0	0	0	0
\$001B	Keyboard Interrupt Enable Register (KBIER)	Read:	0	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$001C	Unimplemented	Read:								
		Write:								
\$001D	IRQ Status and Control Register (INTSCR)	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:						ACK		
		Reset:	0	0	0	0	0	0	0	0
\$001E	Configuration Register 2 (CONFIG2) [†]	Read:	IRQPUD	R	R	LVIT1	LVIT0	R	R	R
		Write:								
		Reset:	0	0	0	0*	0*	0	0	0
\$001F	Configuration Register 1 (CONFIG1) [†]	Read:	COPRS	R	R	LVID	R	SSREC	STOP	COPD
		Write:								
		Reset:	0	0	0	0	0	0	0	0

[†] One-time writable register after each reset. * LVIT1 and LVIT0 reset to 0 by a power-on reset (POR) only.

\$0020	TIM Status and Control Register (TSC)	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
\$0021	TIM Counter Register High (TCNTH)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0022	TIM Counter Register Low (TCNTL)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0023	TIM Counter Modulo Register High (TMODH)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0024	TIM Counter Modulo Register Low (TMODL)	Read:	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0025	TIM Channel 0 Status and Control Register (TSC0)	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0026	TIM Channel 0 Register High (TCH0H)	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:								
		Reset:	Indeterminate after reset							

= Unimplemented

R = Reserved

Figure 2-2. Control, Status, and Data Registers (Sheet 2 of 4)

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$0027	TIM Channel 0 Register Low (TCH0L)	Read: Bit7 Write: Bit7	Read: Bit6 Write: Bit6	Read: Bit5 Write: Bit5	Read: Bit4 Write: Bit4	Read: Bit3 Write: Bit3	Read: Bit2 Write: Bit2	Read: Bit1 Write: Bit1	Read: Bit0 Write: Bit0
		Reset: Indeterminate after reset							
\$0028	TIM Channel 1 Status and Control Register (TSC1)	Read: CH1F Write: 0	Read: CH1IE Write: CH1IE	Read: 0 Write: 0	Read: MS1A Write: MS1A	Read: ELS1B Write: ELS1B	Read: ELS1A Write: ELS1A	Read: TOV1 Write: TOV1	Read: CH1MAX Write: CH1MAX
		Reset: 0 0 0 0 0 0 0 0							
\$0029	TIM Channel 1 Register High (TCH1H)	Read: Bit15 Write: Bit15	Read: Bit14 Write: Bit14	Read: Bit13 Write: Bit13	Read: Bit12 Write: Bit12	Read: Bit11 Write: Bit11	Read: Bit10 Write: Bit10	Read: Bit9 Write: Bit9	Read: Bit8 Write: Bit8
		Reset: Indeterminate after reset							
\$002A	TIM Channel 1 Register Low (TCH1L)	Read: Bit7 Write: Bit7	Read: Bit6 Write: Bit6	Read: Bit5 Write: Bit5	Read: Bit4 Write: Bit4	Read: Bit3 Write: Bit3	Read: Bit2 Write: Bit2	Read: Bit1 Write: Bit1	Read: Bit0 Write: Bit0
		Reset: Indeterminate after reset							
\$002B ↓ \$003B	Unimplemented	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]
\$003C	ADC Status and Control Register (ADSCR)	Read: COCO Write: [Grey]	Read: AIEN Write: AIEN	Read: ADCO Write: ADCO	Read: ADCH4 Write: ADCH4	Read: ADCH3 Write: ADCH3	Read: ADCH2 Write: ADCH2	Read: ADCH1 Write: ADCH1	Read: ADCH0 Write: ADCH0
		Reset: 0 0 0 1 1 1 1 1							
\$003D	ADC Data Register (ADR)	Read: AD7 Write: [Grey]	Read: AD6 Write: [Grey]	Read: AD5 Write: [Grey]	Read: AD4 Write: [Grey]	Read: AD3 Write: [Grey]	Read: AD2 Write: [Grey]	Read: AD1 Write: [Grey]	Read: AD0 Write: [Grey]
		Reset: Indeterminate after reset							
\$003E	ADC Input Clock Register (ADICLK)	Read: ADIV2 Write: ADIV2	Read: ADIV1 Write: ADIV1	Read: ADIV0 Write: ADIV0	Read: 0 Write: [Grey]	Read: 0 Write: [Grey]	Read: 0 Write: [Grey]	Read: 0 Write: [Grey]	Read: 0 Write: [Grey]
		Reset: 0 0 0 0 0 0 0 0							
\$003F	Unimplemented	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]	Read: [Grey] Write: [Grey]
\$FE00	Break Status Register (BSR)	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: SBSW Write: See note	Read: R Write: R
		Reset: 0							
Note: Writing a 0 clears SBSW.									
\$FE01	Reset Status Register (RSR)	Read: POR Write: [Grey]	Read: PIN Write: [Grey]	Read: COP Write: [Grey]	Read: ILOP Write: [Grey]	Read: ILAD Write: [Grey]	Read: MODRST Write: [Grey]	Read: LVI Write: [Grey]	Read: 0 Write: [Grey]
		POR: 1 0 0 0 0 0 0 0							
\$FE02	Reserved	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R
\$FE03	Break Flag Control Register (BFCR)	Read: BCFE Write: BCFE	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R	Read: R Write: R
		Reset: 0							
		[Grey] = Unimplemented				[R] = Reserved			

Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 4)