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MC68HC908MR32
MC68HC908MR16

Data Sheet

M68HC08
Microcontrollers

MC68HC908MR32
Rev. 6.1
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MC68HC908MR32
MC68HC908MR16

Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
August, 2001	3.0	Figure 2-1. MC68HC908MR32 Memory Map — Added FLASH Block Protect Register (FLBPR) at address location $FF7E	29
		Figure A-1. MC68HC908MR16 Memory Map — Added FLASH Block Protect Register (FLBPR) at address location $FF7E	306
October, 2001	4.0	3.3.3 Conversion Time — Reworked equations and text for clarity.	50
December, 2001	5.0	Figure 18-8. Monitor Mode Circuit — PTA7 and connecting circuitry added	279
		Table 18-2. Monitor Mode Signal Requirements and Options — Switch locations added to column headings for clarity	281
		Section 16. Timer Interface A (TIMA) — Timer discrepancies corrected throughout this section.	233
		Section 17. Timer Interface B (TIMB) — Timer discrepancies corrected throughout this section.	255
November, 2003	6.0	Reformatted to meet current publication standards	Throughout
		2.8.2 FLASH Page Erase Operation — Procedure reworked for clarity	42
		2.8.3 FLASH Mass Erase Operation — Procedure reworked for clarity	42
		2.8.4 FLASH Program Operation — Procedure reworked for clarity	43
		Figure 14-14. SIM Break Status Register (SBSR) — Clarified definition of SBSW bit.	207
		19.5 DC Electrical Characteristics — Corrected maximum value for monitor mode entry voltage (on $\overline{\text{IRQ}}$)	291
		19.6 FLASH Memory Characteristics — Updated table entries	292
July, 2005	6.1	Updated to meet Freescale identity guidelines.	Throughout

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Appendix A
MC68HC908MR16

Chapter 1
General Description

1.1 Introduction

The MC68HC908MR32 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

The information contained in this document pertains to the MC68HC908MR16 with the exceptions shown in Appendix A MC68HC908MR16.

1.2 Features

Features include:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- On-chip FLASH memory with in-circuit programming capabilities of FLASH program memory:
  MC68HC908MR32 — 32 Kbytes
  MC68HC908MR16 — 16 Kbytes
- On-chip programming firmware for use with host personal computer
- FLASH data security[1]
- 768 bytes of on-chip random-access memory (RAM)
- 12-bit, 6-channel center-aligned or edge-aligned pulse-width modulator (PWMMC)
- Serial peripheral interface module (SPI)
- Serial communications interface module (SCI)
- 16-bit, 4-channel timer interface module (TIMA)
- 16-bit, 2-channel timer interface module (TIMB)
- Clock generator module (CGM)
- Low-voltage inhibit (LVI) module with software selectable trip points
- 10-bit, 10-channel analog-to-digital converter (ADC)
- System protection features:
  – Optional computer operating properly (COP) reset
  – Low-voltage detection with optional reset
  – Illegal opcode or address detection with optional reset
  – Fault detection with optional PWM disabling

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

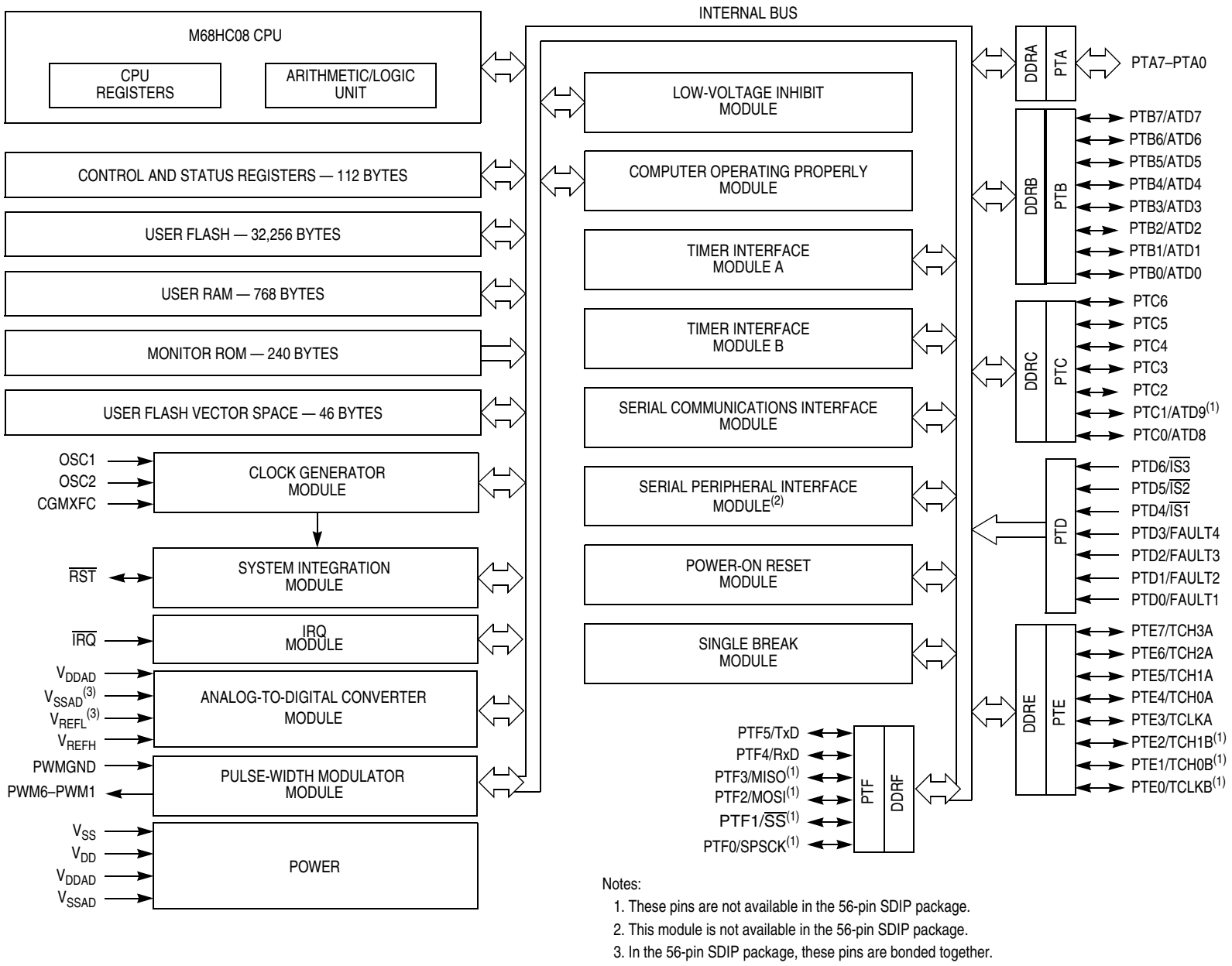
- Available packages:
  - 64-pin plastic quad flat pack (QFP)
  - 56-pin shrink dual in-line package (SDIP)
- Low-power design, fully static with wait mode
- Master reset pin ($\overline{\text{RST}}$) and power-on reset (POR)
- Stop mode as an option
- Break module (BRK) supports setting the in-circuit simulator (ICS) single break point

Features of the CPU08 include:

- Enhanced M68HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the M68HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908MR32.



Notes:
1. These pins are not available in the 56-pin SDIP package.
2. This module is not available in the 56-pin SDIP package.
3. In the 56-pin SDIP package, these pins are bonded together.

Figure 1-1. MCU Block Diagram

1.4 Pin Assignments

Figure 1-2 shows the 64-pin QFP pin assignments and Figure 1-3 shows the 56-pin SDIP pin assignments.

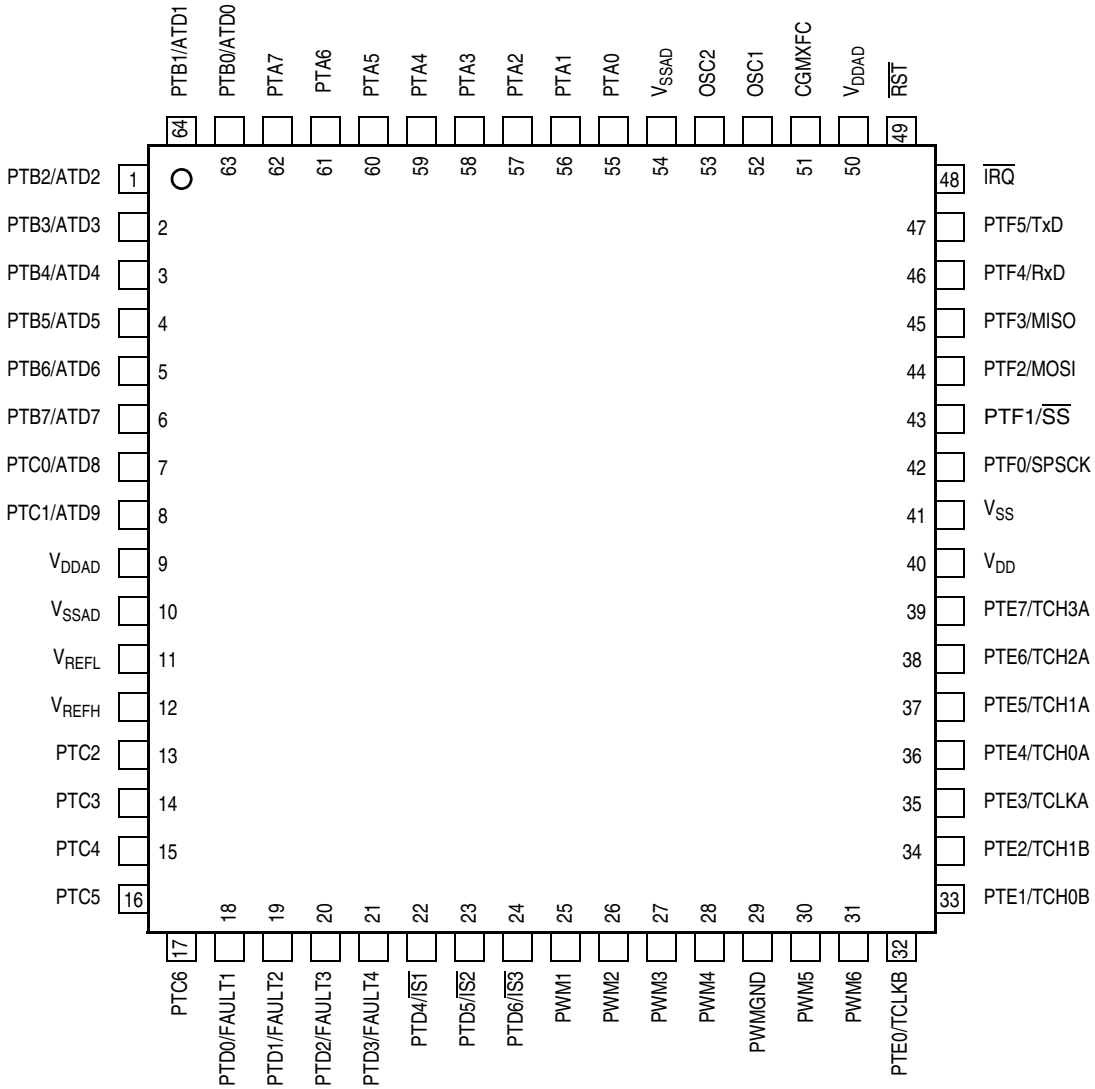
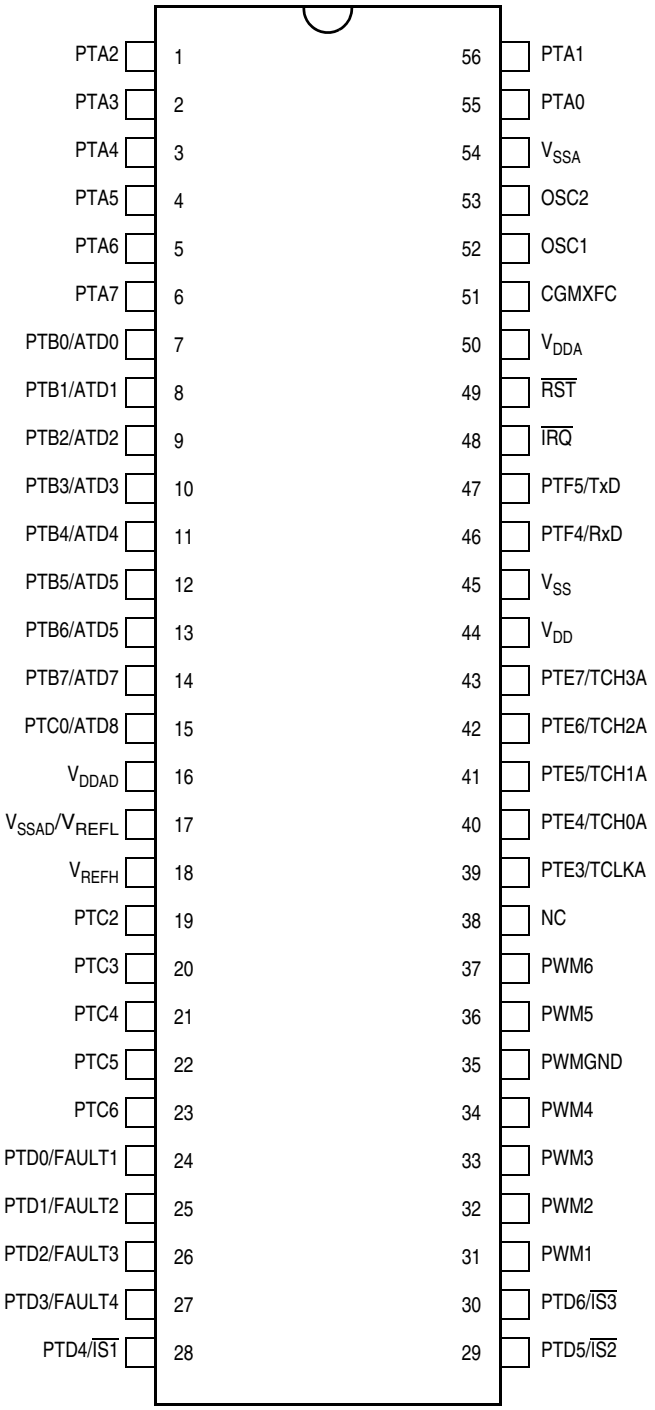


Figure 1-2. 64-Pin QFP Pin Assignments



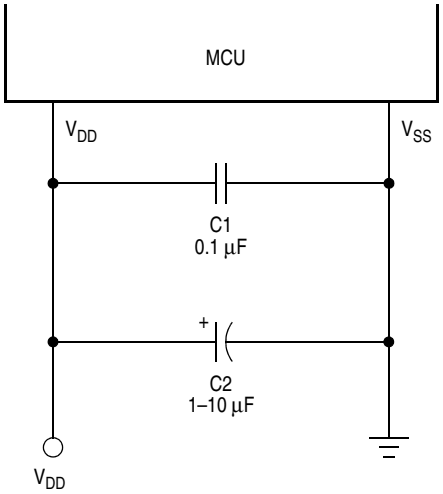
Note:
PTC1, PTE0, PTE1, PTE2, PTF0, PTF1, PTF2, and PTF3 are removed from this package.

Figure 1-3. 56-Pin SDIP Pin Assignments

1.4.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as Figure 1-4 shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high-current levels.



Note: Component values shown represent typical applications.

Figure 1-4. Power Supply Bypassing

1.4.2 Oscillator Pins (OSC1 and OSC2)

The OSC1 and OSC2 pins are the connections for the on-chip oscillator circuit. For more detailed information, see Chapter 4 Clock Generator Module (CGM).

1.4.3 External Reset Pin ($\overline{RST}$)

A logic 0 on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. See Chapter 14 System Integration Module (SIM).

1.4.4 External Interrupt Pin ($\overline{IRQ}$)

$\overline{IRQ}$ is an asynchronous external interrupt pin. See Chapter 8 External Interrupt (IRQ).

1.4.5 CGM Power Supply Pins (V_{DDA} and V_{SSAD})

V_{DDA} and V_{SSAD} are the power supply pins for the analog portion of the clock generator module (CGM). Decoupling of these pins should be per the digital supply. See Chapter 4 Clock Generator Module (CGM).

1.4.6 External Filter Capacitor Pin (CGMXFC)

CGMXFC is an external filter capacitor connection for the CGM. See Chapter 4 Clock Generator Module (CGM).

1.4.7 Analog Power Supply Pins (V_{DDAD} and V_{SSAD})

V_{DDAD} and V_{SSAD} are the power supply pins for the analog-to-digital converter. Decoupling of these pins should be per the digital supply. See Chapter 3 Analog-to-Digital Converter (ADC).

1.4.8 ADC Voltage Decoupling Capacitor Pin (V_{REFH})

V_{REFH} is the power supply for setting the reference voltage. Connect the V_{REFH} pin to the same voltage potential as V_{DDAD}. See Chapter 3 Analog-to-Digital Converter (ADC).

1.4.9 ADC Voltage Reference Low Pin (V_{REFL})

V_{REFL} is the lower reference supply for the ADC. Connect the V_{REFL} pin to the same voltage potential as V_{SSAD}. See Chapter 3 Analog-to-Digital Converter (ADC).

1.4.10 Port A Input/Output (I/O) Pins (PTA7–PTA0)

PTA7–PTA0 are general-purpose bidirectional input/output (I/O) port pins. See Chapter 10 Input/Output (I/O) Ports (PORTS).

1.4.11 Port B I/O Pins (PTB7/ATD7–PTB0/ATD0)

Port B is an 8-bit special function port that shares all eight pins with the analog-to-digital converter (ADC). See Chapter 3 Analog-to-Digital Converter (ADC) and Chapter 10 Input/Output (I/O) Ports (PORTS).

1.4.12 Port C I/O Pins (PTC6–PTC2 and PTC1/ATD9–PTC0/ATD8)

PTC6–PTC2 are general-purpose bidirectional I/O port pins Chapter 10 Input/Output (I/O) Ports (PORTS). PTC1/ATD9–PTC0/ATD8 are special function port pins that are shared with the analog-to-digital converter (ADC). See Chapter 3 Analog-to-Digital Converter (ADC) and Chapter 10 Input/Output (I/O) Ports (PORTS).

1.4.13 Port D Input-Only Pins (PTD6/$\overline{IS3}$–PTD4/$\overline{IS1}$ and PTD3/FAULT4–PTD0/FAULT1)

PTD6/$\overline{IS3}$–PTD4/$\overline{IS1}$ are special function input-only port pins that also serve as current sensing pins for the pulse-width modulator module (PWMMC). PTD3/FAULT4–PTD0/FAULT1 are special function port pins that also serve as fault pins for the PWMMC. See Chapter 12 Pulse-Width Modulator for Motor Control (PWMMC) and Chapter 10 Input/Output (I/O) Ports (PORTS).

1.4.14 PWM Pins (PWM6–PWM1)

PWM6–PWM1 are dedicated pins used for the outputs of the pulse-width modulator module (PWMMC). These are high-current sink pins. See Chapter 12 Pulse-Width Modulator for Motor Control (PWMMC) and Chapter 19 Electrical Specifications.

1.4.15 PWM Ground Pin (PWMGND)

PWMGND is the ground pin for the pulse-width modulator module (PWMMC). This dedicated ground pin is used as the ground for the six high-current PWM pins. See Chapter 12 Pulse-Width Modulator for Motor Control (PWMMC).

1.4.16 Port E I/O Pins (PTE7/TCH3A–PTE3/TCLKA and PTE2/TCH1B–PTE0/TCLKB)

Port E is an 8-bit special function port that shares its pins with the two timer interface modules (TIMA and TIMB). See Chapter 16 Timer Interface A (TIMA), Chapter 17 Timer Interface B (TIMB), and Chapter 10 Input/Output (I/O) Ports (PORTS).

1.4.17 Port F I/O Pins (PTF5/TxD–PTF4/RxD and PTF3/MISO–PTF0/SPSCK)

Port F is a 6-bit special function port that shares two of its pins with the serial communications interface module (SCI) and four of its pins with the serial peripheral interface module (SPI). See Chapter 15 Serial Peripheral Interface Module (SPI), Chapter 13 Serial Communications Interface Module (SCI), and Chapter 10 Input/Output (I/O) Ports (PORTS).

Chapter 2
Memory

2.1 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in Figure 2-1, includes:

- 32 Kbytes of FLASH
- 768 bytes of random-access memory (RAM)
- 46 bytes of user-defined vectors
- 240 bytes of monitor read-only memory (ROM)

2.2 Unimplemented Memory Locations

Some addresses are unimplemented. Accessing an unimplemented address can cause an illegal address reset. In the memory map and in the input/output (I/O) register summary, unimplemented addresses are shaded.

Some I/O bits are read only; the write function is unimplemented. Writing to a read-only I/O bit has no effect on microcontroller unit (MCU) operation. In register figures, the write function of read-only bits is shaded.

Similarly, some I/O bits are write only; the read function is unimplemented. Reading of write-only I/O bits has no effect on MCU operation. In register figures, the read function of write-only bits is shaded.

2.3 Reserved Memory Locations

Some addresses are reserved. Writing to a reserved address can have unpredictable effects on MCU operation. In the memory map (Figure 2-1) and in the I/O register summary (Figure 2-2) reserved addresses are marked with the word reserved.

Some I/O bits are reserved. Writing to a reserved bit can have unpredictable effects on MCU operation. In register figures, reserved bits are marked with the letter R.