



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Addendum to MC68HC908QC16, rev. 5

This addendum introduces a change to this data sheet.

## Chapter 18 Development Support, Section 18.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations \$FFF6–\$FFFD. Locations \$FFF6–\$FFFD contain user-defined data.

### **NOTE**

*Do not leave locations \$FFF6–\$FFFD blank. For security reasons, program locations \$FFF6–\$FFFD even if they are not used for vectors.*

Changes to:

## Chapter 18 Development Support, Section 18.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations \$FFF6–\$FFFD. Locations \$FFF6–\$FFFD contain user-defined data.

### **NOTE**

*Do not leave locations \$FFF6–\$FFFD blank. For security reasons, program locations \$FFF6–\$FFFD even if they are not used for vectors. An improved security function denies monitor mode entry if five or more of the eight security bytes are \$00 (zero bytes).*

# MC68HC908QC16

# MC68HC908QC8

# MC68HC908QC4

Data Sheet

***M68HC08***  
***Microcontrollers***

MC68HC908QC16  
Rev. 5  
4/2008

[freescale.com](http://freescale.com)



**MC68HC908QC16**

**MC68HC908QC8**

**MC68HC908QC4**

**Data Sheet**

---

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://www.freescale.com>

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.  
This product incorporates SuperFlash® technology licensed from SST.

© Freescale Semiconductor, Inc., 2007, 2008. All rights reserved.

## Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

## Revision History

Date	Revision Level	Description	Page Number(s)
April, 2006	1.0	Initial release	N/A
May, 2006	1.1	19.5 5-V DC Electrical Characteristics — Updated values	237
		19.8 3.3-V DC Electrical Characteristics — Updated values	240
		19.11 Oscillator Characteristics — Updated values	243
		Figure 19-9. Typical 5-Volt Run Current versus Bus Frequency (25 C) and Figure 19-10. Typical 3.3-Volt Run Current versus Bus Frequency (25 C) — added	247
October, 2006	2.0	1.7 Unused Pin Termination — Added new section	24
		11.2 Unused Pin Termination — Replaced note with new section	107
		19.5 5-V DC Electrical Characteristics — New values for: DC injection current Low-voltage inhibit reset, trip rising voltage	237
		19.8 3.3-V DC Electrical Characteristics — New values for: DC injection current Low-voltage inhibit reset, trip rising voltage	240
		19.12 Supply Current Characteristics — New values for stop mode supply currents at -40 to 125°C	246
		20.3 Package Dimensions — Updated package dimension drawing for the 28-lead TSSOP.	261
April, 2007	3.0	Table 1-2. Pin Functions — Added note	22
		Figure 2-2. Control, Status, and Data Registers — Corrected Port C Data Register bit PTC3	27
		Chapter 3 Analog-to-Digital Converter (ADC10) Module — Renamed ADCSC register to ADSCR to be consistent with development tools	45
		Chapter 4 Configuration Registers (CONFIG1 and CONFIG2) — Changed CGMXCLK to BUSCLKX4	60
		11.3 Port A — Added information to first paragraph of note	107
		11.3.1 Port A Data Register — Corrected bit designations for the first entry under Figure 11-1. Port A Data Register (PTA).	108
		11.5 Port C — Added note and corrected address location designation in last paragraph	112 113
		Chapter 13 Enhanced Serial Communications Interface (ESCI) Module — Changed SCIBDSRC to ESCIBDSRC and CGMXCLK to BUSCLKX4	123
		13.9.3 Bit Time Measurement — Corrected first sentence of listing number 1	150
		Figure 18-18. Monitor Mode Entry Timing — Changed CGMXCLK to BUSCLKX4	234
October, 2007	4.0	In 19.12 Supply Current Characteristics, updated stop I <sub>DD</sub> values	246
April, 2008	5.0	In <a href="#">19.12 Supply Current Characteristics</a> , reverted to Rev. 3 stop I <sub>DD</sub> values	<a href="#">246</a>

# List of Sections

Chapter 1 General Description . . . . .	17
Chapter 2 Memory . . . . .	25
Chapter 3 Analog-to-Digital Converter (ADC10) Module . . . . .	45
Chapter 4 Configuration Registers (CONFIG1 and CONFIG2) . . . . .	59
Chapter 5 Computer Operating Properly (COP) . . . . .	63
Chapter 6 Central Processor Unit (CPU) . . . . .	67
Chapter 7 External Interrupt (IRQ) . . . . .	79
Chapter 8 Keyboard Interrupt Module (KBI) . . . . .	85
Chapter 9 Low-Voltage Inhibit (LVI) . . . . .	93
Chapter 10 Oscillator Mode (OSC) . . . . .	97
Chapter 11 Input/Output Ports (PORTS) . . . . .	107
Chapter 12 Periodic Wakeup Module (PWU) . . . . .	117
Chapter 13 Enhanced Serial Communications Interface (ESCI) Module . . . . .	123
Chapter 14 System Integration Module (SIM) . . . . .	153
Chapter 15 Serial Peripheral Interface (SPI) Module . . . . .	169
Chapter 16 Timer Interface Module (TIM1) . . . . .	189
Chapter 17 Timer Interface Module (TIM2) . . . . .	205
Chapter 18 Development Support . . . . .	219
Chapter 19 Electrical Specifications . . . . .	235
Chapter 20 Ordering Information and Mechanical Specifications . . . . .	257





# Table of Contents

## Chapter 1 General Description

1.1	Introduction . . . . .	17
1.2	Features . . . . .	17
1.3	MCU Block Diagram . . . . .	19
1.4	Pin Assignments . . . . .	19
1.5	Pin Functions . . . . .	19
1.6	Pin Function Priority . . . . .	24
1.7	Unused Pin Termination . . . . .	24

## Chapter 2 Memory

2.1	Introduction . . . . .	25
2.2	Unimplemented Memory Locations . . . . .	25
2.3	Reserved Memory Locations . . . . .	25
2.4	Direct Page Registers . . . . .	25
2.5	Random-Access Memory (RAM) . . . . .	35
2.6	FLASH Memory (FLASH) . . . . .	36
2.6.1	FLASH Control Register . . . . .	36
2.6.2	FLASH Page Erase Operation . . . . .	37
2.6.3	FLASH Mass Erase Operation . . . . .	38
2.6.4	FLASH Program Operation . . . . .	39
2.6.5	FLASH Protection . . . . .	41
2.6.6	FLASH Block Protect Register . . . . .	41
2.6.7	EEPROM Memory Emulation Using FLASH Memory . . . . .	42

## Chapter 3 Analog-to-Digital Converter (ADC10) Module

3.1	Introduction . . . . .	45
3.2	Features . . . . .	45
3.3	Functional Description . . . . .	45
3.3.1	Clock Select and Divide Circuit . . . . .	47
3.3.2	Input Select and Pin Control . . . . .	48
3.3.3	Conversion Control . . . . .	48
3.3.3.1	Initiating Conversions . . . . .	48
3.3.3.2	Completing Conversions . . . . .	48
3.3.3.3	Aborting Conversions . . . . .	48
3.3.3.4	Total Conversion Time . . . . .	49
3.3.4	Sources of Error . . . . .	50
3.3.4.1	Sampling Error . . . . .	50
3.3.4.2	Pin Leakage Error . . . . .	50
3.3.4.3	Noise-Induced Errors . . . . .	50

## Table of Contents

3.3.4.4	Code Width and Quantization Error . . . . .	51
3.3.4.5	Linearity Errors . . . . .	51
3.3.4.6	Code Jitter, Non-Monotonicity and Missing Codes. . . . .	51
3.4	Interrupts . . . . .	52
3.5	Low-Power Modes . . . . .	52
3.5.1	Wait Mode . . . . .	52
3.5.2	Stop Mode . . . . .	52
3.6	ADC10 During Break Interrupts . . . . .	52
3.7	I/O Signals . . . . .	53
3.7.1	ADC10 Analog Power Pin ( $V_{DDA}$ ) . . . . .	53
3.7.2	ADC10 Analog Ground Pin ( $V_{SSA}$ ) . . . . .	53
3.7.3	ADC10 Voltage Reference High Pin ( $V_{REFH}$ ) . . . . .	53
3.7.4	ADC10 Voltage Reference Low Pin ( $V_{REFL}$ ) . . . . .	53
3.7.5	ADC10 Channel Pins (ADn) . . . . .	54
3.8	Registers . . . . .	54
3.8.1	ADC10 Status and Control Register . . . . .	54
3.8.2	ADC10 Result High Register (ADRH) . . . . .	56
3.8.3	ADC10 Result Low Register (ADRL) . . . . .	56
3.8.4	ADC10 Clock Register (ADCLK) . . . . .	56

## Chapter 4

### Configuration Registers (CONFIG1 and CONFIG2)

4.1	Introduction . . . . .	59
4.2	Functional Description . . . . .	59

## Chapter 5

### Computer Operating Properly (COP)

5.1	Introduction . . . . .	63
5.2	Functional Description . . . . .	63
5.3	I/O Signals . . . . .	64
5.3.1	BUSCLKX4 . . . . .	64
5.3.2	STOP Instruction . . . . .	64
5.3.3	COPCTL Write . . . . .	64
5.3.4	Power-On Reset. . . . .	64
5.3.5	Internal Reset. . . . .	64
5.3.6	COPD (COP Disable). . . . .	64
5.3.7	COPRS (COP Rate Select) . . . . .	65
5.4	COP Control Register . . . . .	65
5.5	Interrupts . . . . .	65
5.6	Monitor Mode . . . . .	65
5.7	Low-Power Modes . . . . .	65
5.7.1	Wait Mode . . . . .	65
5.7.2	Stop Mode . . . . .	65
5.8	COP Module During Break Mode . . . . .	65

## Chapter 6 Central Processor Unit (CPU)

6.1	Introduction . . . . .	67
6.2	Features . . . . .	67
6.3	CPU Registers . . . . .	67
6.3.1	Accumulator . . . . .	68
6.3.2	Index Register . . . . .	68
6.3.3	Stack Pointer . . . . .	69
6.3.4	Program Counter . . . . .	69
6.3.5	Condition Code Register . . . . .	70
6.4	Arithmetic/Logic Unit (ALU) . . . . .	71
6.5	Low-Power Modes . . . . .	71
6.5.1	Wait Mode . . . . .	71
6.5.2	Stop Mode . . . . .	71
6.6	CPU During Break Interrupts . . . . .	71
6.7	Instruction Set Summary . . . . .	72
6.8	Opcode Map . . . . .	77

## Chapter 7 External Interrupt (IRQ)

7.1	Introduction . . . . .	79
7.2	Features . . . . .	79
7.3	Functional Description . . . . .	79
7.3.1	MODE = 1 . . . . .	81
7.3.2	MODE = 0 . . . . .	82
7.4	Interrupts . . . . .	82
7.5	Low-Power Modes . . . . .	82
7.5.1	Wait Mode . . . . .	82
7.5.2	Stop Mode . . . . .	82
7.6	IRQ Module During Break Interrupts . . . . .	82
7.7	I/O Signals . . . . .	83
7.7.1	IRQ Input Pins ( $\bar{I}RQ$ ) . . . . .	83
7.8	Registers . . . . .	83

## Chapter 8 Keyboard Interrupt Module (KBI)

8.1	Introduction . . . . .	85
8.2	Features . . . . .	85
8.3	Functional Description . . . . .	85
8.3.1	Keyboard Operation . . . . .	87
8.3.1.1	MODEK = 1 . . . . .	87
8.3.1.2	MODEK = 0 . . . . .	87
8.3.2	Keyboard Initialization . . . . .	88
8.4	Interrupts . . . . .	88
8.5	Low-Power Modes . . . . .	88
8.5.1	Wait Mode . . . . .	88
8.5.2	Stop Mode . . . . .	88
8.6	KBI During Break Interrupts . . . . .	89

## Table of Contents

8.7	I/O Signals . . . . .	89
8.7.1	KBI Input Pins (KBI7:KBI0) . . . . .	89
8.8	Registers . . . . .	89
8.8.1	Keyboard Status and Control Register (KBSCR) . . . . .	89
8.8.2	Keyboard Interrupt Enable Register (KBIER) . . . . .	90
8.8.3	Keyboard Interrupt Polarity Register (KBIPR) . . . . .	91

## Chapter 9 Low-Voltage Inhibit (LVI)

9.1	Introduction . . . . .	93
9.2	Features . . . . .	93
9.3	Functional Description . . . . .	93
9.3.1	Polled LVI Operation . . . . .	94
9.3.2	Forced Reset Operation . . . . .	94
9.3.3	LVI Hysteresis . . . . .	94
9.3.4	LVI Trip Selection . . . . .	94
9.4	LVI Interrupts . . . . .	95
9.5	Low-Power Modes . . . . .	95
9.5.1	Wait Mode . . . . .	95
9.5.2	Stop Mode . . . . .	95
9.6	Registers . . . . .	95

## Chapter 10 Oscillator Mode (OSC)

10.1	Introduction . . . . .	97
10.2	Features . . . . .	97
10.3	Functional Description . . . . .	97
10.3.1	Internal Signal Definitions . . . . .	97
10.3.1.1	Oscillator Enable Signal (SIMOSCEN) . . . . .	97
10.3.1.2	XTAL Oscillator Clock (XTALCLK) . . . . .	99
10.3.1.3	RC Oscillator Clock (RCCLK) . . . . .	99
10.3.1.4	Internal Oscillator Clock (INTCLK) . . . . .	99
10.3.1.5	Bus Clock Times 4 (BUSCLKX4) . . . . .	99
10.3.1.6	Bus Clock Times 2 (BUSCLKX2) . . . . .	99
10.3.2	Internal Oscillator . . . . .	99
10.3.2.1	Internal Oscillator Trimming . . . . .	99
10.3.2.2	Internal to External Clock Switching . . . . .	100
10.3.2.3	External to Internal Clock Switching . . . . .	100
10.3.3	External Oscillator . . . . .	100
10.3.4	XTAL Oscillator . . . . .	100
10.3.5	RC Oscillator . . . . .	101
10.4	Interrupts . . . . .	102
10.5	Low-Power Modes . . . . .	102
10.5.1	Wait Mode . . . . .	102
10.5.2	Stop Mode . . . . .	102
10.6	OSC During Break Interrupts . . . . .	102
10.7	I/O Signals . . . . .	103
10.7.1	Oscillator Input Pin (OSC1) . . . . .	103
10.7.2	Oscillator Output Pin (OSC2) . . . . .	103

10.8	Registers	103
10.8.1	Oscillator Status and Control Register	103
10.8.2	Oscillator Trim Register (OSCTRIM)	105

## Chapter 11 Input/Output Ports (PORTS)

11.1	Introduction	107
11.2	Unused Pin Termination	107
11.3	Port A	107
11.3.1	Port A Data Register	108
11.3.2	Data Direction Register A	108
11.3.3	Port A Input Pullup Enable Register	109
11.4	Port B	110
11.4.1	Port B Data Register	110
11.4.2	Data Direction Register B	110
11.4.3	Port B Input Pullup Enable Register	111
11.5	Port C	112
11.5.1	Port C Data Register	112
11.5.2	Data Direction Register C	113
11.5.3	Port C Input Pullup Enable Register	114
11.6	Port D	114
11.6.1	Port D Data Register	114
11.6.2	Data Direction Register D	115
11.6.3	Port D Input Pullup Enable Register	116

## Chapter 12 Periodic Wakeup Module (PWU)

12.1	Introduction	117
12.2	Features	117
12.3	Functional Description	117
12.4	Interrupts	118
12.5	Low-Power Modes	118
12.5.1	Wait Mode	118
12.5.2	Stop Mode	119
12.6	PWU During Break Interrupts	119
12.7	I/O Signals	119
12.8	Registers	119
12.8.1	Periodic Wakeup Status and Control Register	119
12.8.2	Periodic Wakeup Prescaler Register	120
12.8.3	Periodic Wakeup Modulo Register	121

## Chapter 13 Enhanced Serial Communications Interface (ESCI) Module

13.1	Introduction	123
13.2	Features	123
13.3	Functional Description	125
13.3.1	Data Format	126
13.3.2	Transmitter	126
13.3.2.1	Character Length	126

## Table of Contents

13.3.2.2	Character Transmission . . . . .	126
13.3.2.3	Break Characters . . . . .	127
13.3.2.4	Idle Characters . . . . .	128
13.3.2.5	Inversion of Transmitted Output . . . . .	128
13.3.3	Receiver . . . . .	128
13.3.3.1	Character Length . . . . .	128
13.3.3.2	Character Reception . . . . .	128
13.3.3.3	Data Sampling . . . . .	130
13.3.3.4	Framing Errors . . . . .	131
13.3.3.5	Baud Rate Tolerance . . . . .	131
13.3.3.6	Receiver Wakeup . . . . .	133
13.4	Interrupts . . . . .	134
13.4.1	Transmitter Interrupts . . . . .	134
13.4.2	Receiver Interrupts . . . . .	134
13.4.3	Error Interrupts . . . . .	134
13.5	Low-Power Modes . . . . .	135
13.5.1	Wait Mode . . . . .	135
13.5.2	Stop Mode . . . . .	135
13.6	ESCI During Break Interrupts . . . . .	135
13.7	I/O Signals . . . . .	135
13.7.1	ESCI Transmit Data (TxD) . . . . .	135
13.7.2	ESCI Receive Data (RxD) . . . . .	136
13.8	Registers . . . . .	136
13.8.1	ESCI Control Register 1 . . . . .	136
13.8.2	ESCI Control Register 2 . . . . .	138
13.8.3	ESCI Control Register 3 . . . . .	140
13.8.4	ESCI Status Register 1 . . . . .	141
13.8.5	ESCI Status Register 2 . . . . .	143
13.8.6	ESCI Data Register . . . . .	144
13.8.7	ESCI Baud Rate Register . . . . .	144
13.8.8	ESCI Prescaler Register . . . . .	145
13.9	ESCI Arbiter . . . . .	149
13.9.1	ESCI Arbiter Control Register . . . . .	149
13.9.2	ESCI Arbiter Data Register . . . . .	150
13.9.3	Bit Time Measurement . . . . .	150
13.9.4	Arbitration Mode . . . . .	151

## Chapter 14 System Integration Module (SIM)

14.1	Introduction . . . . .	153
14.2	$\overline{RST}$ and $\overline{IRQ}$ Pins Initialization . . . . .	153
14.3	SIM Bus Clock Control and Generation . . . . .	153
14.3.1	Bus Timing . . . . .	155
14.3.2	Clock Start-Up from POR . . . . .	155
14.3.3	Clocks in Stop Mode and Wait Mode . . . . .	155
14.4	Reset and System Initialization . . . . .	155
14.4.1	External Pin Reset . . . . .	155

14.4.2	Active Resets from Internal Sources	156
14.4.2.1	Power-On Reset	157
14.4.2.2	Computer Operating Properly (COP) Reset	157
14.4.2.3	Illegal Opcode Reset	158
14.4.2.4	Illegal Address Reset	158
14.4.2.5	Low-Voltage Inhibit (LVI) Reset	158
14.5	SIM Counter	158
14.5.1	SIM Counter During Power-On Reset	158
14.5.2	SIM Counter During Stop Mode Recovery	158
14.5.3	SIM Counter and Reset States	159
14.6	Exception Control	159
14.6.1	Interrupts	159
14.6.1.1	Hardware Interrupts	159
14.6.1.2	SWI Instruction	162
14.6.2	Interrupt Status Registers	162
14.6.2.1	Interrupt Status Register 1	163
14.6.2.2	Interrupt Status Register 2	163
14.6.2.3	Interrupt Status Register 3	163
14.6.3	Reset	163
14.6.4	Break Interrupts	164
14.6.5	Status Flag Protection in Break Mode	164
14.7	Low-Power Modes	164
14.7.1	Wait Mode	164
14.7.2	Stop Mode	165
14.8	SIM Registers	166
14.8.1	SIM Reset Status Register	167
14.8.2	Break Flag Control Register	168

## Chapter 15

### Serial Peripheral Interface (SPI) Module

15.1	Introduction	169
15.2	Features	169
15.3	Functional Description	169
15.3.1	Master Mode	172
15.3.2	Slave Mode	172
15.3.3	Transmission Formats	173
15.3.3.1	Clock Phase and Polarity Controls	173
15.3.3.2	Transmission Format When CPHA = 0	173
15.3.3.3	Transmission Format When CPHA = 1	174
15.3.3.4	Transmission Initiation Latency	175
15.3.4	Queuing Transmission Data	177
15.3.5	Resetting the SPI	178
15.3.6	Error Conditions	178
15.3.6.1	Overflow Error	178
15.3.6.2	Mode Fault Error	180
15.4	Interrupts	181
15.5	Low-Power Modes	182
15.5.1	Wait Mode	182
15.5.2	Stop Mode	182

## Table of Contents

15.6	SPI During Break Interrupts	182
15.7	I/O Signals	183
15.7.1	MISO (Master In/Slave Out)	183
15.7.2	MOSI (Master Out/Slave In)	183
15.7.3	SPSCK (Serial Clock)	183
15.7.4	$\overline{SS}$ (Slave Select)	183
15.8	Registers	184
15.8.1	SPI Control Register	184
15.8.2	SPI Status and Control Register	186
15.8.3	SPI Data Register	188

## Chapter 16 Timer Interface Module (TIM1)

16.1	Introduction	189
16.2	Features	189
16.3	Functional Description	189
16.3.1	TIM1 Counter Prescaler	192
16.3.2	Input Capture	192
16.3.3	Output Compare	192
16.3.3.1	Unbuffered Output Compare	192
16.3.3.2	Buffered Output Compare	192
16.3.4	Pulse Width Modulation (PWM)	193
16.3.4.1	Unbuffered PWM Signal Generation	194
16.3.4.2	Buffered PWM Signal Generation	194
16.3.4.3	PWM Initialization	195
16.4	Interrupts	196
16.5	Low-Power Modes	196
16.5.1	Wait Mode	196
16.5.2	Stop Mode	196
16.6	TIM1 During Break Interrupts	197
16.7	I/O Signals	197
16.7.1	TIM1 Channel I/O Pins (T1CH3:T1CH0)	197
16.7.2	TIM1 Clock Pin (T1CLK)	197
16.8	Registers	197
16.8.1	TIM1 Status and Control Register	197
16.8.2	TIM1 Counter Registers	199
16.8.3	TIM1 Counter Modulo Registers	200
16.8.4	TIM1 Channel Status and Control Registers	200
16.8.5	TIM1 Channel Registers	204

## Chapter 17 Timer Interface Module (TIM2)

17.1	Introduction	205
17.2	Features	205
17.3	Functional Description	205
17.3.1	TIM2 Counter Prescaler	205
17.3.2	Input Capture	207



17.3.3	Output Compare . . . . .	207
17.3.3.1	Unbuffered Output Compare . . . . .	207
17.3.3.2	Buffered Output Compare . . . . .	208
17.3.4	Pulse Width Modulation (PWM) . . . . .	208
17.3.4.1	Unbuffered PWM Signal Generation . . . . .	209
17.3.4.2	Buffered PWM Signal Generation . . . . .	210
17.3.4.3	PWM Initialization . . . . .	210
17.4	Interrupts . . . . .	211
17.5	Low-Power Modes . . . . .	211
17.5.1	Wait Mode . . . . .	211
17.5.2	Stop Mode . . . . .	211
17.6	TIM2 During Break Interrupts . . . . .	211
17.7	I/O Signals . . . . .	212
17.7.1	TIM2 Channel I/O Pins (T2CH1:T2CH0) . . . . .	212
17.7.2	TIM2 Clock Pin (T2CLK) . . . . .	212
17.8	Registers . . . . .	212
17.8.1	TIM2 Status and Control Register . . . . .	212
17.8.2	TIM2 Counter Registers . . . . .	214
17.8.3	TIM2 Counter Modulo Registers . . . . .	215
17.8.4	TIM2 Channel Status and Control Registers . . . . .	215
17.8.5	TIM2 Channel Registers . . . . .	218

## Chapter 18 Development Support

18.1	Introduction . . . . .	219
18.2	Break Module (BRK) . . . . .	219
18.2.1	Functional Description . . . . .	219
18.2.1.1	Flag Protection During Break Interrupts . . . . .	221
18.2.1.2	TIM1 During Break Interrupts . . . . .	221
18.2.1.3	COP During Break Interrupts . . . . .	221
18.2.2	Break Module Registers . . . . .	222
18.2.2.1	Break Status and Control Register . . . . .	222
18.2.2.2	Break Address Registers . . . . .	222
18.2.2.3	Break Auxiliary Register . . . . .	223
18.2.2.4	Break Status Register . . . . .	223
18.2.2.5	Break Flag Control Register . . . . .	223
18.2.3	Low-Power Modes . . . . .	224
18.3	Monitor Module (MON) . . . . .	224
18.3.1	Functional Description . . . . .	224
18.3.1.1	Normal Monitor Mode . . . . .	228
18.3.1.2	Forced Monitor Mode . . . . .	229
18.3.1.3	Monitor Vectors . . . . .	229
18.3.1.4	Data Format . . . . .	230
18.3.1.5	Break Signal . . . . .	230
18.3.1.6	Baud Rate . . . . .	230
18.3.1.7	Commands . . . . .	230
18.3.2	Security . . . . .	234

**Chapter 19**  
**Electrical Specifications**

19.1	Introduction . . . . .	235
19.2	Absolute Maximum Ratings . . . . .	235
19.3	Functional Operating Range . . . . .	236
19.4	Thermal Characteristics . . . . .	236
19.5	5-V DC Electrical Characteristics . . . . .	237
19.6	Typical 5-V Output Drive Characteristics . . . . .	239
19.7	5-V Control Timing . . . . .	240
19.8	3.3-V DC Electrical Characteristics . . . . .	240
19.9	Typical 3.3-V Output Drive Characteristics . . . . .	242
19.10	3.3-V Control Timing . . . . .	243
19.11	Oscillator Characteristics . . . . .	243
19.12	Supply Current Characteristics . . . . .	246
19.13	ADC10 Characteristics . . . . .	248
19.14	5.0-Volt SPI Characteristics . . . . .	250
19.15	3.3-Volt SPI Characteristics . . . . .	251
19.16	Timer Interface Module Characteristics . . . . .	254
19.17	Memory Characteristics . . . . .	255

**Chapter 20**  
**Ordering Information and Mechanical Specifications**

20.1	Introduction . . . . .	257
20.2	MC Order Numbers . . . . .	257
20.3	Package Dimensions . . . . .	257

# Chapter 1

## General Description

### 1.1 Introduction

The MC68HC908QC16, MC68HC908QC8, and MC68HC908QC4 are members of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

**Table 1-1. Summary of Device Variations**

Device	FLASH Memory Size	RAM	Pin Count
MC68HC908QC16	16 Kbytes	512 bytes	16, 20, 28 pins
MC68HC908QC8	8 Kbytes	384 bytes	16, 20, 28 pins
MC68HC908QC4	4 Kbytes	384 bytes	16, 20, 28 pins

### 1.2 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- 5.0-V and 3.3-V operating voltages ( $V_{DD}$ )
- 8-MHz internal bus operation at 5 V, 4-MHz at 3.3 V
- Trimmable internal oscillator
  - Software selectable 1 MHz, 2 MHz, 3.2 MHz, or 6.4 MHz internal bus operation
  - 8-bit trim capability
  - 25% untrimmed
  - Trimmable to approximately 0.4%<sup>(1)</sup>
- Software selectable crystal oscillator range, 32–100 kHz, 1–8 MHz, and 8–32 MHz
- Software configurable input clock from either internal or external source
- Auto wakeup from STOP capability using dedicated internal 32-kHz RC or bus clock source
- FLASH security<sup>(2)</sup>
- On-chip in-application programmable FLASH memory (with internal program/erase voltage generation)

1. See [19.11 Oscillator Characteristics](#) for internal oscillator specifications

2. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

## General Description

- Enhanced serial communications interface (ESCI) module
- Serial peripheral interface (SPI) module
- 4-channel, 16-bit timer interface (TIM1) module
- 2-channel, 16-bit timer interface (TIM2) module
- 10-channel, 10-bit analog-to-digital converter (ADC) with internal bandgap reference channel (ADC10)
- Up to 24 bidirectional input/output (I/O) lines and two input only:
  - Six shared with keyboard interrupt function
  - Ten shared with ADC
  - Four shared with TIM1
  - Two shared with TIM2
  - Two shared with ESCI
  - Four shared with SPI
  - One input only shared with external interrupt (IRQ)
  - High current sink/source capability on all port pins
  - Selectable pullups on all ports, selectable on an individual bit basis
  - Three-state ability on all port pins
- 6-bit keyboard interrupt with wakeup feature (KBI)
  - Programmable for rising/falling edge or high/low level detection
- Low-voltage inhibit (LVI) module features:
  - Software selectable trip point in CONFIG register
- System protection features:
  - Computer operating properly (COP) watchdog
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- External asynchronous interrupt pin with internal pullup ( $\overline{\text{IRQ}}$ ) shared with general-purpose input pin
- Master asynchronous reset pin with internal pullup ( $\overline{\text{RST}}$ ) shared with general-purpose input/output (I/O) pin
- Memory mapped I/O registers
- Power saving stop and wait modes
- MC68HC908QC16, MC68HC908QC8, and MC68HC908QC4 are available in these packages:
  - 28-pin small outline integrated circuit package (SOIC)
  - 28-pin thin shrink small outline package (TSSOP)
  - 20-pin SOIC
  - 20-pin TSSOP
  - 16-pin SOIC
  - 16-pin TSSOP

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast  $8 \times 8$  multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

### 1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908QC16, MC68HC908QC8, and MC68HC908QC4.

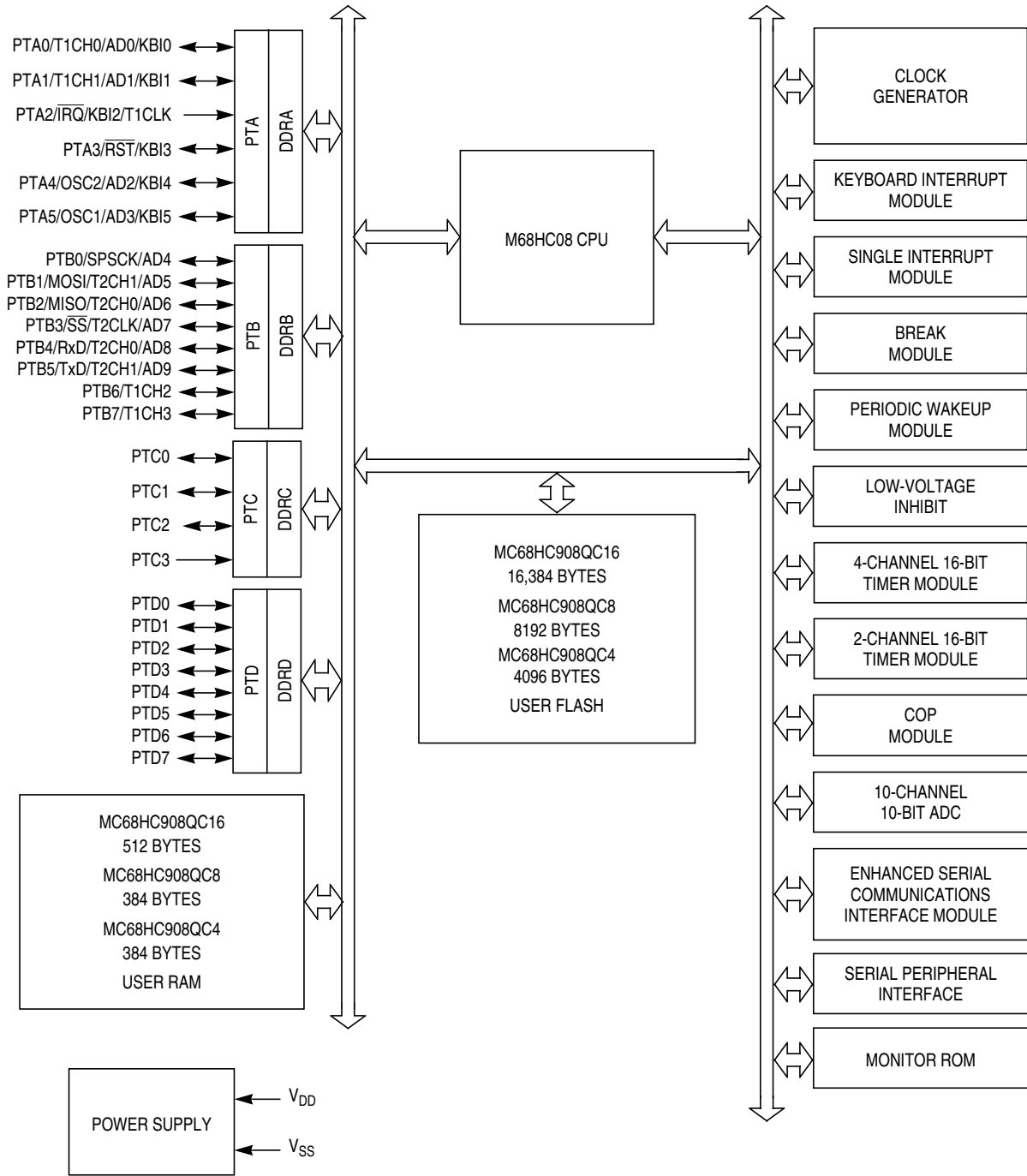
### 1.4 Pin Assignments

The MC68HC908QC16, MC68HC908QC8, and MC68HC908QC4 are available in 16-pin, 20-pin, and 28-pin packages. Figure 1-2 shows the pin assignment for these packages.

### 1.5 Pin Functions

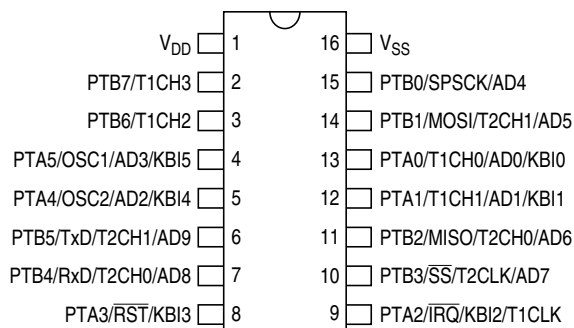
Table 1-2 provides a description of the pin functions.

General Description

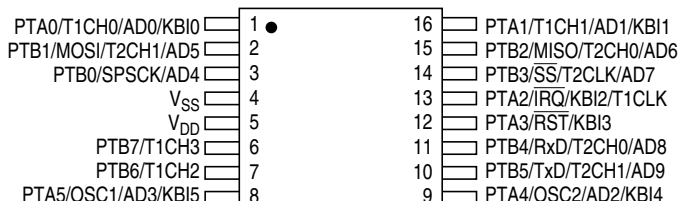


All port pins can be configured with internal pullup  
 PTC not available on 16-pin devices (see note in 11.1 Introduction)  
 PTD not available on 16-pin or 20-pin devices (see note in 11.1 Introduction)

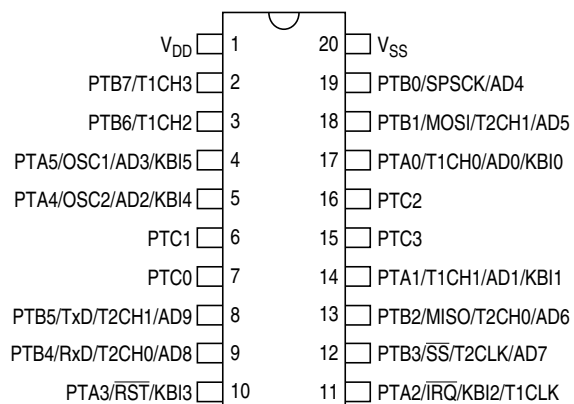
Figure 1-1. Block Diagram



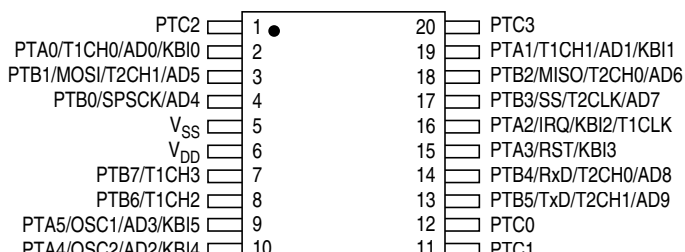
16-PIN ASSIGNMENT  
MC68HC908QCxx SOIC



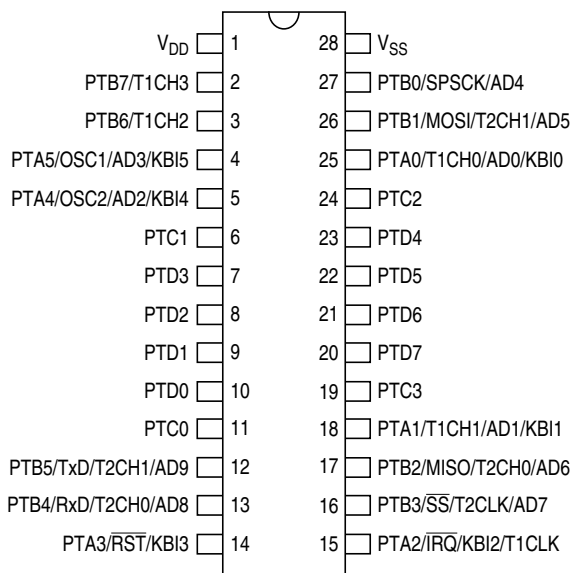
16-PIN ASSIGNMENT  
MC68HC908QCxx TSSOP



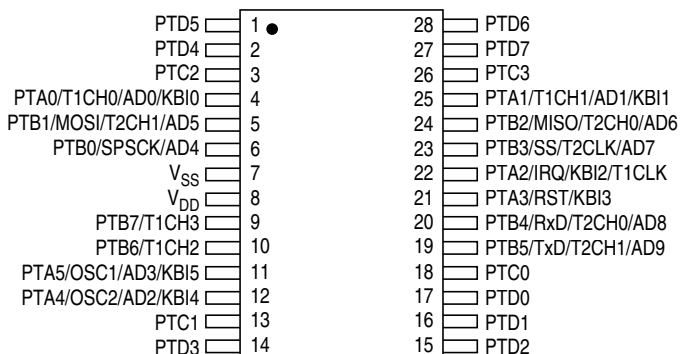
20-PIN ASSIGNMENT  
MC68HC908QCxx SOIC



20-PIN ASSIGNMENT  
MC68HC908QCxx TSSOP



28-PIN ASSIGNMENT  
MC68HC908QCxx SOIC



28-PIN ASSIGNMENT  
MC68HC908QCxx TSSOP

NOTE: T2CH0 and T2CH1 can be repositioned using TIM2POS in CONFIG2.

Figure 1-2. MC68HC908QC16, MC68HC908QC8, and MC68HC908QC4 Pin Assignments

**Table 1-2. Pin Functions**

Pin Name	Description	Input/Output
V <sub>DD</sub>	Power supply	Power
V <sub>SS</sub>	Power supply ground	Power
PTA0	PTA0 — General purpose I/O port	Input/Output
	T1CH0 — Timer Channel 0 I/O	Input/Output
	AD0 — A/D channel 0 input	Input
	KBI0 — Keyboard interrupt input 0	Input
PTA1	PTA1 — General purpose I/O port	Input/Output
	T1CH1 — Timer Channel 1 I/O	Input/Output
	AD1 — A/D channel 1 input	Input
	KBI1 — Keyboard interrupt input 1	Input
PTA2 <sup>(1)</sup>	PTA2 — General purpose input-only port	Input
	IRQ — External interrupt with programmable pullup and Schmitt trigger input	Input
	KBI2 — Keyboard interrupt input 2	Input
	T1CLK — TIM1 timer clock input	Input
PTA3	PTA3 — General purpose I/O port	Input/Output
	RST — Reset input, active low with internal pullup and Schmitt trigger	Input
	KBI3 — Keyboard interrupt input 3	Input
PTA4	PTA4 — General purpose I/O port	Input/Output
	OSC2 — XTAL oscillator output (XTAL option only) RC or internal oscillator output (OSC2EN = 1 in PTAPUE register)	Output Output
	AD2 — A/D channel 2 input	Input
	KBI4 — Keyboard interrupt input 4	Input
PTA5	PTA5 — General purpose I/O port	Input/Output
	OSC1 — XTAL, RC, or external oscillator input	Input
	AD3 — A/D channel 3 input	Input
	KBI5 — Keyboard interrupt input 5	Input
PTB0	PTB0 — General-purpose I/O port	Input/Output
	SPSCK — SPI serial clock	Input/Output
	AD4 — A/D channel 4 input	Input
PTB1	PTB1 — General-purpose I/O port	Input/Output
	MOSI — SPI data transmitted	Input/Output
	T2CH1 <sup>(2)</sup> — TIM2 channel 1	Input/Output
	AD5 — A/D channel 5 input	Input

— Continued on next page



**Table 1-2. Pin Functions (Continued)**

Pin Name	Description	Input/Output
PTB2	PTB2 — General-purpose I/O port	Input/Output
	MISO — SPI data received	Input/Output
	T2CH0 <sup>(2)</sup> — TIM2 channel 0	Input/Output
	AD6 — A/D channel 6 input	Input
PTB3	PTB3 — General-purpose I/O port	Input/Output
	$\overline{SS}$ — SPI slave select	Input
	T2CLK — TIM2 timer clock input	Input
	AD7 — A/D channel 7 input	Input
PTB4	PTB4 — General-purpose I/O port	Input/Output
	RxD — ESCI receive data I/O	Input
	T2CH0 <sup>(2)</sup> — TIM2 channel 0	Input/Output
	AD8 — A/D channel 8 input	Input
PTB5	PTB5 — General-purpose I/O port	Input/Output
	TxD — ESCI transport data I/O	Output
	T2CH1 <sup>(2)</sup> — TIM2 channel 1	Input/Output
	AD9 — A/D channel 9 input	Input
PTB6	PTB6 — General-purpose I/O port	Input/Output
	T1CH2 — Timer channel 2 I/O	Input/Output
PTB7	PTB7 — General-purpose I/O port	Input/Output
	T1CH3 — Timer channel 3 I/O	Input/Output
PTC0–PTC2 <sup>(3)</sup>	General-purpose I/O port	Input/Output
PTC3 <sup>(1, 3)</sup>	General-purpose input port	Input
PTD0–PTD7 <sup>(4)</sup>	General-purpose I/O port	Input/Output

1. PTA2 and PTC3 pins have high voltage detectors to enter special modes.
2. T2CH0 and T2CH1 can be repositioned using TIM2POS in CONFIG2.
3. Pins not available on 16-pin devices (see note in [11.1 Introduction](#)).
4. Pins not available on 16-pin or 20-pin devices (see note in [11.1 Introduction](#)).

## 1.6 Pin Function Priority

Table 1-3 is meant to resolve the priority if multiple functions are enabled on a single pin.

**NOTE**

*Upon reset all pins come up as input ports regardless of the priority table.*

**Table 1-3. Function Priority in Shared Pins**

Pin Name	Highest-to-Lowest Priority Sequence
PTA0 <sup>(1)</sup>	AD0 → T1CH0 → KBI0 → PTA0
PTA1 <sup>(1)</sup>	AD1 → T1CH1 → KBI1 → PTA1
PTA2	$\overline{\text{IRQ}}$ → T1CLK → KBI2 → PTA2
PTA3	$\overline{\text{RST}}$ → KBI3 → PTA3
PTA4 <sup>(1)</sup>	OSC2 → AD2 → KBI4 → PTA4
PTA5 <sup>(1)</sup>	OSC1 → AD3 → KBI5 → PTA5
PTB0 <sup>(1)</sup>	AD4 → SPCK → PTB0
PTB1 <sup>(1)</sup>	AD5 → MOSI → T2CH1 <sup>(2)</sup> → PTB1
PTB2 <sup>(1)</sup>	AD6 → MISO → T2CH0 <sup>(2)</sup> → PTB2
PTB3 <sup>(1)</sup>	AD7 → $\overline{\text{SS}}$ → T2CLK → PTB3
PTB4 <sup>(1)</sup>	AD8 → RxD → T2CH0 <sup>(2)</sup> → PTB4
PTB5 <sup>(1)</sup>	AD9 → TxD → T2CH1 <sup>(2)</sup> → PTB5
PTB6	T1CH2 → PTB6
PTB7	T1CH3 → PTB7
PTCx	PTCx
PTDx	PTDx

1. When a pin is to be used as an ADC pin, the I/O port function should be left as an input and all other shared modules should be disabled. The ADC does not override additional modules using the pin.
2. T2CH0 and T2CH1 can be repositioned using TIM2POS in CONFIG2 (see [Figure 2-2. Control, Status, and Data Registers](#)).

## 1.7 Unused Pin Termination

Input pins and I/O port pins that are not used in the application must be terminated. This prevents excess current caused by floating inputs, and enhances immunity during noise or transient events. Termination methods include:

1. Configuring unused pins as outputs and driving high or low;
2. Configuring unused pins as inputs and enabling internal pull-ups;
3. Configuring unused pins as inputs and using external pull-up or pull-down resistors.

Never connect unused pins directly to  $V_{DD}$  or  $V_{SS}$ .

Since some general-purpose I/O pins are not available on all packages, these pins must be terminated as well. Either method 1 or 2 above are appropriate.