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MC92501

Advance Information

ATM Cell Processor

The MC92501 is an Asynchronous Transfer Mode (ATM) Cell Processor layer device composed of dedicated high-performance ingress and egress cell processors combined with UTOPIA Level 2-compliant physical (PHY) and UTOPIA Level 1-compliant switch interface (see **Figure 1**). It integrates address translation, UPC/ NPC, OAM, and statistical functions into a single semiconductor device. This second generation ATM cell processor in Motorola's MC92500 series can be used both in the line cards used by the switching systems in the ATM network core and in the access multiplexer. The primary function of the MC92501 in either application is to provide ATM-layer cell processing and routing functions. The advanced ATM functionality permits simultaneous tranmission of voice, video, and data within broadband services such as high-speed Internet operations, LAN interconnections for commuters, and video-on-demand using a variety of applications such as Digital Subscriber Line Access Multiplexers (DSLAMs), Wide-Area Networks (WANs), Enterprise Switches, and Multi-service Platforms,

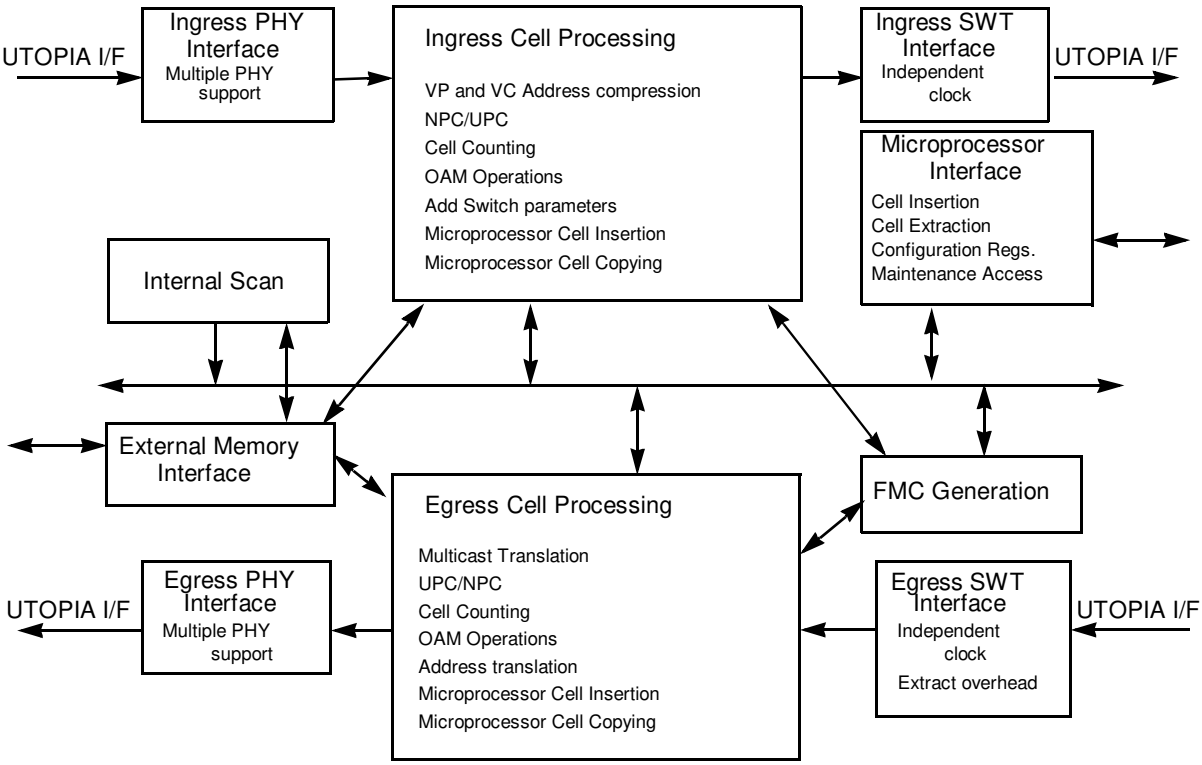

Figure 1. MC92501 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Rev. 2, Feb. 1999 **Preliminary Data**

MOTOROLA

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FOR TECHNICAL ASSISTANCE:

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Email: TBD

Internet: http://www.mot.com/SPS/MCTG/MDAD/atmc

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the RESET pin is active when low.)
asserted	Means that a high true (active high) signal is high or that a low true (active low) signal is low
deasserted	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

New Features in the MC92501

- Implements ATM Layer functions for Broadband ISDN according to ANSI recommendations, ATM Forum UNI 4.0 and TM 4.0 Specifications, ITU recommendations, and Bellcore recommendations.
- Provides ABR Relative Rate marking and EFCI marking according to TM 4.0
- Select Discard CLP = 1 (or CLP = 0 + 1) Flow on selected connections
- UTOPIA Level 2 PHY Interface and UTOPIA ATM Layer Interface
- Supports both Partial Packet Discard (PPD) and Early Packet Discard (EPD)
- Change ABR RM Cell priority
- Supports CLP transparency
- Unidirectional (Ingress or Egress) UPC or NPC

Standard ATMC Features in the MC92500 Family

- Full duplex operation at data rates up to 155 Mbps
- Performs internal VPI and VCI address compression for up to 64 K VCs
- CLP-Aware peak, average, and burst-length policing with programmable Tag/ Drop action per policer
- Supports up to 16 physical links unsing dedicated Ingress/ Egress multiPHY control signals
- Each physical link can be configured as either a UNI or NNI port
- Supports multicast, multiport address translation
- Maintains both virtual connection and physical link counters on both Ingress and Egress cell flows
- Provides a flexible 32-bit external memory port for context management
- Automated AIS, RDI, CC, and loopback functions with performance monitoring block test on all 64 K connections
- Programmable 32-bit microprocessor interface supporting Big-Endian or Little-Endian bus formats
- Unidirectional (Ingress only) UPC or NPC design with up to four leaky buckets per connection
- Supports a programmable number of additional switch overhead parameters allowing adaptiation to any switch routing header format
- Provides per-link cell counters in both directions

Product Documentation

The three documents listed in the following table are required for complete description of the MC92501 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

Table 1. MC92501 Documentation

Name	Description	Order Number
MC92501 Product Brief	MC92501 product overview	MC92501/P
MC92501 Technical Data	MC92501 features list and physical, electrical, timing, and package specifications	MC92501/D
MC92501 User's Manual	Detailed functional description of the MC92501 configuration, operation, and register programming	MC92501UM/D
ATM Cell Processor Evaluation Board User's Manual	Detailed description of the ATMC EVB hardware, operation, installation, and design recommendations	MC92501EVKUM/D

1

Signal Descriptions

1.1 Signal Groupings

The input and output signals of the MC92501 are organized into functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**. The MC92501 is operated from a 3.3 V supply; however, some of the inputs can tolerate 5 V. A special note for this feature is added to the signal descriptions of those inputs.

Table 1-1. MC92501 Functional Signal Groupings

Functional Group	Number of Signals	Detailed Description
Power (VDD and AVDD) and Ground (VSS and AVSS)	47	**Table 1-2**
Control	4	**Table 1-3**
Processor Interface	68	**Table 1-4**
Ingress PHY Interface	17	**Table 1-6**
Egress PHY Interface	18	**Table 1-7**
PLL	4	**Table 1-8**
External Memory Interface	64	**Table 1-9**
Ingress Switch Interface	13	**Table 1-10**
Egress Switch Interface	13	**Table 1-11**
JTAG Interface	5	**Table 1-12**

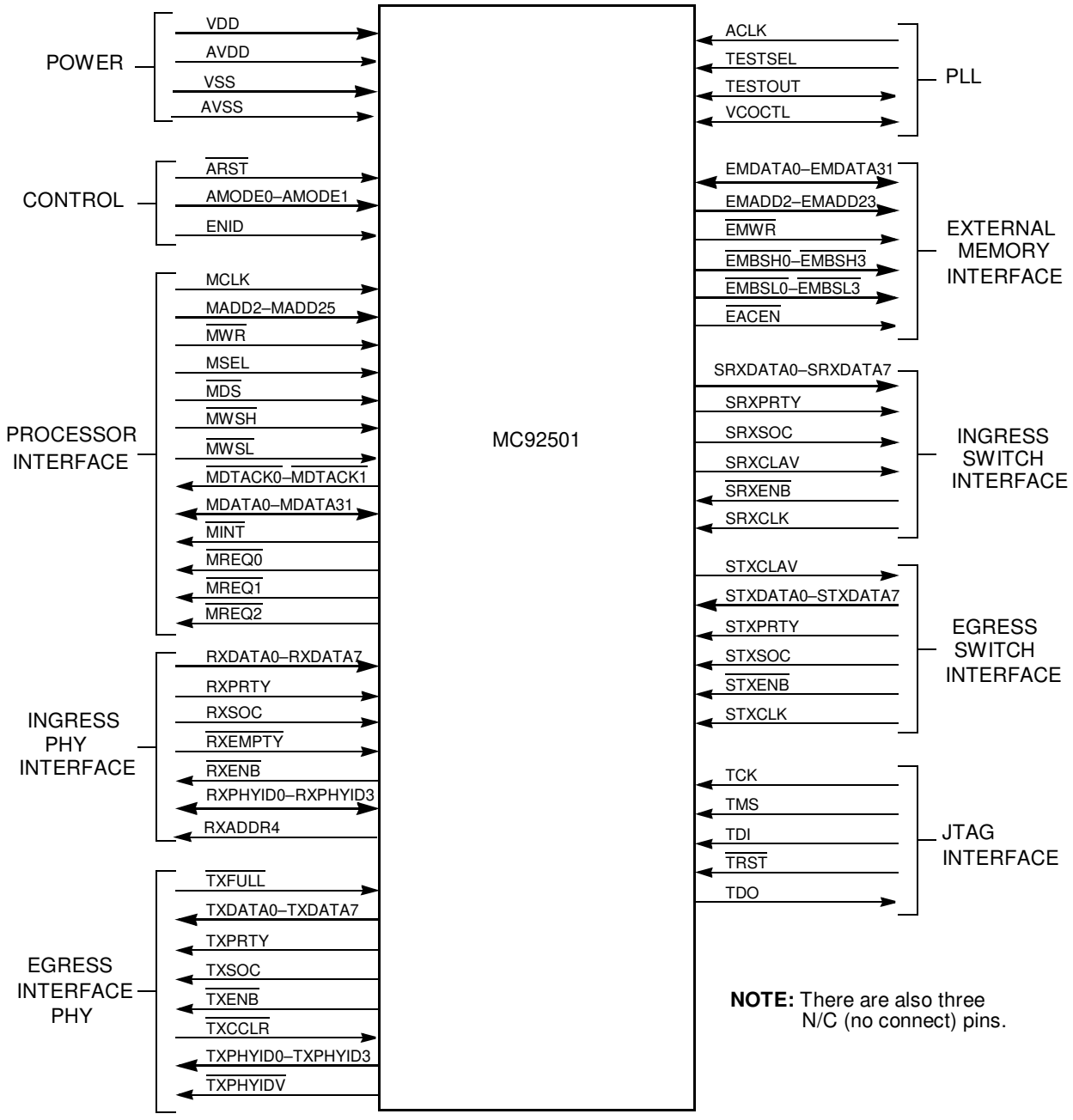


Figure 1-1. Functional Signal Groups

1.2 Power and Ground Signals

Table 1-2. Power and Ground Signals

Signal Name	Description
VDD	**Input Power**
AVDD	**PLL Analog Power**—Isolate this input to eliminate coupling of digital switching noise into the PLL
VSS	**System Ground**
AVSS	**PLL Analog Ground**—Isolate this input to eliminate coupling of digital switching noise into the PLL

1.3 Control Signals

Table 1-3. Control Signals

Signal Name	Signal Type	Detailed Description
$\overline{\text{ARST}}$	Input	**ATMC Power-up Reset**—This input signal is used for power-up reset of the entire chip. It must be asserted for at least the time required by the PLL to stabilize.
AMODE0–AMODE1	Input	**ATMC Mode**—These input signals determine the operating mode of the chip's test features. In normal usage these pins should be grounded.
ENID	Input	**Enable IDD**—This input pin is used for test purposes. In normal usage the ENID pin must be grounded.

Note: All inputs are 5 V tolerant.

1.4 Processor Interface Signals

Table 1-4. Processor Interface Signals

Signal Name	Signal Type	Detailed Description
MCLK	Input	**MP Clock**—This input signal is used as the Microprocessor clock inside the MC92501. This signal drives the microprocessor logic in the MC92501. The duty cycle should be in the range of 40–60%.
MADD2–MADD25	Input	**MP Address Bus**—This input bus contains the address which is used by the microprocessor to define the register being accessed. This bus is used by the MC92501 at the assertion of MSEL and sampled on the falling edge of MCLK.
$\overline{\text{MWR}}$	Input	**MP Write**—This input signal is used to determine whether the MP is reading from the MC92501 or writing to it. This signal is sampled by the MC92501 on the falling edge of MCLK. The MC92501 drives MDATA when $\overline{\text{MSEL}}$ = 0 and $\overline{\text{MWR}}$ = 1.
MSEL	Input	**MP Select**—This input signal is used to determine that the current access to the MC92501 is valid. This signal is sampled by the MC92501 on the falling edge of MCLK.
MDS	Input	**MP Data Select**—This input signal is used to indicate when the data on MDATA is valid during a write access to the MC92501. This signal is sampled by the MC92501 on the falling edge of MCLK.
MWSH	Input	**MP Word Write Enable High**—This signal indicates that the high word is being written. During a maintenance write access, the value detected on $\overline{\text{MWSH}}$/A1 is driven on the appropriate $\overline{\text{EMBSH}}$ signal. During read access $\overline{\text{EMBSH}}$ signal is always asserted.
A1	Input	**Address 1**—When configured appropriately during a maintenance write access, this signal serves as Address 1. During a read access, this signal is ignored. **Note:** This input signal is programmed by the *Word Select Signals Mode (WSSM)* bit in the Microprocessor Configuration Register (MPCONR). The signal is sampled by the MC92501 on the falling edge of MCLK. **Table 1-5** describes the combined MWSH/A1 and MWSL/Size functionality
MWSL	Input	**MP Word Write Enable Low**—This signal indicates that the high word is being written. During a maintenance write access, the value detected on $\overline{\text{MWSL}}$/SIZE is driven on the appropriate $\overline{\text{EMBSL}}$ signal. During read access $\overline{\text{EMBSL}}$ signal is always asserted.
SIZE	Input	**Access Size**—When configured appropriately during a maintenance write access, this signal indicates the size of the maintenance write access: either 32 bits or 16 bits access. During a read access, this signal is ignored and the access width is 32 bits. **Note:** This input signal is programmed by the *Word Select Signals Mode (WSSM)* bit in the Microprocessor Configuration Register (MPCONR). The signal is sampled by the MC92501 on the falling edge of MCLK. **Table 1-5** describes the combined MWSH/A1 and MWSL/Size functionality

Table 1-4. Processor Interface Signals (Continued)

Signal Name	Signal Type	Detailed Description
MDTACK0–MDTACK1	Output	**MP Data Acknowledge 0–1**—These tri-statable output signals are used to indicate the end of an access from the MC92501. At the end of each access, this signal is actively pulled up and then released. The user may program the MC92501 not to drive this signal during certain types of accesses. This signal is output asynchronously to MCLK.
MDATA0–MDATA31	Input/Output	**MP Data Bus**—This tri-state bidirectional bus provides the general data path between the MC92501 and the microprocessor.
MINT	Output	**MP Interrupt**—This output signal is used to notify the microprocessor of the occurrence of interrupting events. This signal is asserted on the rising edge of ACLK (asynchronous with respect to MCLK).
$\overline{\text{MREQ0}}$	Output	**MP Request 0**—This output signal can be programmed to one of three options (described below in note 2). Its default value is option #1: MP Cell In Request ($\overline{\text{MCIREQ}}$).
$\overline{\text{MREQ1}}$	Output	**MP Request 1**—This output signal can be programmed to one of three options (described below in note 2). Its default value is option #2: MP Cell Out Request ($\overline{\text{MCOREQ}}$)..
$\overline{\text{MREQ2}}$	Output	**MP Request 2**—This output signal can be programmed to one of of three options (described below in note 2). Its default value is option #3: External Memory Maintenance Request ($\overline{\text{EMMREQ}}$).

Notes: 1. All inputs are 5 V tolerant.

2. $\overline{\text{MREQ0}}$, $\overline{\text{MREQ1}}$ and $\overline{\text{MREQ2}}$ signals are fully backward compatible to the MC92501 Revision A $\overline{\text{MCIREQ}}$, $\overline{\text{MCOREQ}}$ and $\overline{\text{EMMREQ}}$ signals, respectively. The $\overline{\text{MREQ}}$[n] signals are used by DMA devices and can be programmed to support DMA requests as follows:

— *MP Cell In Request*: $\overline{\text{MREQ}}$[n] is an output signal that can be used by an external DMA device as a control line indicating when to start a new cell insertion cycle into the MC92501. It is asserted whenever the Cell Insertion Register array is available to be written. This signal is output on the falling edge of MCLK.

— *MP Cell Out Request*: $\overline{\text{MREQ}}$[n] is an output signal may be used by an external DMA device as a control line indicating when to start a new cell extraction cycle from the MC92501. It is asserted whenever the Cell Extraction Register array is available to be read. It is output on the falling edge of MCLK.

— *External Memory Maintenance Request*: $\overline{\text{MREQ}}$[n] is an output signal is asserted a programmable number of clock cycles before the start of an External Memory maintenance cycle. It is deasserted after a programmable number of maintenance accesses have been performed. It is output on the falling edge of MCLK.

Table 1-5. Host Interface Fields

WSSM = 0		*WSSM* = 1 and DO-Data Order = 0		*WSSM* = 1 and DO-Data Order=1		Function
$\overline{\text{MWSH}}$	$\overline{\text{MWSL}}$	A1	Size	A1	Size	
0	0	x	0	x	0	Write D(31:0)
0	1	0	1	1	1	Write D(31:16)
1	0	1	1	0	1	Write D(15:00)

Note: All Cell Extraction Register, Cell Insertion Register, and General Register accesses are long-word (32-bit) accesses, so both $\overline{\text{MWSH}}$/A1 and $\overline{\text{MWSL}}$/SIZE should be asserted low for these write accesses when write-enable mode is selected.

1.5 Ingress PHY Interface Signals

Table 1-6. Ingress PHY Interface Signals

Signal Name	Signal Type	Detailed Description
RXDATA0–RXDATA7	Input	**Receive Data Bus**—This input data bus receives octets from the PHY chip. When $\overline{\text{RXENB}}$ is active, RXDATA is sampled into the MC92501.
RXPRTY	Input	**Receive Data Bus Parity (RXPRTY)**—This input is the odd parity over RXDATA. This input is ignored if $\overline{\text{RXENB}}$ is not active or the parity check is disabled.
RXSOC	Input	**Receive Start Of Cell (RXSOC)**—This input, when high, indicates that the current RXDATA is the first byte of a cell. This input is sampled when $\overline{\text{RXENB}}$ is active.
$\overline{\text{RXEMPTY}}$	Input	**Receive PHY Empty**—This input, when low, indicates that currently the PHY chip has no available data.
$\overline{\text{RXENB}}$	Output	**Receive Enable**—This output, when low, indicates that the MC92501 is ready to receive data.
RXPHYID0–RXPHYID3	Input	**Receive PHY Device ID Bus 0–3**—In UTOPIA level 1, this is an input bus that indicates the ID number of the PHY device currently transferring data to the MC92501. If only a single PHY device is supported, this bus should be tied low. This bus is sampled along with the first octet of each cell.
RXADDR0–RXADDR3	Output	**Receive Address 0–3**—In UTOPIA Level 2, this is an output bus that indicates the 4 least significant bits of the ID number of the PHY device which is being polled or selected by the MC92501.
RXADDR4	Output	**Receive Address 4**—This signal is an output signal that indicates the most significant bit of the ID number of the PHY device that is being polled or selected by the MC92501.

Note: All inputs are 5 V tolerant.

1.6 Egress PHY Interface Signals

Table 1-7. Egress PHY Interface Signals

Signal Name	Signal Type	Detailed Description
$\overline{\text{TXFULL}}$	Input	**Transmit PHY Full**—This input signal indicates, when low, that the PHY device is full.
TXDATA0–TXDATA7	Output	**Transmit Data Bus**—This output data bus transmits octets to the PHY chip. When $\overline{\text{TXENB}}$ is active, TXDATA contains a valid octet for the PHY.
TXPRTY	Output	**Transmit Data Bus Parity**—This output signal is the odd parity over TXDATA. When $\overline{\text{TXENB}}$ is active, TXPRTY is a valid parity bit for the PHY.
TXSOC	Output	**Transmit Start Of Cell**—This output signal indicates, when high, that the current data on TXDATA is the first byte of a cell. TXSOC is valid when $\overline{\text{TXENB}}$ is asserted.
$\overline{\text{TXENB}}$	Output	**Transmit Enable**—This output signal, when low, indicates that TXDATA, TXPRTY, and TXSOC are valid data for the PHY.
$\overline{\text{TXCCLR}}$	Input	**Transmit Cell Clear**—This input signal indicates, when low, that the current cell should be cleared from the Egress PHY interface.
TXPHYID0–TXPHYID3	Output	**Transmit PHY ID 0–3—**In UTOPIA level 1, this is an output bus that indicates the ID number of the PHY device to which either the current cell or the next cell is directed. The functionality is controlled by the MC92501 General Configuration Register (GCR).
TXADDR0—TXADDR3	Output	**Transmit Address 0–3—**In UTOPIA level 2, this is an output bus that indicates the 4 least significant bits of the ID number of the PHY device which is being polled or selected by the MC92501.
$\overline{\text{TXPHYIDV}}$	Output	**Transmit Next PHY ID Valid**—In UTOPIA level 1, this is an output signal that, when low, indicates that TXPHYID (when configured as the next cell's ID) is valid. If TXPHYID is configured to refer to the current cell, $\overline{\text{TXPHYIDV}}$ is not used.
TXADDR4	Output	**Transmit Address 4**—In UTOPIA level 2, this an output signal that indicates the most significant bit of the ID number of the PHY device which is being polled or selected by the MC92501.

Note: All inputs are 5 V tolerant.

1.7 PLL Signals

Table 1-8. PLL Signals

Signal Name	Signal Type	Detailed Description
ACLK	Input	**ATMC Master Clock**—This input signal is used by the PLL to generate the internal master clock of MC92501. The duty cycle should be in the range of 40–60%.
TESTSEL	Input	This is a dedicated test signal that must be grounded during normal system operation.
TESTOUT	Input/Output	This is a dedicated test signal that must be connected to the analog ground (AVSS) during normal system operation.
VCOCTL	Input/Output	This is a dedicated test signal that must be connected to the analog ground (AVSS) during normal system operation.

Note: All inputs are 5 V tolerant.

1.8 External Memory Interface Signals

Table 1-9. External Memory Interface Signals

Signal Name	Signal Type	Detailed Description
EMDATA0–EMDATA31	Input/Output	**External Memory Data Bus**—This tri-statable bidirectional bus is the data path between the MC92501 and External Memory.
EMADD2–EMADD23	Output	**External Memory Address Bus**—This output bus is the general address bus used by the MC92501 to access the External Memory.
$\overline{\text{EMWR}}$	Output	**External Memory Write**—When asserted (low), this output signal indicates that the current cycle to the External Memory is a write cycle. This signal is asserted within the cycle.
$\overline{\text{EMBSH0}}$–EMBSH3	Output	**External Memory Bank Select High**—These output signals are used to select the high word of the appropriate memory bank. One or more of these signals is asserted for each External Memory access according to the value of EMADD. During a maintenance write access from the microprocessor, the value detected on MWSH is driven on the appropriate $\overline{\text{EMBSH}}$ signal.
$\overline{\text{EMBSL0}}$–EMBSL3	Output	**External Memory Bank Select Low**—These output signals are used to select the low word of the appropriate memory bank. One or more of these signals is asserted for each External Memory access according to the value of EMADD. During a maintenance write access from the microprocessor, the value detected on $\overline{\text{MWSL}}$ is driven on the appropriate $\overline{\text{EMBSL}}$ signal.

Table 1-9. External Memory Interface Signals (Continued)

Signal Name	Signal Type	Detailed Description
$\overline{\text{EACEN}}$	Output	**External Address Compression Enable**—This output signal is asserted when data is being written to or read from an external address compression device using the External Memory Data Bus.

Note: All inputs are 5 V tolerant.

1.9 Ingress Switch Interface Signals

Table 1-10. Ingress Switch Interface Signals

Signal Name	Signal Type	Detailed Description
SRXDATA0–SRXDATA7	Output	**Receive DATA BUS (SRXDATA0-SRXDATA7)**—This three-state output data bus transmits bytes to the switch. When $\overline{\text{SRXENB}}$ is active, SRXDATA contains valid data for the switch. This bus is updated on the rising edge of SRXCLK.
SRXPRTY	Output	**Receive Data Bus Parity**—This three-state output is the parity protection of SRXDATA transmitted to the switch. The type of parity (even/odd) is defined by the Ingress Switch Interface Configuration Register (ISWCR)..
SRXSOC	Output	**Receive Start Of Cell**—This three-state output, when high, indicates that the current data on SRXDATA is the first byte of a cell structure (including the overhead bytes).
SRXCLAV	Output	**Receive Switch Cell Available**—This output, when asserted, indicates that the MC92501 has a cell ready to transfer to the switch. When deasserted, it indicates that currently there is no data available for the switch.
$\overline{\text{SRXENB}}$	Input	**Receive Enable**—This input, when low, enables new values on SRXDATA, SRXPRTY and SRXSOC.
SRXCLK	Input	**Receive Clock**—This input is used to clock the Ingress switch interface signals.

Note: All inputs are 5 V tolerant.

1.10 Egress Switch Interface Signals

Table 1-11. Egress Switch Interface Signals

Signal Name	Signal Type	Detailed Description
STXCLAV	Output	**Transmit Cell Available**—This output, when asserted, indicates that the MC92501 is prepared to receive a complete cell.
STXDATA0–STXDATA7	Input	**Transmit Data Bus**—This input data bus receives bytes from the switch. When STXENB is asserted, STXDATA is sampled into the MC92501 on the rising edge of STXCLK.
STXPRTY	Input	**Transmit Data Bus Parity**—This input is the parity over STXDATA. The type of parity (even/odd) and the parity check control are defined by the Egress Switch Interface Configuration Register (ESWCR). This input is ignored if STXENB is deasserted or the parity check is disabled. It is sampled on the rising edge of STXCLK.
STXSOC	Input	**Transmit Start Of Cell**—This input indicates, when high, that the current data is the first byte of a cell structure (including the overhead bytes). This input is sampled on the rising edge of STXCLK when STXENB is asserted.
$\overline{\text{STXENB}}$	Input	**Transmit Enable**—This input, when low, enables STXDATA, STXPRTY, and STXSOC.
STXCLK	Input	**Transmit Clock**—This input signal is used to clock the Egress switch interface signals.

Note: All inputs are 5 V tolerant.

1.11 JTAG Interface Signals

Table 1-12. JTAG Interface Signals

Signal Name	Signal Type	Detailed Description
TCK	Input	**Test Clock**—This input pin is the JTAG clock. The TDO, TDI, and TMS pins are synchronized by this signal.
TMS	Input	**Test Mode Select**—This input signal is sampled on the rising edge of TCK. TMS is responsible for the state change in the test access port state machine.
TDI	Input	**Test Data Input**—This input signal is sampled on the rising edge of TCK. TDI is the data to be shifted toward the TDO output.
$\overline{\text{TRST}}$	Input	**Test Reset**—This input signal is the JTAG asynchronous reset. When asserted low, the Test Access Port is forced to the Test_Logic_Reset state. When JTAG is not being used, this signal should be hard-wired to GND or tied to ARST.
TDO	Output	**Test Data Output**—This tri-state output changes its logical value on the falling edge of TCK.

Note: All inputs are 5 V tolerant.

2

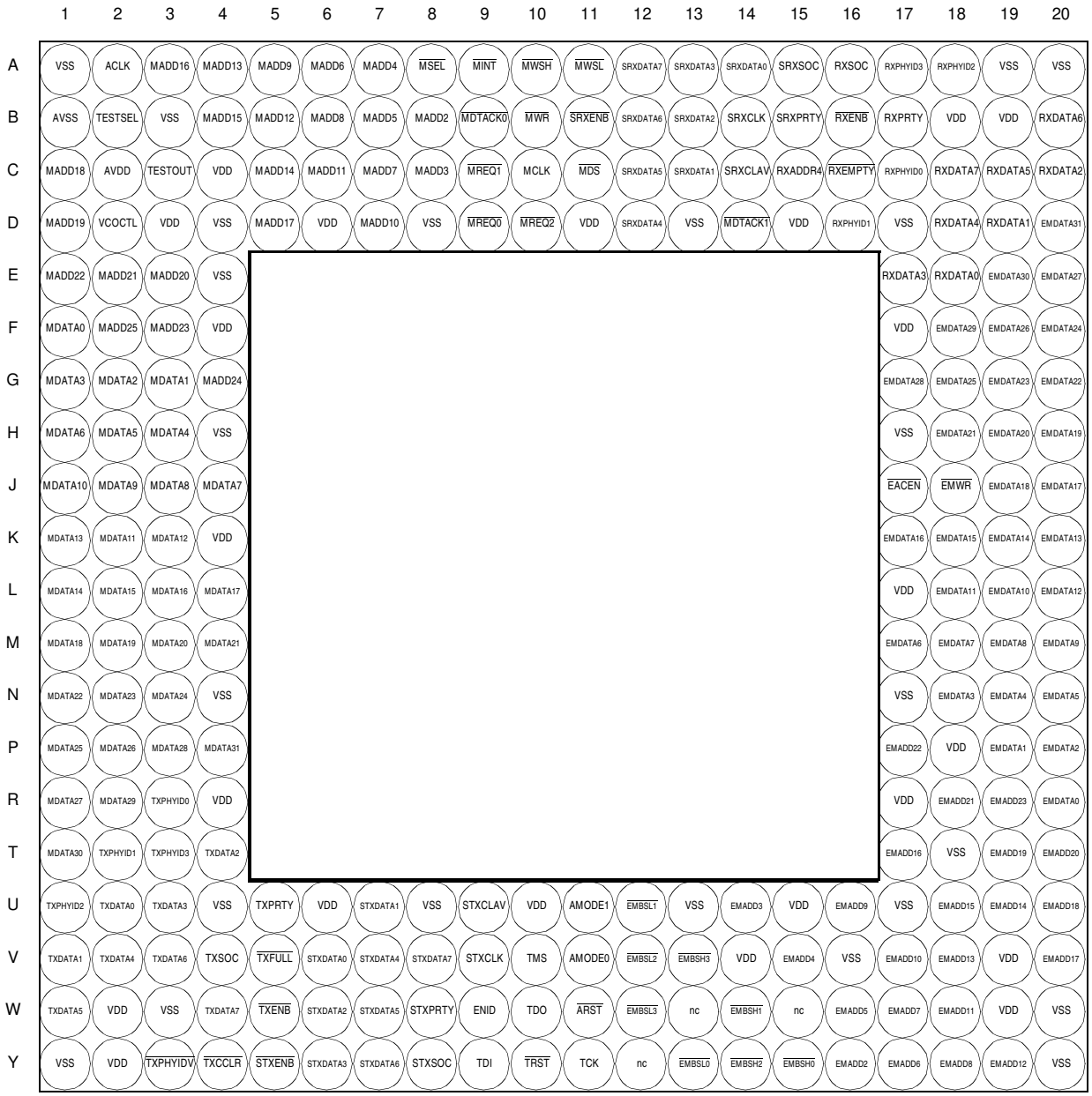
Signal and Packaging Information

2.1 Introduction

This section provides information on packaging, including a diagram of the package with signals and tables showing how the signals described in **Section 1** are allocated. The MC92501 is available in a 256-lead Glob-Top Ball Grid Array (GTBGA) package. The package mechanical drawing is provided at the end of this section.

2.2 GTBGA Package Description

A GTBGA package top view is shown in **Figure 2-1** with signal and location designators.



Notes: **1.** Locations marked as *nc* must not be connected.

2. The figure only shows the primary signal name for each lead. For the Ingress and Egress PHY Interface signals, the primary signal names are those used in UTOPIA Level 1. For UTOPIA Level 2, leads A17, A18, C17, and D16 change to RXADDR3, RXADDR2, RXADDR0, and RXADDR1, respectively. Leads R3, T2, T3, U1, and Y3 change to TXADDR0, TXADDR1, TXADDR3, TXADDR2, and TXADDR4, respectively. The Microprocessor signals also have an alternate configuration that changes leads A10 and A11 to signals A1 and SIZE, respectively.

Figure 2-1. MC92501 256-Lead GTBGA Diagram (Top View)

Table 2-1. MC92501 256-Lead GTBGA Package Signal List by Location

Location	Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name
A1	VSS	B1	AVSS	C1	MADD18	D1	MADD19
A2	ACLK	B2	TESTSEL	C2	AVDD	D2	VCOCTL
A3	MADD16	B3	VSS	C3	TESTOUT	D3	VDD
A4	MADD13	B4	MADD15	C4	VDD	D4	VSS
A5	MADD9	B5	MADD12	C5	MADD14	D5	MADD17
A6	MADD6	B6	MADD8	C6	MADD11	D6	VDD
A7	MADD4	B7	MADD5	C7	MADD7	D7	MADD10
A8	$\overline{\text{MSEL}}$	B8	MADD2	C8	MADD3	D8	VSS
A9	$\overline{\text{MINT}}$	B9	$\overline{\text{MDTACK0}}$	C9	$\overline{\text{MREQ1}}$	D9	$\overline{\text{MREQ0}}$
A10	$\overline{\text{MWSH}}$/A1	B10	$\overline{\text{MWR}}$	C10	MCLK	D10	$\overline{\text{MREQ2}}$
A11	$\overline{\text{MWSL}}$/SIZE	B11	$\overline{\text{SRXENB}}$	C11	$\overline{\text{MDS}}$	D11	VDD
A12	SRXDATA7	B12	SRXDATA6	C12	SRXDATA5	D12	SRXDATA4
A13	SRXDATA3	B13	SRXDATA2	C13	SRXDATA1	D13	VSS
A14	SRXDATA0	B14	SRXCLK	C14	SRXCLAV	D14	$\overline{\text{MDTACK1}}$
A15	SRXSOC	B15	SRXPRTY	C15	RXADDR4	D15	VDD
A16	RXSOC	B16	$\overline{\text{RXENB}}$	C16	$\overline{\text{RXEMPTY}}$	D16	RXPHYID1/ RXADDR1
A17	RXPHYID3/ RXADDR3	B17	RXPRTY	C17	RXPHYID0/ RXADDR0	D17	VSS
A18	RXPHYID2/ RXADDR2	B18	VDD	C18	RXDATA7	D18	RXDATA4
A19	VSS	B19	VDD	C19	RXDATA5	D19	RXDATA1
A20	VSS	B20	RXDATA6	C20	RXDATA2	D20	EMDATA31

Table 2-1. MC92501 256-Lead GTBGA Package Signal List by Location (Continued)

Location	Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name
E1	MADD22	H1	MDATA6	L1	MDATA14	P1	MDATA25
E2	MADD21	H2	MDATA5	L2	MDATA15	P2	MDATA26
E3	MADD20	H3	MDATA4	L3	MDATA16	P3	MDATA28
E4	VSS	H4	VSS	L4	MDATA17	P4	MDATA31
E17	RXDATA3	H17	VSS	L17	VDD	P17	EMADD22
E18	RXDATA0	H18	EMDATA21	L18	EMDATA11	P18	VDD
E19	EMDATA30	H19	EMDATA20	L19	EMDATA10	P19	EMDATA1
E20	EMDATA27	H20	EMDATA19	L20	EMDATA12	P20	EMDATA2
F1	MDATA0	J1	MDATA10	M1	MDATA18	R1	MDATA27
F2	MADD25	J2	MDATA9	M2	MDATA19	R2	MDATA29
F3	MADD23	J3	MDATA8	M3	MDATA20	R3	TXPHYID0/ TXADDR0
F4	VDD	J4	MDATA7	M4	MDATA21	R4	VDD
F17	VDD	J17	$\overline{\text{EACEN}}$	M17	EMDATA8	R17	VDD
F18	EMDATA29	J18	$\overline{\text{EMWR}}$	M18	EMDATA7	R18	EMADD21
F19	EMDATA26	J19	EMDATA18	M19	EMDATA8	R19	EMADD23
F20	EMDATA24	J20	EMDATA17	M20	EMDATA9	R20	EMDATA0
G1	MDATA3	K1	MDATA13‘	N1	MDATA22	T1	MDATA30
G2	MDATA2	K2	MDATA11	N2	MDATA23	T2	TXPHYID1/ TXADDR1
G3	MDATA1	K3	MDATA12	N3	MDATA24	T3	TXPHYID3/ TXADDR3
G4	MADD24	K4	VDD	N4	VSS	T4	TXDATA2
G17	EMDATA28	K17	EMDATA16	N17	VSS	T17	EMADD16
G18	EMDATA25	K18	EMDATA15	N18	EMDATA3	T18	VSS
G19	EMDATA23	K19	EMDATA14	N19	EMDATA4	T19	EMADD19
G20	EMDATA22	K20	EMDATA13	N20	EMDATA5	T20	EMADD20

Table 2-1. MC92501 256-Lead GTBGA Package Signal List by Location (Continued)

Location	Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name
U1	TXPHYID2/ TXADDR2	V1	TXDATA1	W1	TXDAT5	Y1	VSS
U2	TXDATA0	V2	TXDATA4	W2	VDD	Y2	VDD
U3	TXDATA3	V3	TXDATA6	W3	VSS	Y3	$\overline{\text{TXPHYIDV}}$/ TXADDR4
U4	VSS	V4	TXSOC	W4	TXDATA7	Y4	$\overline{\text{TXCCLR}}$
U5	TXPRTY	V5	$\overline{\text{TXFULL}}$	W5	$\overline{\text{TXENB}}$	Y5	$\overline{\text{STXENB}}$
U6	VDD	V6	STXDATA0	W6	STXDATA2	Y6	STXDATA3
U7	STXDATA1	V7	STXDATA4	W7	STXDATA5	Y7	STXDATA6
U8	VSS	V8	STXDATA7	W8	STXPRTY	Y8	STXSOC
U9	STXCLAV	V9	STXCLK	W9	ENID	Y9	TDI
U10	VDD	V10	TMS	W10	TDO	Y10	$\overline{\text{TRST}}$
U11	AMODE1	V11	AMODE0	W11	$\overline{\text{ARST}}$	Y11	TCK
U12	$\overline{\text{EMBSL1}}$	V12	$\overline{\text{EMBSL2}}$	W12	$\overline{\text{EMBSL3}}$	Y12	nc
U13	VSS	V13	$\overline{\text{EMBSH3}}$	W13	nc	Y13	$\overline{\text{EMBSL0}}$
U14	EMADD3	V14	VDD	W14	$\overline{\text{EMBSH1}}$	Y14	$\overline{\text{EMBSH2}}$
U15	VDD	V15	EMADD4	W15	nc	Y15	$\overline{\text{EMBSH0}}$
U16	EMADD9	V16	VSS	W16	EMADD5	Y16	EMADD2
U17	VSS	V17	EMADD10	W17	EMADD7	Y17	EMADD6
U18	EMADD15	V18	EMADD13	W18	EMADD11	Y18	EMADD8
U19	EMADD14	V19	VDD	W19	VDD	Y19	EMADD12
U20	EMADD18	V20	EMADD17	W20	VSS	Y20	VSS

Table 2-2. MC92501 256-Lead GTBGA Package Signal List by Name

Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name	Location
A1	A10	EMADD21	R18	EMDATA10	L19	EMDATA29	F18
ACLK	A2	EMADD22	P17	EMDATA11	L18	EMDATA3	N18
AMODE0	V11	EMADD23	R19	EMDATA12	L20	EMDATA30	E19
AMODE1	U11	EMADD3	U14	EMDATA13	K20	EMDATA31	D20
$\overline{\text{ARST}}$	W11	EMADD4	V15	EMDATA14	K19	EMDATA4	N19
AVDD	C2	EMADD5	W16	EMDATA15	K18	EMDATA5	N20
AVSS	B1	EMADD6	Y17	EMDATA16	K17	EMDATA7	M18
$\overline{\text{EACEN}}$	J17	EMADD7	W17	EMDATA17	J20	EMDATA8	M17
EMADD10	V17	EMADD8	Y18	EMDATA18	J19	EMDATA8	M19
EMADD11	W18	EMADD9	U16	EMDATA19	H20	EMDATA9	M20
EMADD12	Y19	$\overline{\text{EMBSH0}}$	Y15	EMDATA2	P20	$\overline{\text{EMWR}}$	J18
EMADD13	V18	$\overline{\text{EMBSH1}}$	W14	EMDATA20	H19	ENID	W9
EMADD14	U19	$\overline{\text{EMBSH2}}$	Y14	EMDATA21	H18	MADD10	D7
EMADD15	U18	$\overline{\text{EMBSH3}}$	V13	EMDATA22	G20	MADD11	C6
EMADD16	T17	$\overline{\text{EMBSL0}}$	Y13	EMDATA23	G19	MADD12	B5
EMADD17	V20	$\overline{\text{EMBSL1}}$	U12	EMDATA24	F20	MADD13	A4
EMADD18	U20	$\overline{\text{EMBSL2}}$	V12	EMDATA25	G18	MADD14	C5
EMADD19	T19	$\overline{\text{EMBSL3}}$	W12	EMDATA26	F19	MADD15	B4
EMADD2	Y16	EMDATA0	R20	EMDATA27	E20	MADD16	A3
EMADD20	T20	EMDATA1	P19	EMDATA28	G17	MADD17	D5

Table 2-2. MC92501 256-Lead GTBGA Package Signal List by Name (Continued)

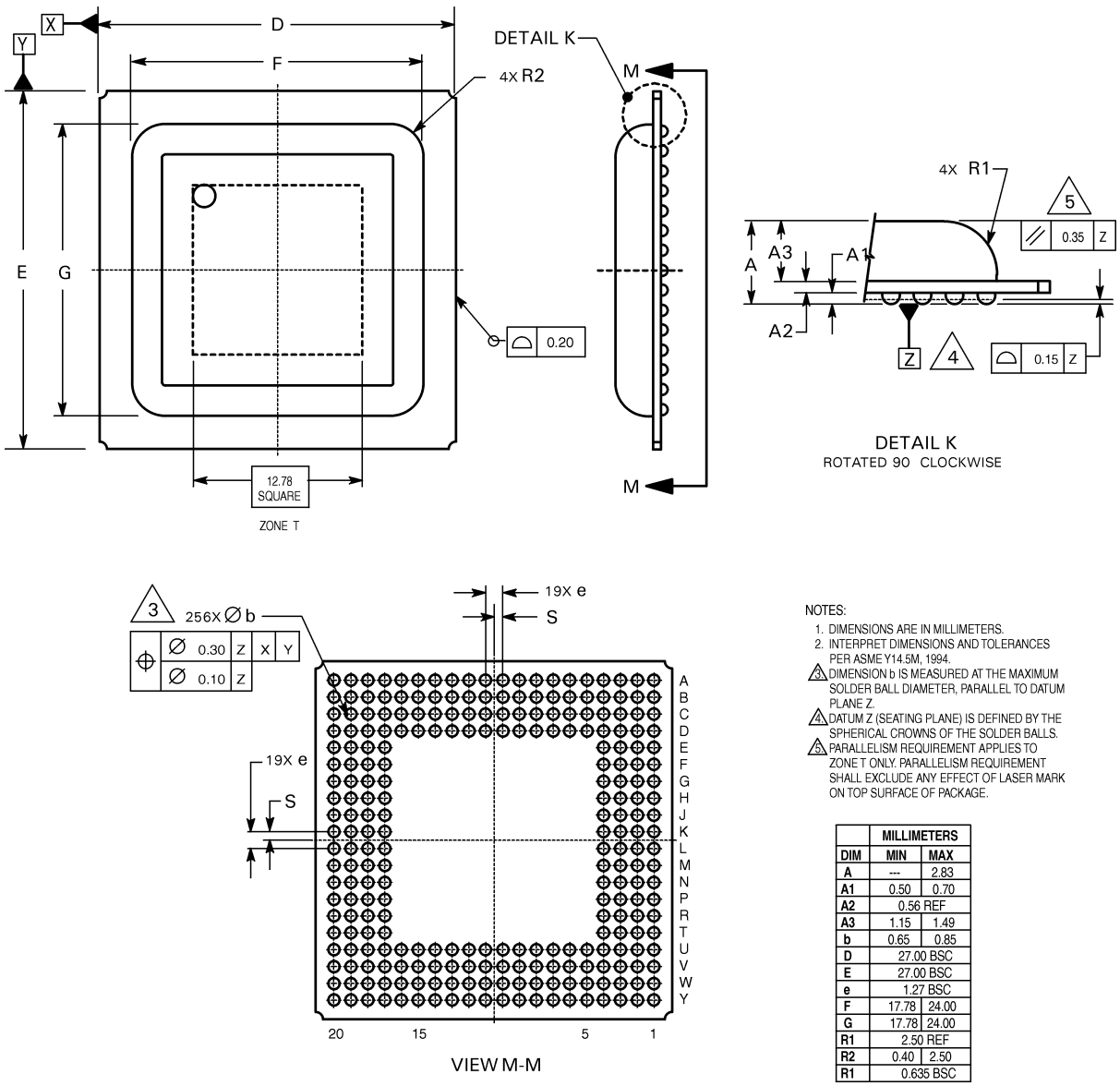
Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name	Location
MADD18	C1	MDATA16	L3	$\overline{\text{MDTACK0}}$	B9	RXDATA7	C18
MADD19	D1	MDATA17	L4	$\overline{\text{MDTACK1}}$	D14	$\overline{\text{RXEMPTY}}$	C16
MADD2	B8	MDATA18	M1	$\overline{\text{MINT}}$	A9	$\overline{\text{RXENB}}$	B16
MADD20	E3	MDATA19	M2	$\overline{\text{MREQ0}}$	D9	RXPHYID0	C17
MADD21	E2	MDATA2	G2	$\overline{\text{MREQ1}}$	C9	RXPHYID1	D16
MADD22	E1	MDATA20	M3	$\overline{\text{MREQ2}}$	D10	RXPHYID2	A18
MADD23	F3	MDATA21	M4	$\overline{\text{MSEL}}$	A8	RXPHYID3	A17
MADD24	G4	MDATA22	N1	$\overline{\text{MWR}}$	B10	RXPRTY	B17
MADD25	F2	MDATA23	N2	$\overline{\text{MWSH}}$	A10	RXSOC	A16
MADD3	C8	MDATA24	N3	$\overline{\text{MWSL}}$	A11	SIZE	A11
MADD4	A7	MDATA25	P1	nc	W13	SRXCLAV	C14
MADD5	B7	MDATA26	P2	nc	W15	SRXCLK	B14
MADD6	A6	MDATA27	R1	nc	Y12	SRXDATA0	A14
MADD7	C7	MDATA28	P3	RXADDR0	C17	SRXDATA1	C13
MADD8	B6	MDATA29	R2	RXADDR1	D16	SRXDATA2	B13
MADD9	A5	MDATA3	G1	RXADDR2	A18	SRXDATA3	A13
MCLK	C10	MDATA30	T1	RXADDR3	A17	SRXDATA4	D12
MDATA0	F1	MDATA31	P4	RXADDR4	C15	SRXDATA5	C12
MDATA1	G3	MDATA4	H3	RXDATA0	E18	SRXDATA6	B12
MDATA10	J1	MDATA5	H2	RXDATA1	D19	SRXDATA7	A12
MDATA11	K2	MDATA6	H1	RXDATA2	C20	$\overline{\text{SRXENB}}$	B11
MDATA12	K3	MDATA7	J4	RXDATA3	E17	SRXPRTY	B15
MDATA13	K1	MDATA8	J3	RXDATA4	D18	SRXSOC	A15
MDATA14	L1	MDATA9	J2	RXDATA5	C19	STXCLAV	U9
MDATA15	L2	$\overline{\text{MDS}}$	C11	RXDATA6	B20	STXCLK	V9

Table 2-2. MC92501 256-Lead GTBGA Package Signal List by Name (Continued)

Signal Name	Location	Signal Name	Location	Signal Name	Location	Signal Name	Location
STXDATA0	V6	TXADDR4	Y3	VDD	C4	VSS	A20
STXDATA1	U7	$\overline{\text{TXCCLR}}$	Y4	VDD	D11	VSS	B3
STXDATA2	W6	TXDAT5	W1	VDD	D15	VSS	D13
STXDATA3	Y6	TXDATA0	U2	VDD	D3	VSS	D17
STXDATA4	V7	TXDATA1	V1	VDD	D6	VSS	D4
STXDATA5	W7	TXDATA2	T4	VDD	F17	VSS	D8
STXDATA6	Y7	TXDATA3	U3	VDD	F4	VSS	E4
STXDATA7	V8	TXDATA4	V2	VDD	K4	VSS	H17
$\overline{\text{STXENB}}$	Y5	TXDATA6	V3	VDD	L17	VSS	H4
STXPRTY	W8	TXDATA7	W4	VDD	P18	VSS	N17
STXSOC	Y8	$\overline{\text{TXENB}}$	W5	VDD	R17	VSS	N4
TCK	Y11	$\overline{\text{TXFULL}}$	V5	VDD	R4	VSS	T18
TDI	Y9	TXPHYID0	R3	VDD	U10	VSS	U13
TDO	W10	TXPHYID1	T2	VDD	U15	VSS	U17
TESTOUT	C3	TXPHYID2	U1	VDD	U6	VSS	U4
TESTSEL	B2	TXPHYID3	T3	VDD	V14	VSS	U8
TMS	V10	$\overline{\text{TXPHYIDV}}$	Y3	VDD	V19	VSS	V16
$\overline{\text{TRST}}$	Y10	TXPRTY	U5	VDD	W19	VSS	W20
TXADDR0	R3	TXSOC	V4	VDD	W2	VSS	W3
TXADDR1	T2	VCOCTL	D2	VDD	Y2	VSS	Y1
TXADDR2	U1	VDD	B18	VSS	A1	VSS	Y20
TXADDR3	T3	VDD	B19	VSS	A19		

2.3 GTBGA Mechanical Drawing

GC Suffix
Case 1208-01



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM REQUIREMENT APPLIES TO ZONE T ONLY. PARALLELISM REQUIREMENT SHALL EXCLUDE ANY EFFECT OF LASER MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.83
A1	0.50	0.70
A2	0.56 REF	
A3	1.15	1.49
b	0.65	0.85
D	27.00 BSC	
E	27.00 BSC	
e	1.27 BSC	
F	17.78	24.00
G	17.78	24.00
R1	2.50 REF	
R2	0.40	2.50
R1	0.635 BSC	

Figure 2-2. Glob-Top Ball Grid Array (GTBGA) Package