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Freescale Semiconductor
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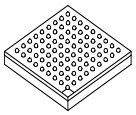
RoHS

MC9328MX1



Package Information
Plastic Package
Case 1304B-01
(MAPBGA–225)

Ordering Information

See Table 1 on page 3

MC9328MX1

1 Introduction

The i.MX Family of applications processors provides a leap in performance with an ARM9™ microprocessor core and highly integrated system functions. The i.MX family specifically addresses the requirements of the personal, portable product market by providing intelligent integrated peripherals, an advanced processor core, and power management capabilities.

The MC9328MX1 (i.MX1) processor features the advanced and power-efficient ARM920T™ core that operates at speeds up to 200 MHz. Integrated modules, which include a USB device, an LCD controller, and an MMC/SD host controller, support a suite of peripherals to enhance portable products seeking to provide a rich multimedia experience. It is packaged in a 256-contact Mold Array Process-Ball Grid Array (MAPBGA). Figure 1 shows the functional block diagram of the i.MX1 processor.

Contents

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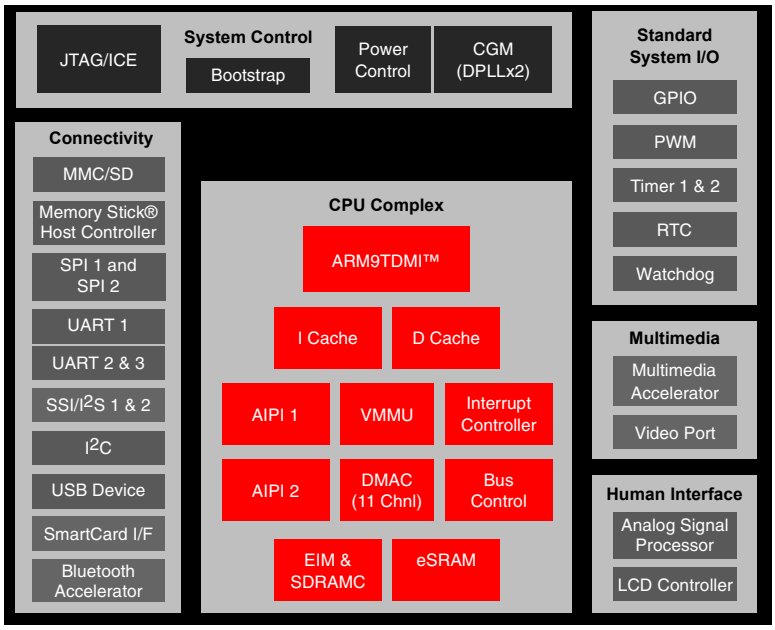

Figure 1. i.MX1 Functional Block Diagram

1.1 Features

To support a wide variety of applications, the processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Three Universal Asynchronous Receiver/Transmitters (UART 1, UART 2, and UART3)
- Two Serial Peripheral Interfaces (SPI1 and SPI2)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Multimedia Card and Secure Digital (MMC/SD) Host Controller Module
- Memory Stick® Host Controller (MSHC)
- Direct Memory Access Controller (DMAC)
- Two Synchronous Serial Interfaces and an Inter-IC Sound (SSI1 and SSI2/I^2S) Module
- Inter-IC (I^2C) Bus Module
- Video Port

- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode
- Analog Signal Processing (ASP) Module
- Bluetooth™ Accelerator (BTA)
- Multimedia Accelerator (MMA)
- Power Management Features
- Operating Voltage Range: 1.7 V to 1.9 V core, 1.7 V to 3.3 V I/O
- 256-pin MAPBGA Package

1.2 Target Applications

The i.MX1 processor is targeted for advanced information appliances, smart phones, Web browsers, based on the popular Palm OS platform, and messaging applications such as wireless cellular products, including the Accompli^{TM} 008 GSM/GPRS interactive communicator.

1.3 Ordering Information

Table 1 provides ordering information.

Table 1. Ordering Information

Package Type	Frequency	Temperature	Solderball Type	Order Number
256-lead MAPBGA	200 MHz	0°C to 70°C	Pb-free	MC9328MX1VM20(R2)
		-30°C to 70°C	Pb-free	MC9328MX1DVM20(R2)
	150 MHz	0°C to 70°C	Pb-free	MC9328MX1VM15(R2)
		-30°C to 70°C	Pb-free	MC9328MX1DVM15(R2)
		-40°C to 85°C	Pb-free	MC9328MX1CVM15(R2)

1.4 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.

- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

2 Signals and Connections

Table 2 identifies and describes the i.MX1 processor signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

Table 2. i.MX1 Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip-Select (EIM)	
A[24:0]	Address bus signals
D[31:0]	Data bus signals
$\overline{EB0}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24].
$\overline{EB1}$	Byte Strobe—Active low external enable byte signal that controls D [23:16].
$\overline{EB2}$	Byte Strobe—Active low external enable byte signal that controls D [15:8].
$\overline{EB3}$	LSB Byte Strobe—Active low external enable byte signal that controls D [7:0].
$\overline{OE}$	Memory Output Enable—Active low output enables external data bus.
$\overline{CS}$ [5:0]	Chip-Select—The chip-select signals $\overline{CS}$ [3:2] are multiplexed with $\overline{CSD}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default $\overline{CSD}$ [1:0] is selected.
$\overline{ECB}$	Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
$\overline{LBA}$	Active low signal sent by a flash device causing the external burst device to latch the starting burst address.
BCLK (burst clock)	Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
$\overline{RW}$	$\overline{RW}$ signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a $\overline{WE}$ input signal by external DRAM.
$\overline{DTACK}$	$\overline{DTACK}$ signal—The external input data acknowledge signal. When using the external DTACK signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external DTACK signal after 1022 clock counts have elapsed.
Bootstrap	
BOOT [3:0]	System Boot Mode Select—The operational system boot mode of the i.MX1 processor upon system reset is determined by the settings of these pins.
SDRAM Controller	
SDBA [4:0]	SDRAM non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM cycles.

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SDIBA [3:0]	SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles.
MA [11:10]	SDRAM address signals
MA [9:0]	SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles.
DQM [3:0]	SDRAM data enable
$\overline{\text{CSD0}}$	SDRAM Chip-select signal which is multiplexed with the $\overline{\text{CS2}}$ signal. These two signals are selectable by programming the system control register.
$\overline{\text{CSD1}}$	SDRAM Chip-select signal which is multiplexed with $\overline{\text{CS3}}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{\text{CSD1}}$ is selected, so it can be used as boot chip-select by properly configuring BOOT [3:0] input pins.
$\overline{\text{RAS}}$	SDRAM Row Address Select signal
$\overline{\text{CAS}}$	SDRAM Column Address Select signal
$\overline{\text{SDWE}}$	SDRAM Write Enable signal
SDCKE0	SDRAM Clock Enable 0
SDCKE1	SDRAM Clock Enable 1
SDCLK	SDRAM Clock
$\overline{\text{RESET\_SF}}$	Not Used
Clocks and Resets	
EXTAL16M	Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.
XTAL16M	Crystal output
EXTAL32K	32 kHz crystal input
XTAL32K	32 kHz crystal output
CLKO	Clock Out signal selected from internal clock signals.
$\overline{\text{RESET\_IN}}$	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.
$\overline{\text{RESET\_OUT}}$	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{\text{RESET\_IN}}$), and Watchdog time-out.
POR	Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.
JTAG	
$\overline{\text{TRST}}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
$\overline{\text{TDO}}$	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
DMA	
$\overline{\text{DMA\_REQ}}$	$\overline{\text{DMA Request}}$—external DMA request signal. Multiplexed with SPI1_SPI_RDY.
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to big endian. If it is driven logic-low at reset, the external chip-select space will be configured to little endian. This input must not change state after power-on reset negates or during chip operation.
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIPESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIPESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with $\overline{\text{ECB}}$, $\overline{\text{LBA}}$, BCLK (burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SIM	
SIM_CLK	SIM Clock
SIM_RST	SIM Reset
SIM_RX	Receive Data

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SIM_TX	Transmit Data
SIM_PD	Presence Detect Schmitt trigger input
SIM_SVEN	SIM Vdd Enable
SPI 1 and SPI 2	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out
SPI1_$\overline{SS}$	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_$\overline{SPI_RDY}$	Serial Data Ready
SPI2_TXD	SPI2 Master TxData Output—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_RXD	SPI2 Master RxData Input—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_$\overline{SS}$	SPI2 Slave Select—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_SCLK	SPI2 Serial Clock—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MX1 Reference Manual* for information about how to bring this signal to the assigned pin.
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB Receive Data
$\overline{USBD\_ROE}$	USB $\overline{OE}$
USBD_AFE	USB Analog Front End Enable
Secure Digital Interface	
SD_CMD	SD Command—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 4.7K–69K external pull up resistor must be added.

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_CLK	MMC Output Clock
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1\_RTS}}$	Request to Send
$\overline{\text{UART1\_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{\text{UART2\_RTS}}$	Request to Send
$\overline{\text{UART2\_CTS}}$	Clear to Send
$\overline{\text{UART2\_DSR}}$	Data Set Ready
$\overline{\text{UART2\_RI}}$	Ring Indicator
$\overline{\text{UART2\_DCD}}$	Data Carrier Detect
$\overline{\text{UART2\_DTR}}$	Data Terminal Ready
UART3_RXD	Receive Data
UART3_TXD	Transmit Data
$\overline{\text{UART3\_RTS}}$	Request to Send
$\overline{\text{UART3\_CTS}}$	Clear to Send
$\overline{\text{UART3\_DSR}}$	Data Set Ready
$\overline{\text{UART3\_RI}}$	Ring Indicator
$\overline{\text{UART3\_DCD}}$	Data Carrier Detect
$\overline{\text{UART3\_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^2S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
SSI2_TXDAT	TxD
SSI2_RXDAT	RxD
SSI2_TXCLK	Transmit Serial Clock
SSI2_RXCLK	Receive Serial Clock
SSI2_TXFS	Transmit Frame Sync
SSI2_RXFS	Receive Frame Sync
I^2C	
I2C_SCL	I^2C Clock
I2C_SDA	I^2C Data
PWM	
PWMO	PWM Output
ASP	
UIN	Positive U analog input (for low voltage, temperature measurement)
UIP	Negative U analog input (for low voltage, temperature measurement)
PX1	Positive pen-X analog input
PY1	Positive pen-Y analog input
PX2	Negative pen-X analog input
PY2	Negative pen-Y analog input
R1A	Positive resistance input (a)
R1B	Positive resistance input (b)
R2A	Negative resistance input (a)
R2B	Negative resistance input (b)
RVP	Positive reference for pen ADC
RVM	Negative reference for pen ADC
AVDD	Analog power supply
AGND	Analog ground
BlueTooth	
BT1	I/O clock signal
BT2	Output
BT3	Input

Table 2. i.MX1 Signal Descriptions (Continued)

Signal Name	Function/Notes
BT4	Input
BT5	Output
BT6	Output
BT7	Output
BT8	Output
BT9	Output
BT10	Output
BT11	Output
BT12	Output
BT13	Output
BTRF VDD	Power supply from external BT RFIC
BTRF GND	Ground from external BT RFIC
Test Function	
TRISTATE	Forces all I/O signals to high impedance for test purposes. For normal operation, terminate this input with a 1 k ohm resistor to ground. (TRI-STATE® is a registered trademark of National Semiconductor.)
Digital Supply Pins	
NVDD	Digital Supply for the I/O pins
NVSS	Digital Ground for the I/O pins
Supply Pins – Analog Modules	
AVDD	Supply for analog blocks
Internal Power Supply	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Ground pins for silicon internal circuitry

2.1 I/O Pads Power Supply and Signal Multiplexing Scheme

This section describes detailed information about both the power supply for each I/O pin and its function multiplexing scheme. The user can reference information provided in Table 6 on page 23 to configure the power supply scheme for each device in the system (memory and external peripherals). The function multiplexing information also shown in Table 6 allows the user to select the function of each pin by configuring the appropriate GPIO registers when those pins are multiplexed to provide different functions.

Table 3. MC9328MX1 Signal Multiplexing Scheme

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	K8	NVDD1	Static										
NVDD1	B1	A24	O		ETMTRACESYNC	O	PA0	69K	SPI2_CLK			L	A24
NVDD1	C2	D31	I/O	69K								Pull-H	
NVDD1	C1	A23	O		ETMTRACECLK	O	PA31	69K				L	A23
NVDD1	D2	D30	I/O	69K								Pull-H	
NVDD1	D1	A22	O		ETMPIPESTAT2	O	PA30	69K				L	A22
NVDD1	D3	D29	I/O	69K								Pull-H	
NVDD1	E2	A21	O		ETMPIPESTAT1	O	PA29	69K				L	A21
NVDD1	E3	D28	I/O	69K								Pull-H	
NVDD1	E1	A20	O		ETMPIPESTAT0	O	PA28	69K				L	A20
NVDD1	F2	D27	I/O	69K								Pull-H	
NVDD1	F4	A19	O		ETMTRACEPKT3	O	PA27	69K				L	A19
NVDD1	E4	D26	I/O	69K								Pull-H	
	A1	VSS	Static										
NVDD1	H5	NVDD1	Static										
NVDD1	F1	A18	O		ETMTRACEPKT2	O	PA26	69K				L	A18
NVDD1	F3	D25	I/O	69K								Pull-H	
NVDD1	G2	A17	O		ETMTRACEPKT1	O	PA25	69K				L	A17
NVDD1	G3	D24	I/O	69K								Pull-H	
NVDD1	F5	A16	O		ETMTRACEPKT0	O	PA24	69K				L	A16
NVDD1	G4	D23	I/O	69K								Pull-H	
NVDD1	G1	A15	O									L	
NVDD1	H2	D22	I/O	69K								Pull-H	
NVDD1	H3	A14	O									L	

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	G5	D21	I/O	69K								Pull-H	
NVDD1	H1	A13	O									L	
NVDD1	H4	D20	I/O	69K								Pull-H	
	T1	VSS	Static										
QVDD1	H9	QVDD1	Static										
	H8	VSS	Static										
NVDD1	J5	NVDD1	Static										
NVDD1	J1	A12	O									L	
NVDD1	J4	D19	I/O	69K								Pull-H	
NVDD1	J2	A11	O									L	
NVDD1	J3	D18	I/O	69K								Pull-H	
NVDD1	K1	A10	O									L	
NVDD1	K4	D17	I/O	69K								Pull-H	
NVDD1	K3	A9	O									L	
NVDD1	K2	D16	I/O	69K								Pull-H	
NVDD1	L1	A8	O									L	
NVDD1	L4	D15	I/O	69K								Pull-H	
NVDD1	L2	A7	O									L	
NVDD1	L5	D14	I/O	69K								Pull-H	
	K6	VSS	Static										
NVDD1	K5	NVDD1	Static										
NVDD1	M4	A6	O									L	
NVDD1	L3	D13	I/O	69K								Pull-H	
NVDD1	M1	A5	O									L	
NVDD1	M2	D12	I/O	69K								Pull-H	

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	N1	A4	O									L	
NVDD1	M3	D11	I/O	69K								Pull-H	
NVDD1	P3	$\overline{EB0}$	O									H	
NVDD1	N3	D10	I/O	69K								Pull-H	
NVDD1	P1	A3	O									L	
NVDD1	N2	$\overline{EB1}$	O									H	
NVDD1	P2	D9	I/O	69K								Pull-H	
NVDD1	R1	$\overline{EB2}$	O									H	
	M6	VSS	Static										
NVDD1	H6	NVDD1	Static										
NVDD1	T2	A2	O									L	
NVDD1	R2	$\overline{EB3}$	O									H	
NVDD1	R5	D8	I/O	69K								Pull-H	
NVDD1	T3	$\overline{OE}$	O									H	
NVDD1	R3	A1	O									L	
NVDD1	T4	$\overline{CS5}$	O				PA23	69K				Pull-H	PA23
NVDD1	N4	D7	I/O	69K								Pull-H	
NVDD1	R4	$\overline{CS4}$	O				PA22	69K				Pull-H	PA22
NVDD1	N5	A0	O				PA21	69K				L	A0
NVDD1	P4	$\overline{CS3}$	O		$\overline{CSD1}$							H	$\overline{CSD1}$
NVDD1	P5	D6	I/O	69K								Pull-H	
NVDD1	T5	$\overline{CS2}$	O		$\overline{CSD0}$							H	$\overline{CSD0}$
	H7	VSS	Static										
NVDD1	J6	NVDD1	Static										
NVDD1	M5	SDCLK	O									H	

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	T6	$\overline{CS1}$	O									H	
NVDD1	T7	$\overline{CS0}$	O									H[1]	
NVDD1	R6	D5	I/O	69K								Pull-H	
NVDD1	P6	$\overline{ECB}$	I		ETMTRACEPKT7		PA20	69K				Pull-H	$\overline{ECB}$
NVDD1	N6	D4	I/O	69K								Pull-H	
NVDD1	R7	$\overline{LBA}$	O		ETMTRACEPKT6		PA19	69K				H	$\overline{LBA}$
NVDD1	P8	D3	I/O	69K								Pull-H	
NVDD1	R8	BCLK			ETMTRACEPKT5		PA18	69K				L	BCLK
NVDD1	P7	D2	I/O	69K								Pull-H	
	J7	VSS	Static										
NVDD1	L6	NVDD1	Static										
NVDD1	N7	DTACK	I		ETMTRACEPKT4		PA17	69K	SPI2_SS	A25		Pull-H	PA17
NVDD1	N8	D1	I/O	69K								Pull-H	
NVDD1	M7	$\overline{RW}$										H	
NVDD1	T8	MA11	O									L	
NVDD1	M8	MA10	O									L	
NVDD1	R9	D0	I/O	69K								Pull-H	
	K7	VSS	Static										
NVDD1	P9	DQM3	O									L	
NVDD1	T9	DQM2	O									L	
NVDD1	N9	DQM1	O									L	
NVDD1	R10	DQM0	O									L	
NVDD1	M9	$\overline{RAS}$	O									H	
NVDD1	L8	$\overline{CAS}$	O									H	
NVDD1	J8	NVDD1	Static										

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD1	T10	$\overline{\text{SDWE}}$	O									H	
NVDD1	R11	SDCKE0	O									H	
NVDD1	P10	SDCKE1	O									H	
NVDD1	N10	$\overline{\text{RESET\_SF}}$	O									L/H	
NVDD1	T11	CLKO	O									L	
	L7	VSS	Static										
AVDD1	T12	AVDD1	Static										
AVDD1	M10	$\overline{\text{RESET\_IN}}$	I	69K								L/H[2]	
AVDD1	N11	$\overline{\text{RESET\_OUT}}$	O									L/H	
AVDD1	R12	POR	I									H/L[2]	
AVDD1	M11	BIG_ENDIAN	I									Hiz[3]	
AVDD1	P11	BOOT3	I									Hiz[4]	
AVDD1	N12	BOOT2	I									Hiz[4]	
AVDD1	R13	BOOT1	I									Hiz[4]	
AVDD1	P12	BOOT0	I									Hiz[4]	
AVDD1	T13	TRISTATE	I									Hiz[4]	
AVDD1	P13	$\overline{\text{TRST}}$	I	69K								H	
QVDD2	R15	QVDD2	Static										
	T16	VSS	Static										
AVDD1	T14	EXTAL16M	I									Hiz	
AVDD1	T15	XTAL16M	O										
AVDD1	R16	EXTAL32K	I									Hiz	
AVDD1	P16	XTAL32K	O										
NVDD2	K10	NVDD2	Static										

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD2	R14	$\overline{TDO}$	O									Hiz[5]	
NVDD2	N15	TMS	I	69K								Pull-H	
NVDD2	L9	TCK	I	69K								Pull-H	
NVDD2	N16	TDI	I	69K								Pull-H	
NVDD2	P14	I2C_SCL	O				PA16	69K				Pull-H	PA16
NVDD2	P15	I2C_SDA	I/O				PA15	69K				Pull-H	PA15
NVDD2	N13	CSI_PIXCLK	I				PA14	69K				Pull-H	PA14
NVDD2	M13	CSI_HSYNC	I				PA13	69K				Pull-H	PA13
NVDD2	M14	CSI_VSYNC	I				PA12	69K				Pull-H	PA12
NVDD2	N14	CSI_D7	I				PA11	69K				Pull-H	PA11
NVDD2	M15	CSI_D6	I				PA10	69K				Pull-H	PA10
NVDD2	M16	CSI_D5	I				PA9	69K				Pull-H	PA9
NVDD2	J10	VSS	Static										
NVDD2	M12	CSI_D4	I				PA8	69K				Pull-H	PA8
NVDD2	L16	CSI_D3	I				PA7	69K				Pull-H	PA7
NVDD2	L15	CSI_D2	I				PA6	69K				Pull-H	PA6
NVDD2	L14	CSI_D1	I				PA5	69K				Pull-H	PA5
NVDD2	L13	CSI_D0	I				PA4	69K				Pull-H	PA4
NVDD2	L12	CSI_MCLK	O				PA3	69K				Pull-H	PA3
NVDD2	L11	PWMO	O				PA2	69K				Pull-H	PA2
NVDD2	L10	TIN	I				PA1	69K			SPI2_RxD	Pull-H	PA1
NVDD2	K15	TMR2OUT	O				PD31	69K	SPI2_TxD			Pull-H	PD31
NVDD2	K16	LD15	O				PD30	69K				Pull-H	PD30
NVDD2	K14	LD14	O				PD29	69K				Pull-H	PD29
NVDD2	K13	LD13	O				PD28	69K				Pull-H	PD28

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD2	K12	LD12	O				PD27	69K				Pull-H	PD27
QVDD3	J15	QVDD3	Static										
	J16	VSS	Static										
NVDD2	K9	NVDD2	Static										
NVDD2	J14	LD11	O				PD26	69K				Pull-H	PD26
NVDD2	K11	LD10	O				PD25	69K				Pull-H	PD25
NVDD2	H15	LD9	O				PD24	69K				Pull-H	PD24
NVDD2	J13	LD8	O				PD23	69K				Pull-H	PD23
NVDD2	J12	LD7	O				PD22	69K				Pull-H	PD22
NVDD2	J11	LD6	O				PD21	69K				Pull-H	PD21
NVDD2	H14	LD5	O				PD20	69K				Pull-H	PD20
NVDD2	H13	LD4	O				PD19	69K				Pull-H	PD19
NVDD2	H16	LD3	O				PD18	69K				Pull-H	PD18
NVDD2	H12	LD2	O				PD17	69K				Pull-H	PD17
NVDD2	G16	LD1	O				PD16	69K				Pull-H	PD16
NVDD2	H11	LD0	O				PD15	69K				Pull-H	PD15
NVDD2	G15	FLM/VSYNC	O				PD14	69K				Pull-H	PD14
NVDD2	G14	LP/HSYNC	O				PD13	69K				Pull-H	PD13
NVDD2	G13	ACD/OE	O				PD12	69K				Pull-H	PD12
NVDD2	G12	CONTRAST	O				PD11	69K		SPI2_SS2		Pull-H	PD11
NVDD2	F16	SPL_SPR	O		$\overline{\text{UART2\_DSR}}$	O	PD10	69K	SPI2_TxD			Pull-H	PD10
NVDD2	H10	PS	O		$\overline{\text{UART2\_RI}}$	O	PD9	69K			SPI2_RxD	Pull-H	PD9
NVDD2	G11	CLS	O		$\overline{\text{UART2\_DCD}}$	O	PD8	69K	SPI2_SS			Pull-H	PD8
NVDD2	F12	REV	O		$\overline{\text{UART2\_DTR}}$	I	PD7	69K	SPI2_CLK			Pull-H	PD7
NVDD2	F15	LSCLK	O				PD6	69K				Pull-H	PD6

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
	J9	VSS	Static										
QVDD[6]	E16	R2A	I									qvdd	
QVDD[6]	D16	R2B	I										
QVDD[6]	F14	PX1	I										
QVDD[6]	F13	PY1	I										
QVDD[6]	E15	PX2	I										
QVDD[6]	E14	PY2	I										
QVDD[6]	D15	R1A	I										
QVDD[6]	C16	R1B	I										
	C15	VSS	Static										
AVDD2[6]	C14	AVDD2	Static										
QVDD[6]	B16	NC	I										
QVDD[6]	A16	NC	I										
QVDD[6]	B15	UIN	I										
QVDD[6]	A15	UIP	I										
QVDD[6]	E13	NC	I										
QVDD[6]	D14	NC	I										
QVDD[6]	B14	RVM	I										
QVDD[6]	A14	RVP	I										
QVDD[6]	D13	NC	I										
QVDD[6]	C13	NC	I										
QVDD[6]	E12	NC	O										

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
QVDD[6]	D12	NC	O										
QVDD4	A13	QVDD4	Static										
	B13	VSS	Static										
BTRFVDD	C12	BTRFVDD	Static										
BTRFVDD	B12	BT1	I				PC31	69K			UART3_RX	Pull-H	PC31
BTRFVDD	F11	BT2	O				PC30	69K		UART3_TX		Hiz	PC30
BTRFVDD	A12	BT3	I				PC29	69K			UART3_RTS	Pull-H	PC29
BTRFVDD	E11	BT4	I				PC28	69K		UART3_CTS		Pull-H	PC28
BTRFVDD	A11	BT5	I/O				PC27	69K		UART3_DCD		Pull-H	PC27
BTRFVDD	D11	BT6	O				PC26	69K		SPI2_SS3	UART3_DTR	L	PC26
BTRFVDD	B11	BT7	O				PC25	69K		UART3_DSR		L	PC25
BTRFVDD	C11	BT8	O		SSI2_RXFS		PC24	69K		UART3_RI		Hiz	PC24
BTRFVDD	G10	BT9	O		SSI2_RX		PC23	69K				L	PC23
BTRFVDD	F10	BT10	O		SSI2_TX		PC22	69K				H	PC22
BTRFVDD	B10	BT11	O		SSI2_TXCLK		PC21	69K				H	PC21
BTRFVDD	E10	BT12	O		SSI2_TXFS		PC20	69K				Hiz	PC20
BTRFVDD	D10	BT13	O		SSI2_RXCLK		PC19	69K				L	PC19
	C10	BTRFGND	Static										
NVDD3	A10	NVDD3	Static										
NVDD3	G9	SPI1_MOSI	I/O				PC17	69K				Pull-H	PC17
NVDD3	F9	SPI1_MISO	I/O				PC16	69K				Pull-H	PC16
NVDD3	E9	SPI1_$\overline{SS}$	I/O				PC15	69K				Pull-H	PC15
NVDD3	B9	SPI1_SCLK	I/O				PC14	69K				Pull-H	PC14
NVDD3	D9	SPI1_$\overline{SPI_RDY}$	I				PC13	69K			$\overline{DMA\_Req}$	Pull-H	PC13
NVDD3	A9	UART1_RXD	I				PC12	69K				Pull-H	PC12

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD3	C9	UART1_TXD	O				PC11	69K				Pull-H	PC11
NVDD3	A8	$\overline{\text{UART1\_RTS}}$	I				PC10	69K				Pull-H	PC10
NVDD3	G8	$\overline{\text{UART1\_CTS}}$	O				PC9	69K				Pull-H	PC9
NVDD3	B8	SSI_TXCLK	I/O				PC8	69K				Pull-H	PC8
NVDD3	F8	SSI_TXFS	I/O				PC7	69K				Pull-H	PC7
NVDD3	E8	SSI_TXDAT	O				PC6	69K				Pull-H	PC6
NVDD3	D8	SSI_RXDAT	I				PC5	69K				Pull-H	PC5
NVDD3	B7	SSI_RXCLK	I/O				PC4	69K				Pull-H	PC4
NVDD3	C8	SSI_RXFS	I/O				PC3	69K				Pull-H	PC3
	A7	VSS	Static										
NVDD4	C7	UART2_RXD	I				PB31	69K				Pull-H	PB31
NVDD4	F7	UART2_TXD	O				PB30	69K				Pull-H	PB30
NVDD4	E7	$\overline{\text{UART2\_RTS}}$	I				PB29	69K				Pull-H	PB29
NVDD4	C6	$\overline{\text{UART2\_CTS}}$	O				PB28	69K				Pull-H	PB28
NVDD4	D7	USBD_VMO	O				PB27	69K				Pull-H	PB27
NVDD4	D6	USBD_VPO	O				PB26	69K				Pull-H	PB26
NVDD4	E6	USBD_VM	I				PB25	69K				Pull-H	PB25
NVDD4	B6	USBD_VP	I				PB24	69K				Pull-H	PB24
NVDD4	D5	USBD_SUSPND	O				PB23	69K				Pull-H	PB23
NVDD4	C5	USBD_RCV	I/O				PB22	69K				Pull-H	PB22
NVDD4	B5	$\overline{\text{USBD\_ROE}}$	O				PB21	69K				Pull-H	PB21
NVDD4	A5	USBD_AFE	O				PB20	69K				Pull-H	PB20
	A4	VSS	Static										
NVDD4	A6	NVDD4	Static										
NVDD4	G7	SIM_CLK	O		SSI_TXCLK	I/O	PB19	69K				Pull-H	PB19

Table 3. MC9328MX1 Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	BGA Pin	Primary			Alternate		GPIO					RESE State (At/After)	Default
		Signal	Dir	Pull-up	Signal	Dir	Mux	Pull-up	Ain	Bin	Aout		
NVDD4	F6	SIM_RST	O		SSI_TXFS	I/O	PB18	69K				Pull-H	PB18
NVDD4	G6	SIM_RX	I		SSI_TXDAT	O	PB17	69K				Pull-H	PB17
NVDD4	B4	SIM_TX	I/O		SSI_RXDAT	I	PB16	69K				Pull-H	PB16
NVDD4	C4	SIM_PD	I		SSI_RXCLK	I/O	PB15	69K				Pull-H	PB15
NVDD4	D4	SIM_SVEN	O		SSI_RXFS	I/O	PB14	69K				Pull-H	PB14
NVDD4	B3	SD_CMD	I/O		MS_BS	O	PB13	69K				Pull-H	PB13
NVDD4	A3	SD_CLK	O		MS_SCLKO	O	PB12	69K				Pull-H	PB12
NVDD4	A2	SD_DAT3	I/O		MS_SDIO	I/O	PB11	69K (pull down)				Pull-L	PB11
NVDD4	E5	SD_DAT2	I/O		MS_SCLKI	I	PB10	69K				Pull-H	PB10
NVDD4	B2	SD_DAT1	I/O		MS_PI1	I	PB9	69K				Pull-H	PB9
NVDD4	C3	SD_DAT0	I/O		MS_PI0	I	PB8	69K				Pull-H	PB8

1 After reset, $\overline{CS0}$ goes H/L depends on BOOT[3:0].

2 Need external circuitry to drive the signal.

3 Need external pull-up.

4 External resistor is needed.

5 Need external pull-up or pull-down.

6 ASP signals are clamped by AVDD2 to prevent ESD (electrostatic discharge) damage. AVDD2 must be greater than QVDD to keep diodes reverse-biased.

3 Electrical Characteristics

This section contains the electrical specifications and timing diagrams for the i.MX1 processor.

3.1 Maximum Ratings

Table 4 provides information on maximum ratings which are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits listed in Recommended Operating Range Table 5 on page 23 or the DC Characteristics table.

Table 4. Maximum Ratings

Symbol	Rating	Minimum	Maximum	Unit
NV_{DD}	DC I/O Supply Voltage	-0.3	3.3	V
QV_{DD}	DC Internal (core = 150 MHz) Supply Voltage	-0.3	1.9	V
QV_{DD}	DC Internal (core = 200 MHz) Supply Voltage	-0.3	2.0	V
AV_{DD}	DC Analog Supply Voltage	-0.3	3.3	V
$BTRFV_{DD}$	DC Bluetooth Supply Voltage	-0.3	3.3	V
VESD_HBM	ESD immunity with HBM (human body model)	–	2000	V
VESD_MM	ESD immunity with MM (machine model)	–	100	V
ILatchup	Latch-up immunity	–	200	mA
Test	Storage temperature	-55	150	°C
Pmax	Power Consumption	800[1]	1300[2]	mW

1 A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM® core-that is, 7x GPIO, 15x Data bus, and 8x Address bus.

2 A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core-that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at MHz, and where the whole image is running out of SDRAM. QVDD at V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

3.2 Recommended Operating Range

Table 5 provides the recommended operating ranges for the supply voltages and temperatures. The i.MX1 processor has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

BTRFVDD is the supply voltage for the Bluetooth interface signals. It is quite sensitive to the data transmit/receive accuracy. Please refer to Bluetooth RF spec for special handling. If Bluetooth is not used

in the system, these Bluetooth pins can be used as general purpose I/O pins and BTRFVDD can be used as other NVDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.

Table 5. Recommended Operating Range

Symbol	Rating	Minimum	Maximum	Unit
T_A	Operating temperature range MC9328MX1VM20\MC9328MX1VM15	0	70	°C
T_A	Operating temperature range MC9328MX1DVM20\MC9328MX1DVM15	-30	70	°C
T_A	Operating temperature range MC9328MX1CVM15	-40	85	°C
NVDD	I/O supply voltage (if using MSHC, CSI, SPI, BTA, LCD, and USBd which are only 3 V interfaces)	2.70	3.30	V
NVDD	I/O supply voltage (if not using the peripherals listed above)	1.70	3.30	V
QVDD	Internal supply voltage (Core = 150 MHz)	1.70	1.90	V
QVDD	Internal supply voltage (Core = 200 MHz)	1.80	2.00	V
AVDD	Analog supply voltage	1.70	3.30	V

3.3 Power Sequence Requirements

For required power-up and power-down sequencing, please refer to the “Power-Up Sequence” section of application note AN2537 on the i.MX applications processor website.

3.4 DC Electrical Characteristics

Table 6 contains both maximum and minimum DC characteristics of the i.MX1 processor.

Table 6. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Min	Typical	Max	Unit
Iop	Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, MPEG4 decoding playback from external memory card to both external SSI audio decoder and driving TFT display panel, and OS with MMU enabled memory system is running on external SDRAM).	–	QVDD at 1.8V = 120mA; NVDD+AVDD at 3.0V = 30mA	–	mA
$Sidd_1$	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 25°C)	–	25	–	µA
$Sidd_2$	Standby current (Core = 150 MHz, QVDD = 1.8V, temp = 55°C)	–	45	–	µA
$Sidd_3$	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 25°C)	–	35	–	µA

Table 6. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Min	Typical	Max	Unit
$Sidd_4$	Standby current (Core = 150 MHz, QVDD = 2.0V, temp = 55°C)	–	60	–	µA
V_{IH}	Input high voltage	$0.7V_{DD}$	–	Vdd+0.2	V
V_{IL}	Input low voltage	–	–	0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0 mA)	$0.7V_{DD}$	–	Vdd	V
V_{OL}	Output low voltage (I_{OL} = -2.5 mA)	–	–	0.4	V
I_{IL}	Input low leakage current (V_{IN} = GND, no pull-up or pull-down)	–	–	±1	µA
I_{IH}	Input high leakage current (V_{IN} = V_{DD}, no pull-up or pull-down)	–	–	±1	µA
I_{OH}	Output high current (V_{OH} = $0.8V_{DD}$, V_{DD} = 1.8V)	4.0	–	–	mA
I_{OL}	Output low current (V_{OL} = 0.4V, V_{DD} = 1.8V)	-4.0	–	–	mA
I_{OZ}	Output leakage current (V_{out} = V_{DD}, output is high impedance)	–	–	±5	µA
C_i	Input capacitance	–	–	5	pF
C_o	Output capacitance	–	–	5	pF

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 150 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading.

Table 7. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	–	20.8	ns

Table 8. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak)	–	5	20	ns
EXTAL32k startup time	800	–	–	ms

Table 8. 32k/16M Oscillator Signal Timing (Continued)

Parameter	Minimum	RMS	Maximum	Unit
EXTAL16M input jitter (peak to peak) [1]	–	TBD	TBD	–
EXTAL16M startup time [1]	TBD	–	–	–

[1] The 16 MHz oscillator is not recommended for use in new designs.

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MX1.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

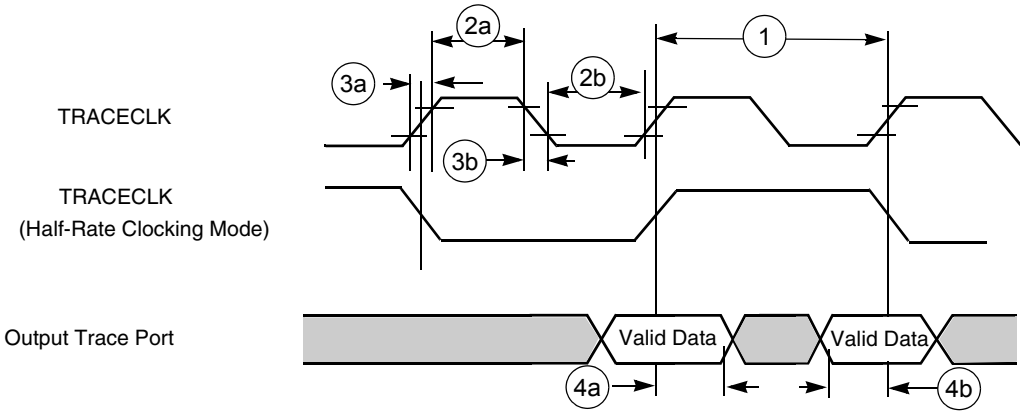

Figure 2. Trace Port Timing Diagram