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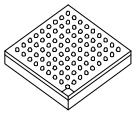
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9328MX21S
Rev. 1.3, 06/2008

MC9328MX21S



Package Information

(MAPBGA–289)

Ordering Information: See Table 1 on page 3

MC9328MX21S

266 MHz

1 Introduction

Freescale's i.MX family of microprocessors has demonstrated leadership in the portable handheld market. Building on the success of the MX (Media Extensions) series, the i.MX21S (MC9328MX21S) provides a leap in performance with an ARM926EJ-S™ microprocessor core that provides accelerated Java support in addition to highly integrated system functions. The i.MX21S device addresses the needs of multiple markets with intelligent integrated peripherals, advanced ARM® processor core, and power management capabilities.

The i.MX21S features the advanced and power-efficient ARM926EJ-S core operating at speeds up to 266 MHz and is part of a growing family of *Smart Speed* products that offer high performance processing optimized for lowest power consumption. On-chip modules such as an LCD controller, USB On-The-Go, 1-Wire® interface, and synchronous serial interfaces offer designers a rich suite of peripherals that can enhance many products.

For cost sensitive applications, the NAND Flash controller allows the use of low-cost NAND Flash

Contents

devices to be used as primary or secondary non-volatile storage. The on-chip error correction code (ECC) and parity checking circuitry of the NAND Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The device is packaged in a 289-pin MAPBGA.

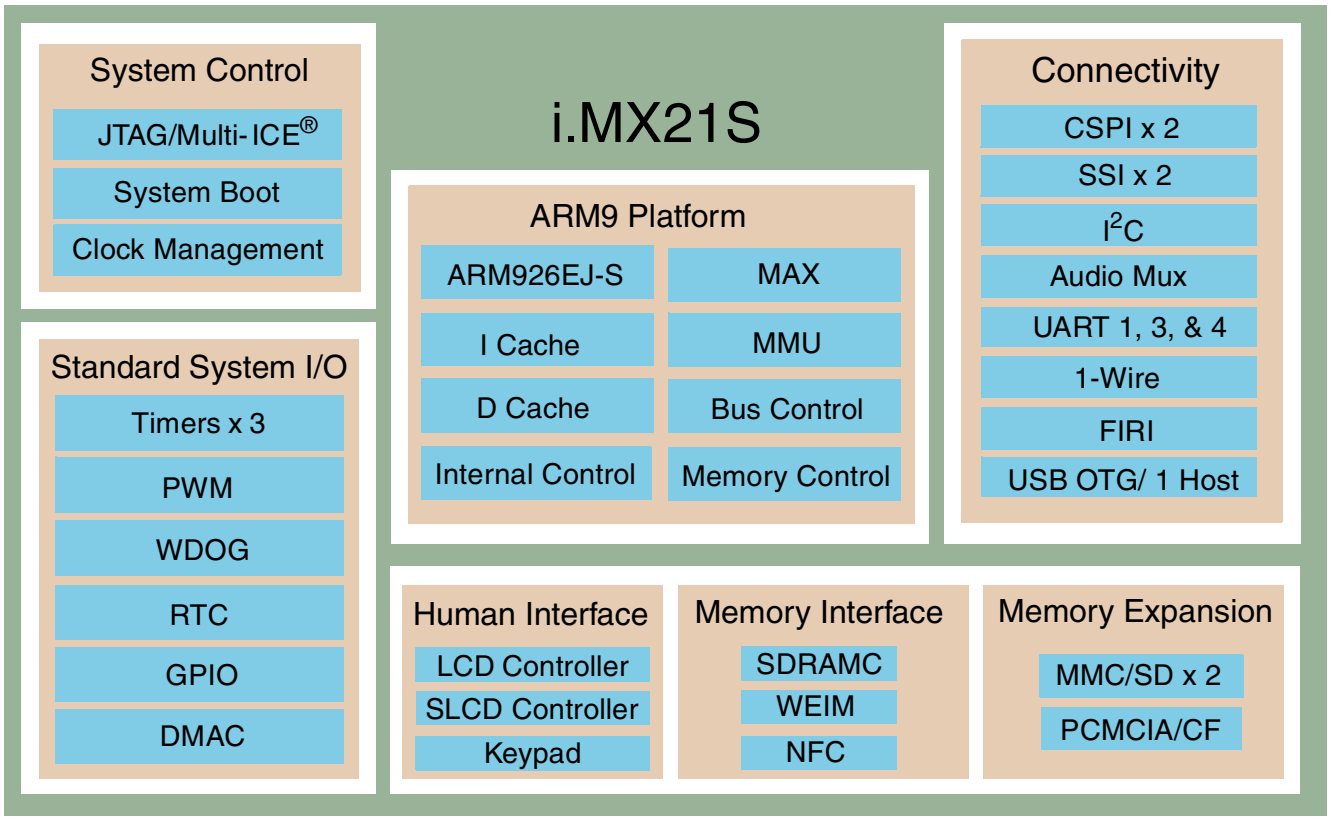


Figure 1. i.MX21S Functional Block Diagram

1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.

- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

1.2 Reference Documentation

The following documents are required for a complete description of the i.MX21S and are necessary to design properly with the device. Especially for those not familiar with the ARM926EJ-S processor the following documents are helpful when used in conjunction with this manual.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM7TDMI Data Sheet (ARM Ltd., order number ARM DDI 0029)

ARM920T Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

MC9328MX21S Product Brief (order number MC9328MX21SPB)

The Freescale manuals are available on the Freescale Semiconductor Web site at http://www.freescale.com. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.

1.3 Ordering Information

Table 1 provides ordering information for the device.

Table 1. Ordering Information

Part Order Number	Package Size	Package Type	Operating Range
MC9328MX21SVK	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	0°C–70°C
MC9328MX21SCVK	289-lead MAPBGA 0.65mm, 14mm x 14mm	Lead-free	-40°C–85°C
MC9328MX21SVM	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	0°C–70°C
MC9328MX21SCVM	289-lead MAPBGA 0.8mm, 17mm x 17mm	Lead-free	-40°C–85°C

1.4 Features

The i.MX21S boasts a robust array of features that can support a wide variety of applications. Below is a brief description of i.MX21S features.

- ARM926EJ-S Core Complex
- Display and Video Modules
  - LCD Controller (LCDC)
  - Smart LCD Controller (SLCDC)
- Wireless Connectivity
  - Fast Infra-Red Interface (FIRI)
- Wired Connectivity
  - USB On-The-Go (USBOTG) Controller

  - Three Universal Asynchronous Receiver/Transmitters (UART*x*)
  - Two Configurable Serial Peripheral Interfaces (CSPI*x*) for High Speed Data Transfer
  - Inter-IC (I^2C) Bus Module
  - Two Synchronous Serial Interfaces (SSI) with Inter-IC Sound (I^2S)
  - Digital Audio Mux
  - One-Wire Controller
  - Keypad Interface
- Memory Expansion and I/O Card Support
  - Two Multimedia Card and Secure Digital (MMC/SD) Host Controller Modules
- Memory Interface
  - External Interface Module (EIM)
  - SDRAM Controller (SDRAMC)
  - NAND Flash Controller (NFC)
  - PCMCIA/CF Interface
- Standard System Resources
  - Clock Generation Module (CGM) and Power Control Module
  - Three General-Purpose 32-Bit Counters/Timers
  - Watchdog Timer
  - Real-Time Clock/Sampling Timer (RTC)
  - Pulse-Width Modulator (PWM) Module
  - Direct Memory Access Controller (DMAC)
  - General-Purpose I/O (GPIO) Ports
  - Debug Capability

2 Signal Descriptions

Table 2 identifies and describes the i.MX21S signals. Pin assignment is provided in Section 4, "Pin Assignment and Package Information" and in the "Signal Multiplexing Scheme" table within the reference manual.

The connections of the pins in Table 2 depends solely upon the user application, however there are a few factory test signals that are not used in a normal application. Following is a list of these signals and how they are to be terminated for proper operation of the i.MX21S processor:

- CLKMODE[1:0]: To ensure proper operation, leave these signals as no connects.
- OSC26M_TEST: To ensure proper operation, leave this signal as no connect.
- EXT_48M: To ensure proper operation, connect this signal to ground.
- EXT_266M: To ensure proper operation, connect this signal to ground.
- TEST_WB[2:0]: These signals are also multiplexed with GPIO PORT E as well as alternate keypad signals. If not utilizing these signals for GPIO functionality or for their other multiplexed function, then configure as GPIO input with pull up enabled, and leave as a no connect.
- TEST_WB[4:3]: To ensure proper operation, leave these signals as no connects.

Table 2. i.MX21S Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip Select (EIM)	
A [25:0]	Address bus signals
D [31:0]	Data bus signals
$\overline{EB0}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24], shared with SDRAM DQM0.
$\overline{EB1}$	Byte Strobe—Active low external enable byte signal that controls D [23:16], shared with SDRAM DQM1.
$\overline{EB2}$	Byte Strobe—Active low external enable byte signal that controls D [15:8], shared with SDRAM DQM2 and PCMCIA $\overline{PC\_REG}$.
$\overline{EB3}$	LSB Byte Strobe—Active low external enable byte signal that controls D [7:0], shared with SDRAM DQM3 and PCMCIA $\overline{PC\_IORD}$.
$\overline{OE}$	Memory Output Enable—Active low output enables external data bus, shared with PCMCIA $\overline{PC\_IOWR}$.
$\overline{CS}$ [5:0]	Chip Select—The chip select signals $\overline{CS}$ [3:2] are multiplexed with $\overline{CSD}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR) in the System Control chapter. By default $\overline{CSD}$ [1:0] is selected. DTACK is multiplexed with $\overline{CS4}$.
$\overline{ECB}$	Active low input signal sent by flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
$\overline{LBA}$	Active low signal sent by flash device causing the external burst device to latch the starting burst address.
BCLK	Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
$\overline{RW}$	$\overline{RW}$ signal—Indicates whether external access is a read (high) or write (low) cycle. This signal is also shared with the PCMCIA $\overline{PC\_WE}$.
DTACK	DTACK signal—External input data acknowledge signal, multiplexed with $\overline{CS4}$.
Bootstrap	
BOOT [3:0]	System Boot Mode Select—The operational system boot mode upon system reset is determined by the settings of these pins. To hardwire these inputs low, terminate with a 1 KΩ resister to ground. For a logic high, terminate with a 1 KΩ resistor to VDDA. Do not change the state of these inputs after power-up. Boot 3 should always be tied to logic low.
SDRAM Controller	
SDBA [4:0]	SDRAM non-interleave mode bank address signals. These signals are multiplexed with address signals A[20:16].
SDIBA [3:0]	SDRAM interleave addressing mode bank address signals. These signals are multiplexed with address signals A[24:21].
MA [11:0]	SDRAM address signals. MA[9:0] are multiplexed with address signals A[10:1].
DQM [3:0]	SDRAM data qualifier mask multiplexed with $\overline{EB}$[3:0]. DQM3 corresponds to D[31:24], DQM2 corresponds to D[23:16], DQM1 corresponds to D[15:8], and DQM0 corresponds to D[7:0].
$\overline{CSD0}$	SDRAM Chip Select signal. This signal is multiplexed with the $\overline{CS2}$ signal. This signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter.
$\overline{CSD1}$	SDRAM Chip Select signal. This signal is multiplexed with the $\overline{CS3}$ signal. This signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter.
$\overline{RAS}$	SDRAM Row Address Select signal.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{CAS}$	SDRAM Column Address Select signal
$\overline{SDWE}$	SDRAM Write Enable signal
SDCKE0	SDRAM Clock Enable 0
SDCKE1	SDRAM Clock Enable 1
SDCLK	SDRAM Clock
Clocks and Resets	
EXTAL26M	Crystal input (26MHz), or a 16 MHz to 32 MHz oscillator (or square-wave) input when the internal oscillator circuit is shut down. When using an external signal source, feed this input with a square wave signal switching from GND to VDDA.
XTAL26M	Oscillator output to external crystal. When using an external signal source, float this output.
EXTAL32K	32 kHz or 32.768 kHz crystal input. When using an external signal source, feed this input with a square wave signal switching from GND to QVDD5.
XTAL32K	Oscillator output to external crystal. When using an external signal source, float this output.
CLKO	Clock Out signal selected from internal clock signals. Please refer to clock controller for internal clock selection.
EXT_48M	This is a special factory test signal. To ensure proper operation, connect this signal to ground.
EXT_266M	This is a special factory test signal. To ensure proper operation, connect this signal to ground.
$\overline{RESET\_IN}$	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset.
$\overline{RESET\_OUT}$	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{RESET\_IN}$), and Watchdog time-out.
$\overline{POR}$	Power On Reset—Active low Schmitt trigger input signal. The $\overline{POR}$ signal is normally generated by an external RC circuit designed to detect a power-up event.
CLKMODE[1:0]	These are special factory test signals. To ensure proper operation, leave these signals as no connects.
OSC26M_TEST	This is a special factory test signal. To ensure proper operation, leave this signal as a no connect.
TEST_WB[2:0]	These are special factory test signals. However, these signals are also multiplexed with GPIO PORT E as well as alternate keypad signals. If not using these signals for GPIO functions or for other multiplexed functions, then configure as GPIO input with pull-up enabled, and leave as a no connect.
TEST_WB[4:3]	These are special factory test signals. To ensure proper operation, leave these signals as no connects.
WKGD	Battery indicator input used to qualify the walk-up process. Also multiplexed with TIN.
JTAG For termination recommendations, see the Table "*JTAG pinouts*" in the *Multi-ICE® User Guide* from ARM® Limited.	
$\overline{TRST}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
TDO	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
JTAG_CTRL	JTAG Controller select signal—JTAG_CTRL is sampled during the rising edge of TRST. Must be pulled to logic high for proper JTAG interface to debugger. Pulling JTAG_CRTL low is for internal test purposes only.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
RTCK	JTAG Return Clock used to enhance stability of JTAG debug interface devices. This signal is multiplexed with 1-Wire, therefore using 1-Wire renders RTCK unusable and vice versa.
LCD Controller	
LD [17:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off. LD[15:0] signals are multiplexed with SLCDC1_DAT[15:0] from SLCDC1. LD[16] is multiplexed with $\overline{\text{EXT\_DMAGRANT}}$.
FLM_VSYNC (or simply referred to as VSYNC)	Frame Sync or Vsync—This signal also serves as the clock signal output for gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP_HSYNC (or simply referred to as HSYNC)	Line Pulse or HSync
LSCLK	Shift Clock.
OE_ACD	Alternate Crystal Direction/Output Enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Sampling start signal for left and right scanning. This signal is multiplexed with the SLCDC1_CLK.
PS	Control signal output for source driver (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_CS.
CLS	Start signal output for gate driver. This signal is invert version of PS (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_RS.
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal). This signal is multiplexed with SLCDC1_D0.
Smart LCD Controller	
SLCDC1_CLK	SLCDC Clock output signal. This signal is multiplexed and available at 2 alternate locations. These are SPL_SPR and SD2_CLK signals of LCDC and SD2, respectively.
SLCDC1_CS	SLCDC Chip Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are PS and SD2_CMD signals of LCDC and SD2, respectively.
SLCDC1_RS	SLCDC Register Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are CLS and SD2_D3 signals of LCDC and SD2, respectively.
SLCDC1_D0	SLCDC serial data output signal. This signal is multiplexed and available at 2 alternate signal locations. These are and REV and SD2_D2 signals of LCDC and SD2, respectively. This signal is inactive when a parallel data interface is used.
SLCDC1_DAT[15:0]	SLCDC Data output signals for connection to a parallel SLCD panel interface. These signals are multiplexed with LD[15:0] while an alternate 8-bit SLCD muxing is available on LD[15:8]. Further alternate muxing of these signals are available on some of the USB OTG and USBH1 signals.
SLCDC2_CLK	SLCDC Clock input signal for pass through to SLCD device. This signal is multiplexed with SSI3_CLK signal from SSI3.
SLCDC2_CS	SLCDC Chip Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_TXD signal from SSI3.
SLCDC2_RS	SLCDC Register Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_RXD signal from SSI3.
SLCDC2_D0	SLCD Data input signal for pass through to SLCD device. This signal is multiplexed with SSI3_FS signal from SSI3.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
External DMA	
EXT_DMAREQ	External DMA Request input signal. This signal is multiplexed with CSPI1_RDY.
EXT_DMAGRANT	External DMA Grant output signal. This signal is multiplexed with LD[16] of LCDC and CSPI1_SS1 of CSPI1.
NAND Flash Controller	
NF_CLE	NAND Flash Command Latch Enable output signal. Multiplexed with PC_POE of PCMCIA.
NF_CE	NAND Flash Chip Enable output signal. This signal is multiplexed with PC_CE1 of PCMCIA.
NF_WP	NAND Flash Write Protect output signal. This signal is multiplexed with PC_CE2 of PCMCIA.
NF_ALE	NAND Flash Address Latch Enable output signal. This signal is multiplexed with PC_OE of PCMCIA.
NF_RE	NAND Flash Read Enable output signal. This signal is multiplexed with PC_RW of PCMCIA.
NF_WE	NAND Flash Write Enable output signal. This signal is multiplexed with and PC_BVD2 of PCMCIA.
NF_RB	NAND Flash Ready Busy input signal. This signal is multiplexed with PC_RST of PCMCIA.
NF_IO[15:0]	NAND Flash Data input and output signals. NF_IO[15:7] signals are multiplexed with A[25:21] and A[15:13]. NF_IO[7:0] signals are multiplexed with several PCMCIA signals.
PCMCIA Controller	
PC_A[25:0]	PCMCIA Address signals. These signals are multiplexed with A[25:0].
PC_D[15:0]	PCMCIA Data input and output signals. These signals are multiplexed with D[15:0].
PC_CD1	PCMCIA Card Detect1 input signal. This signal is multiplexed with NFIO[7] signal of NF.
PC_CD2	PCMCIA Card Detect2 input signal. This signal is multiplexed with NFIO[6] signal of NF.
PC_WAIT	PCMCIA Wait input signal to extend current access. This signal is multiplexed with NFIO[5] signal of NF.
PC_READY	PCMCIA Ready input signal indicates card is ready for access. Multiplexed with NFIO[4] signal of NF.
PC_RST	PCMCIA Reset output signal. This signal is multiplexed with NFRB signal of NF.
PC_OE	PCMCIA Memory Read Enable output signal asserted during common or attribute memory read cycles. This signal is multiplexed with NFALE signal of NF.
PC_WE	PCMCIA Memory Write Enable output signal asserted during common or attribute memory cycles. This signal is shared with RW of the EIM.
PC_VS1	PCMCIA Voltage Sense1 input signal. This signal is multiplexed with NFIO[2] signal of NF.
PC_VS2	PCMCIA Voltage Sense2 input signal. This signal is multiplexed with NFIO[1] signal of NF.
PC_BVD1	PCMCIA Battery Voltage Detect1 input signal. This signal is multiplexed with NFIO[0] signal of NF.
PC_BVD2	PCMCIA Battery Voltage Detect2 input signal. This signal is multiplexed with NF_WE signal of NF.
PC_SPKOUT	PCMCIA Speaker Out output signal. This signal is multiplexed with PWMO signal.
PC_REG	PCMCIA Register Select output signal. This signal is shared with EB2 of EIM.
PC_CE1	PCMCIA Card Enable1 output signal. This signal is multiplexed with NFCE signal of NF.
PC_CE2	PCMCIA Card Enable2 output signal. This signal is multiplexed with NFWP signal of NF.
PC_IORD	PCMCIA IO Read output signal. This signal is shared with EB3 of EIM.
PC_IOWR	PCMCIA IO Write output signal. This signal is shared with OE signal of EIM.
PC_WP	PCMCIA Write Protect input signal. This signal is multiplexed with NFIO[3] signal of NF.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
PC_POE	PCMCIA Output Enable signal to enable voltage translation buffers and transceivers. This signal is multiplexed with NFCLE signal of NF.
$\overline{\text{PC\_RW}}$	PCMCIA Read Write output signal to control external transceiver direction. Asserted high for read access and negated low for write access. This signal is multiplexed with $\overline{\text{NFRE}}$ signal of NF.
PC_PWRON	PCMCIA input signal to indicate that the card power has been applied and stabilized.
CSPI	
CSPI1_MOSI	Master Out/Slave In signal
CSPI1_MISO	Master In/Slave Out signal
CSPI1_SS[2:0]	Slave Select (Selectable polarity) signal. CSPI1_SS2 is also multiplexed with USBG_RXDAT and CSPI1_SS1 is multiplexed with $\overline{\text{EXT\_DMAGRANT}}$.
CSPI1_SCLK	Serial Clock signal
CSPI1_$\overline{\text{RDY}}$	Serial Data Ready signal. Also multiplexed with $\overline{\text{EXT\_DMAREQ}}$.
CSPI2_MOSI	Master Out/Slave In signal. This signal is multiplexed with USBH2_TXDP signal of USB OTG.
CSPI2_MISO	Master In/Slave Out signal. This signal is multiplexed with USBH2_TXDM signal of USB OTG.
CSPI2_SS[2:0]	Slave Select (Selectable polarity) signals. These signals are multiplexed with USBH2_FS, USBH2_RXDP and USBH2_RXDM signal of USB OTG
CSPI2_SCLK	Serial Clock signal. This signal is multiplexed with $\overline{\text{USBH2\_OE}}$ signal of USB OTG
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to all 3 timers simultaneously. This signal is muxed with the Walk-up Guard Mode $\overline{\text{WKGD}}$ signal in the PLL, Clock, and Reset Controller module.
TOUT1 (or simply TOUT)	Timer Output signal from General Purpose Timer1 (GPT1). This signal is multiplexed with SYS_CLK1 and SYS_CLK2 signal of SSI1 and SSI2. The pin name of this signal is simply TOUT.
TOUT2	Timer Output signal from General Purpose Timer1 (GPT2). This signal is multiplexed with PWMO.
TOUT3	Timer Output signal from General Purpose Timer1 (GPT3). This signal is multiplexed with PWMO.
USB On-The-Go	
$\overline{\text{USB\_BYP}}$	USB Bypass input active low signal. This signal can only be used for USB function, not for GPIO.
USB_PWR	USB Power output signal
$\overline{\text{USB\_OC}}$	USB Over current input signal. This signal can only be used for USB function, not for GPIO.
USBG_RXDP	USB OTG Receive Data Plus input signal. This signal is muxed with SLCDC1_DAT15.
USBG_RXDM	USB OTG Receive Data Minus input signal. This signal is muxed with SLCDC1_DAT14.
USBG_TXDP	USB OTG Transmit Data Plus output signal. This signal is muxed with SLCDC1_DAT13.
USBG_TXDM	USB OTG Transmit Data Minus output signal. This signal is muxed with SLCDC1_DAT12.
USBG_RXDAT	USB OTG Transceiver differential data receive signal. Multiplexed with CSPI1_SS2.
$\overline{\text{USBG\_OE}}$	USB OTG Output Enable signal. This signal is muxed with SLCDC1_DAT11.
$\overline{\text{USBG\_ON}}$	USB OTG Transceiver ON output signal. This signal is muxed with SLCDC1_DAT9.
USBG_FS	USB OTG Full Speed output signal. This signal is multiplexed with external transceiver $\overline{\text{USBG\_TXR\_INT}}$ signal of USB OTG. This signal is muxed with SLCDC1_DAT10.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
USBH1_RXDP	USB Host1 Receive Data Plus input signal. This signal is multiplexed with UART4_RXD and SLCDC1_DAT6. It also provides an alternative multiplex for $\overline{\text{UART4\_RTS}}$, where this signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter.
USBH1_RXDM	USB Host1 Receive Data Minus input signal. This signal is muxed with SLCDC1_DAT5. It also provides an alternative multiplex for $\overline{\text{UART4\_CTS}}$.
USBH1_TXDP	USB Host1 Transmit Data Plus output signal. This signal is multiplexed with $\overline{\text{UART4\_CTS}}$ and SLCDC1_DAT4. It also provides an alternative multiplex for UART4_RXD, where this signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter.
USBH1_TXDM	USB Host1 Transmit Data Minus output signal. Multiplexed with UART4_TXD and SLCDC1_DAT3.
USBH1_RXDAT	USB Host1 Transceiver differential data receive signal. Multiplexed with USBH1_FS.
$\overline{\text{USBH1\_OE}}$	USB Host1 Output Enable signal. This signal is muxed with SLCDC1_DAT2.
USBH1_FS	USB Host1 Full Speed output signal. Multiplexed with $\overline{\text{UART4\_RTS}}$ and SLCDC1_DAT1 and USBH1_RXDAT.
$\overline{\text{USBH\_ON}}$	USB Host transceiver ON output signal. This signal is muxed with SLCDC1_DAT0.
USBG_SCL	USB OTG I^2C Clock input/output signal. This signal is multiplexed with SLCDC1_DAT8.
USBG_SDA	USB OTG I^2C Data input/output signal. This signal is multiplexed with SLCDC1_DAT7.
$\overline{\text{USBG\_TXR\_INT}}$	USB OTG transceiver interrupt input. Multiplexed with USBG_FS.
Secure Digital Interface	
SD1_CMD	SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4.7k–69k external pull-up resistor must be added.
SD1_CLK	SD Output Clock.
SD1_D[3:0]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50k–69k external pull-up resistor must be added.
SD2_CMD	SD Command bidirectional signal. This signal is multiplexed with SLCDC1_CS signal from SLCDC1.
SD2_CLK	SD Output Clock signal. This signal is multiplexed with SLCDC1_CLK signal from SLCDC1.
SD2_D[3:0]	SD Data bidirectional signals. SD2_D[3:2] are multiplexed with SLCDC1_RS and SLCDC_D0 signals from SLCDC1.
UARTs – IrDA/Auto-Bauding (Note: UART2 is not used in the MC9328MX21S)	
UART1_RXD	Receive Data input signal
UART1_TXD	Transmit Data output signal
$\overline{\text{UART1\_RTS}}$	Request to Send input signal
$\overline{\text{UART1\_CTS}}$	Clear to Send output signal
UART3_RXD	Receive Data input signal. This signal is multiplexed with IR_RXD from FIRI.
UART3_TXD	Transmit Data output signal. This signal is multiplexed with IR_TXD from FIRI.
$\overline{\text{UART3\_RTS}}$	Request to Send input signal
$\overline{\text{UART3\_CTS}}$	Clear to Send output signal
UART4_RXD	Receive Data input signal which is multiplexed with USBH1_RXDP and USBH1_TXDP.
UART4_TXD	Transmit Data output signal which is multiplexed with USBH1_TXDM.
$\overline{\text{UART4\_RTS}}$	Request to Send input signal which is multiplexed with USBH1_FS and USBH1_RXDP.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
$\overline{\text{UART4\_CTS}}$	Clear to Send output signal which is multiplexed with USBH1_TXDP and USBH1_RXDM.
Serial Audio Port – SSI (configurable to I^2S protocol and AC97)	
SSI1_CLK	Serial clock signal which is output in master or input in slave
SSI1_TXD	Transmit serial data
SSI1_RXD	Receive serial data
SSI1_FS	Frame Sync signal which is output in master and input in slave
SYS_CLK1	SSI1 master clock. Multiplexed with TOUT.
SSI2_CLK	Serial clock signal which is output in master or input in slave.
SSI2_TXD	Transmit serial data signal
SSI2_RXD	Receive serial data
SSI2_FS	Frame Sync signal which is output in master and input in slave.
SYS_CLK2	SSI2 master clock. Multiplexed with TOUT.
SSI3_CLK	Serial clock signal which is output in master or input in slave. Multiplexed with SLCDC2_CLK
SSI3_TXD	Transmit serial data signal which is multiplexed with SLCDC2_CS
SSI3_RXD	Receive serial data which is multiplexed with SLCDC2_RS
SSI3_FS	Frame Sync signal which is output in master and input in slave. Multiplexed with SLCDC2_D0.
SAP_CLK	Serial clock signal which is output in master or input in slave.
SAP_TXD	Transmit serial data
SAP_RXD	Receive serial data
SAP_FS	Frame Sync signal which is output in master and input in slave.
I^2C	
I2C_CLK	I^2C Clock
I2C_DATA	I^2C Data
1-Wire	
OWIRE	1-Wire input and output signal. This signal is multiplexed with JTAG RTCK.
PWM	
PWMO	PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module.
General Purpose Input/Output	
PB[10:21], PF[16]	Dedicated GPIO. When unused, program this signal as an input with the on-chip pull-up resistor enabled.
Keypad	
KP_COL[7:0]	Keypad Column selection signals. KP_COL[7:6] are multiplexed with $\overline{\text{UART2\_CTS}}$ and UART2_TXD respectively. Alternatively, KP_COL6 is also available on the internal factory test signal TEST_WB2. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signal KP_COL6 is available.

Table 2. i.MX21S Signal Descriptions (Continued)

Signal Name	Function/Notes
KP_ROW[7:0]	Keypad Row selection signals. KP_ROW[7:6] are multiplexed with $\overline{\text{UART2\_RTS}}$ and UART2_$\overline{\text{RXD}}$ signals respectively. Alternatively, KP_ROW7 and KP_ROW6 are available on the internal factory test signals TEST_WB0 and TEST_WB1 respectively. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signals KP_ROW6 and KP_ROW7 are available.
Noisy Supply Pins	
NVDD	Noisy Supply for the I/O pins. There are six (6) I/O voltages, NVDD1 through NVDD6.
NVSS	Noisy Ground for the I/O pins
Supply Pins – Analog Modules	
VDDA	Supply for analog blocks
QVSS (internally connected to AVSS)	Quiet GND for analog blocks (QVSS and AVSS are synonymous)
Internal Power Supplies	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Quiet GND pins for silicon internal circuitry
QVDDX	Power supply pin for the ARM core. Externally connect directly to QVDD

3 Specifications

This section contains the electrical specifications and timing diagrams for the i.MX21S processor.

3.1 Maximum Ratings

Table 3 provides the maximum ratings.

CAUTION

Stresses beyond those listed under "Maximum Ratings," (Table 3) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "266 MHz Recommended Operating Range" (Table 4) is not implied. Exposure to maximum-rated conditions for extended periods may affect device reliability.

Table 3. Maximum Ratings

Ref. Num	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	$QVDD_{max}$, $QVDDX_{max}$	-0.3	2.1	V
		$NVDD_{max}$, $VDDA_{max}$	-0.3	3.3	V
2	Input Voltage Range	V_{Imax}	-0.3	VDD + 0.3[1]	V
3	Storage Temperature Range	$T_{storage}$	-55	150	°C

1. VDD is the supply voltage associated with the input. See *Signal Multiplexing Scheme* table in the reference manual.

3.2 Recommended Operating Range

Table 4 provides the recommended operating ranges. The device has multiple pairs of VDD and VSS power supply and return pins. QVDD, QVDDx, and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because VDDA pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the VDDA pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 4.

Table 4. 266 MHz Recommended Operating Range

Rating		Symbol	Minimum	Maximum	Unit
Operating temperature range	**Part No. Suffix**				
	VK/VM	T_A	0	70	°C
	CVK/CVM	T_A	- 40	85	°C
I/O supply voltage NVDD 1–6		$NVDD_x$	1.70	3.30	V
Internal supply voltage (Core = 266 MHz)		QVDD, QVDDx	1.45	1.65	V
Analog supply voltage		VDDA	1.70	3.30	V

3.3 DC Electrical Characteristics

Table 5 contains the DC characteristics of the i.MX21S.

Table 5. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
High-level input voltage	V_{IH}	–	0.7NVDD	–	NVDD	
Low-level Input voltage	V_{IL}	–	O	–	0.3NVDD	
High-level output voltage	V_{OH}	I_{OH} = spec'ed Drive	0.8NVDD	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = spec'ed Drive	–	–	0.2NVDD	V
High-level output current, slow I/O	I_{OH_S}	V_{out}=0.8NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -2 -4 -8 -12	–	–	mA
High-level output current, fast I/O	I_{OH_F}	V_{out}=0.8NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 -3.5 -4.5 -5.5 -6.5	–	–	mA
Low-level output current, slow I/O	I_{OL_S}	V_{out}=0.2NVDD DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 2 4 8 12	–	–	mA

Table 5. DC Characteristics (Continued)

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Units
Low-level output current, fast I/O	I_{OL_F}	V_{out}=0.2NVDD1 DSCR[2] = 000 DSCR = 001 DSCR = 011 DSCR = 111	 3.5 4.5 5.5 6.5	–	–	mA
Schmitt trigger Positive–input threshold	V_T +	–	–	–	2.15	V
Schmitt trigger Negative–input threshold	V_T -		0.75	–	–	V
Hysteresis	V_{HYS}	–	–	0.3	–	V
Input leakage current (no pull-up or pull-down)	I_{in}	V_{in} = 0 or NVDD	–	–	±1	µA
I/O leakage current	I_{OZ}	$V_{I/O}$ = NVDD or 0 I/O = High impedance state	–	–	±5	µA

1. Data labeled Typical is not guaranteed, but is intended as an indication of the IC's potential performance.
2. For DSCR definition refer to the System Control chapter in the reference manual.

Table 6 shows the input and output capacitance for the device.

Table 6. Input/Output Capacitance

Parameter	Symbol	Min	Typ	Max	Units
Input capacitance	C_i	_	_	5	pF
Output capacitance	C_o	_	_	5	pF

Table 7 shows the power consumption for the device.

Table 7. Power Consumption

ID	Parameter	Conditions	Symbol	Typ	Max	Units
1	Run Current	QVDD = QVDDX = 1.65 V, NVDD1 = 1.8 V. NVDD2 through NVDD6 = VDDA = 3.1V. Core = 266 MHz, System = 133 MHz. MPEG4 Playback (QVGA) from MMC/SD card, 30fps, 44.1kHz audio.	I_{QVDD} + I_{QVDDX}	120	–	mA
			I_{NVDD1}	8	–	mA
			I_{NVDD2} through I_{NVDD6} + I_{VDDA}	6.6	–	mA
2	Sleep Current	Standby current with Well Biasing System enabled. Well Bias Control Register (WBCR) must be set as follows: WBCR: CRM_WBS bits = 01 CRM_WBFA bit = 1 CRM_WBM bits = 001 CRM_SPA_SEL bit = 1 FMCR bit = 1 For WBCR definition refer to System Control Chapter in the reference manual.	**I_{STBY}**			
			QVDD = QVDDX = 1.65V, TA[1]	–	3.0	mA
			QVDD = QVDDX = 1.65V, 25°	–	700	µA
			QVDD = QVDDX = 1.55V, 25°	320	–	µA

1. TA = 70°C for suffixes VK, VM, DVK, DVM, and SVK. TA = 85°C for suffixes CVK, CVM, and SCVK.

3.4 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency (HCLK) from 0 MHz to 133 MHz (core operating frequency 266 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading with the exception of fast I/O signals as discussed below. Refer to the reference manual's System Control Chapter for details on drive strength settings.

Table 8 provides the maximum loading guidelines that can be tolerated on a memory I/O signal (also known as Fast I/O) to achieve 133 MHz operation. These critical signals include the SDRAM Clock (SDCLK), Data Bus signals (D[31:0]), lower order address signals such as A0-A10, MA10, MA11, and other signals required to meet 133 MHz timing.

The values shown in Table 8 apply over the recommended operating temperature range. Care must be taken to minimize parasitic capacitance of associated printed circuit board traces.

Table 8. Loading Guidelines for Fast IO Signals to Achieve 133 MHz Operation

Drive Strength Setting (DSCR2–DSCR12)	Maximum I/O Loading at 1.8 V	Maximum I/O Loading at 3.0 V
000: 3.5 mA	9 pF	12 pF
001: 4.5 mA	12 pF	16 pF
011: 5.5 mA	15 pF	21 pF
111: 6.5 mA	19 pF	26 pF

Table 9. 32k/26M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak) for both System PLL and MCUPLL	–	5	20	ns
EXTAL32k input jitter (peak to peak) for MCUPLL only	–	5	100	ns
EXTAL32k startup time	800	–	–	ms

Table 10. CLKO Rise/Fall Time (at 30pF Loaded)

	Best Case	Typical	Worst Case	Units
Rise Time	0.80	1.00	1.40	ns
Fall Time	0.74	1.08	1.67	ns

3.5 DPLL Timing Specifications

Parameters of the DPLL are given in Table 11. In this table, T_{ref} is a reference clock period after the predivider and T_{dck} is the output double clock period.

Table 11. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
Reference clock frequency range	Vcc = 1.5V	16	–	320	MHz
Pre-divider output clock frequency range	Vcc = 1.5V	16	–	32	MHz
Double clock frequency range	Vcc = 1.5V	220	–	560	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Frequency lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	350	400	450	T_{ref}
Frequency lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	280	330	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	480	530	580	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	360	410	460	T_{ref}
Frequency jitter (p-p)	–	–	0.02	0.03	$2 \bullet T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.7V	–	1.0	1.5	ns
Power dissipation	FOL mode, integer MF, f_{dck} = 560 MHz, Vcc = 1.5V	–	1.5	–	mW (Avg)

3.6 Reset Module

The timing relationships of the Reset module with the $\overline{\text{POR}}$ and $\overline{\text{RESET\_IN}}$ are shown in Figure 2 and Figure 3. Be aware that NVDD must ramp up to at least 1.7V for NVDD1 and 2.7V for NVDD2-6 before QVDD is powered up to prevent forward biasing.

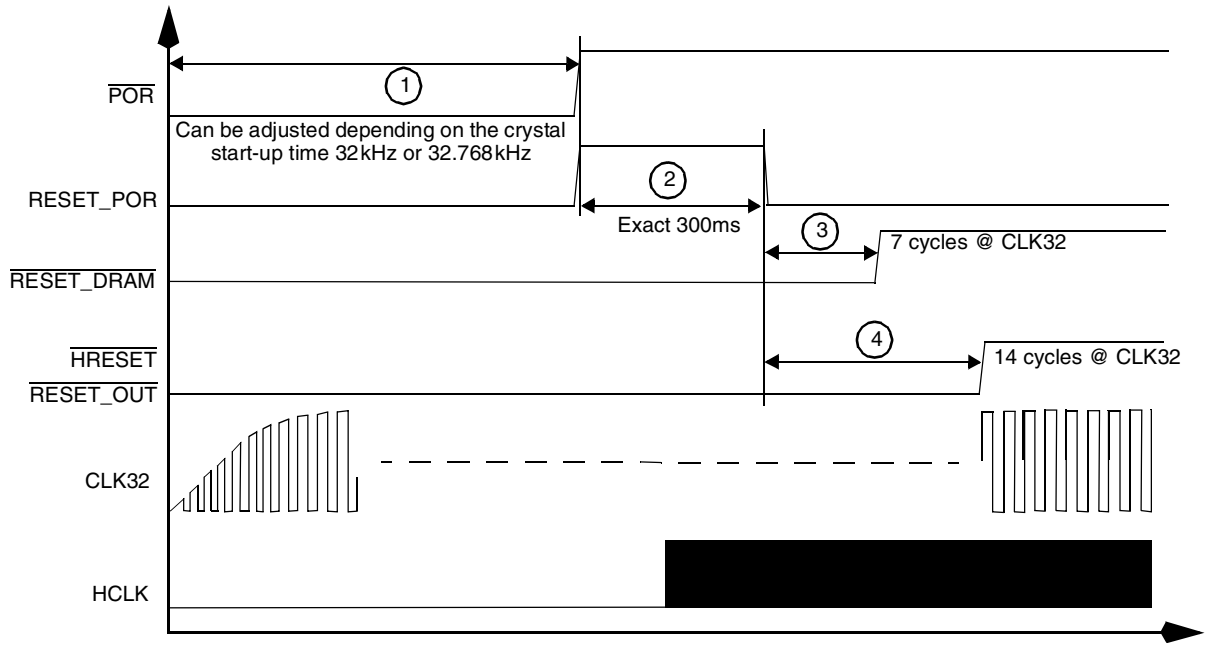


Figure 2. Timing Relationship with $\overline{\text{POR}}$

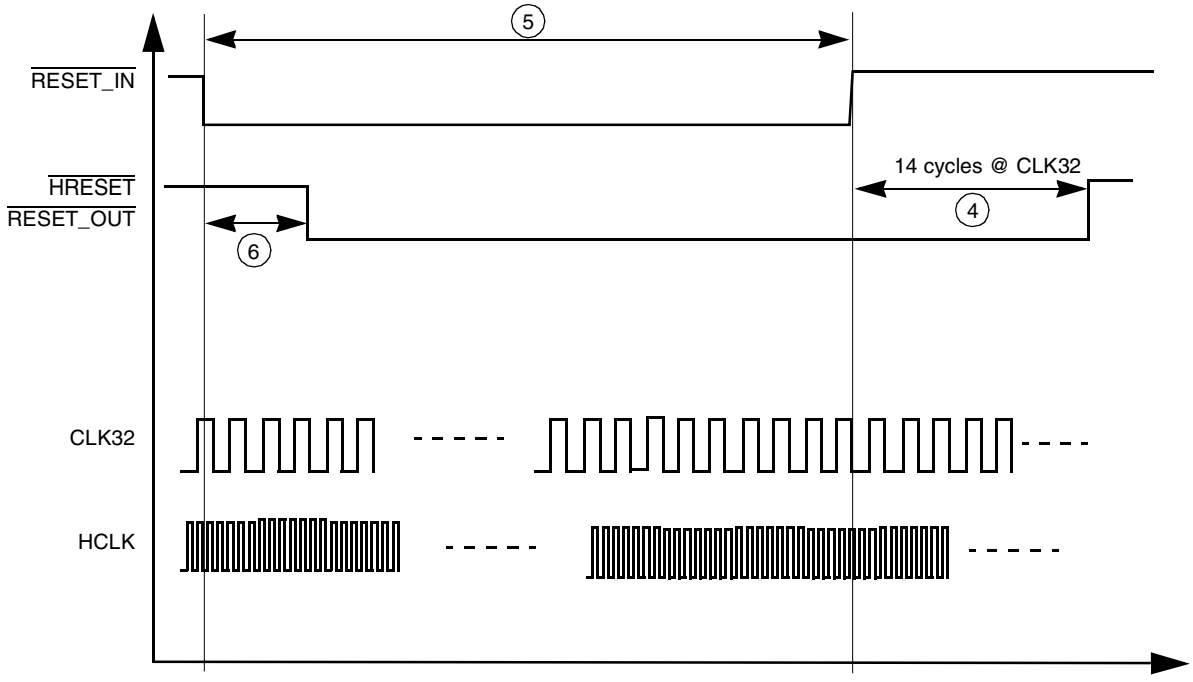


Figure 3. Timing Relationship with $\overline{\text{RESET\_IN}}$

Table 12. Reset Module Timing Parameters

Ref No.	Parameter	1.8 V ± 0.10 V		3.0 V ± 0.30 V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	800	–	800	–	ms
2	Width of internal $\overline{\text{POWER\_ON\_RESET}}$ (CLK32 at 32 kHz)	300	300	300	300	ms
3	7k to 32k-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14k to 32k-cycle stretcher for internal system reset $\overline{\text{HRESERT}}$ and output reset at pin $\overline{\text{RESET\_OUT}}$	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset $\overline{\text{RESET\_IN}}$	4	–	4	–	Cycles of CLK32
6	4k to 32k-cycle qualifier	4	4	4	4	Cycles of CLK32

3.7 External DMA Request and Grant

The External DMA request is an active low signal to be used by devices external to i.MX21 processor to request the DMAC for data transfer.

After assertion of External DMA request the DMA burst will start when the channel on which the External request is the source (as per the RSSR settings) becomes the current highest priority channel. The external device using the External DMA request should keep its request asserted until it is serviced by the DMAC. One External DMA request will initiate one DMA burst.

The output External Grant signal from the DMAC is an active-low signal.When the following conditions are true, the External DMA Grant signal is asserted with the initiation of the DMA burst.

- The DMA channel for which the DMA burst is ongoing has request source as external DMA Request (as per source select register setting).
- REN and CEN bit of this channel are set.
- External DMA Request is asserted.

After the grant is asserted, the External DMA request will not be sampled until completion of the DMA burst. As the external request is synchronized, the request synchronization will not be done during this period. The priority of the external request becomes low for the next consecutive burst, if another DMA request signal is asserted.

Worst case—that is, the smallest burst (1 byte read/write) timing diagrams are shown in Figure 4 and Figure 5. Minimum and maximum timings for the External request and External grant signals are present in Table 13.

Figure 4 shows the minimum time for which the External Grant signal remains asserted when an External DMA request is de-asserted immediately after sensing grant signal active.

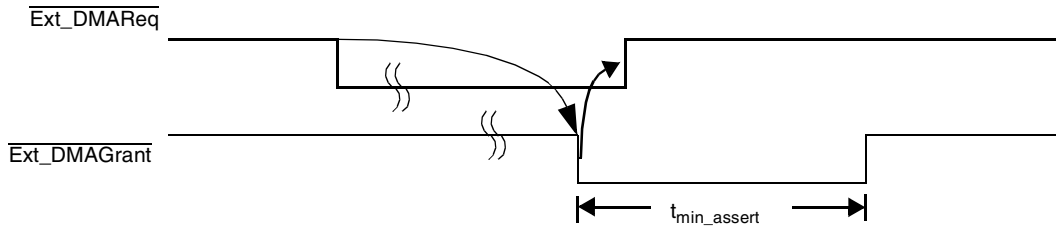
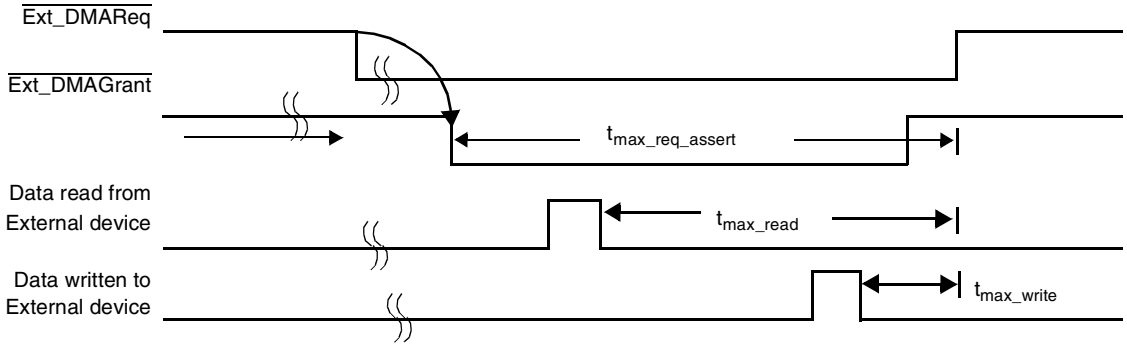


Figure 4. Assertion of DMA External Grant Signal

Figure 5 shows the safe maximum time for which External DMA request can be kept asserted, after sensing grant signal active such that a new burst is not initiated.



NOTE: Assuming in worst case the data is read/written from/to External device as per the above waveform.

Figure 5. Safe Maximum Timings for External Request De-Assertion

Table 13. DMA External Request and Grant Timing Parameters

Parameter	Description	3.0 V		1.8 V		Unit
		WCS	BCS	WCS	BCS	
t_{min_assert}	Minimum assertion time of External Grant signal	8 hclk + 8.6	8 hclk + 2.74	8 hclk + 7.17	8 hclk + 3.25	ns
$t_{max\_req\_assert}$	Maximum External request assertion time after assertion of Grant signal	9 hclk - 20.66	9 hclk - 6.7	9 hclk - 17.96	9 hclk - 8.16	ns
t_{max_read}	Maximum External request assertion time after first read completion	8 hclk - 6.21	8 hclk - 0.77	8 hclk - 5.84	8 hclk - 0.66	ns
t_{max_write}	Maximum External request assertion time after completion of first write	3 hclk - 15.87	3 hclk - 8.83	3 hclk - 15.9	3 hclk - 9.12	ns

3.8 CSPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the CSPI1 module is configured as a master, two control signals are used for data transfer rate control: the $\overline{SS}$ signal (output) and the $\overline{SPI\_RDY}$ signal (input). The SPI 1 Sample Period Control Register (PERIODREG1) and the SPI 2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either CSPI1 or CSPI2. When the CSPI1 module is configured as a slave, the user can configure the SPI 1 Control Register (CONTROLREG1) to match the external CSPI master's timing. In this configuration, $\overline{SS}$

becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO.

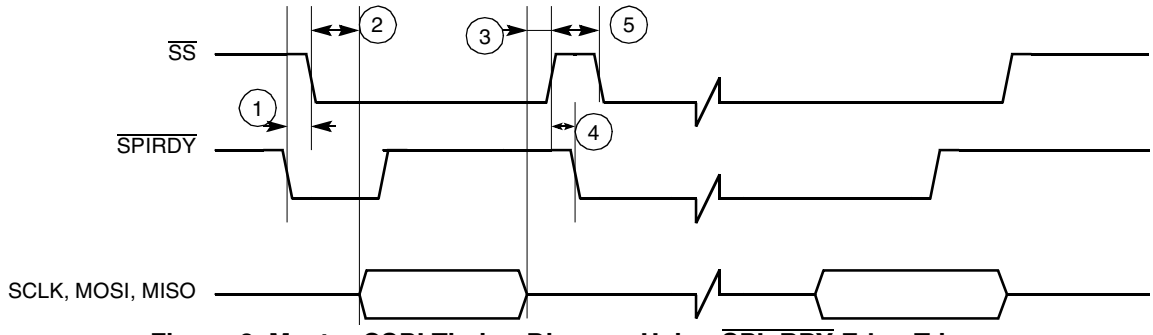


Figure 6. Master CSPI Timing Diagram Using SPI_RDY Edge Trigger

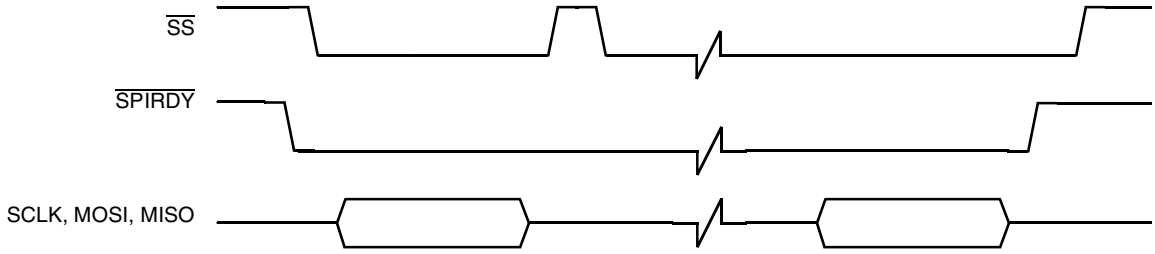


Figure 7. Master CSPI Timing Diagram Using SPI_RDY Level Trigger

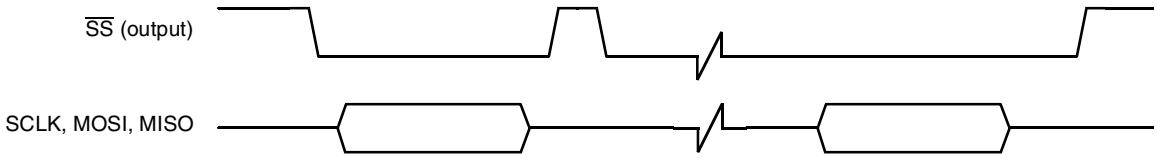


Figure 8. Master CSPI Timing Diagram Ignore SPI_RDY Level Trigger

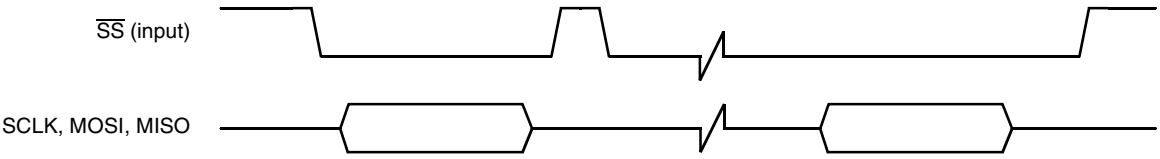


Figure 9. Slave CSPI Timing Diagram FIFO Advanced by BIT COUNT

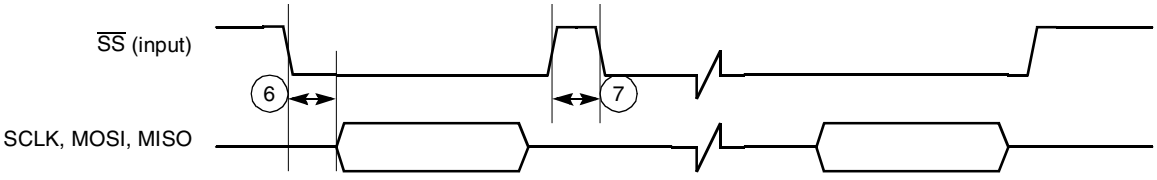


Figure 10. Slave CSPI Timing Diagram FIFO Advanced by SS Rising Edge

Table 14. Timing Parameters for Figure 6 through Figure 10

Ref No.	Parameter	Minimum	Maximum	Unit
1	$\overline{\text{SPI\_RDY}}$ to $\overline{\text{SS}}$ output low	2T [1]	–	ns
2	$\overline{\text{SS}}$ output low to first SCLK edge	3·Tsclk [2]	–	ns
3	Last SCLK edge to $\overline{\text{SS}}$ output high	2·Tsclk	–	ns
4	$\overline{\text{SS}}$ output high to $\overline{\text{SPI\_RDY}}$ low	0	–	ns
5	$\overline{\text{SS}}$ output pulse width	Tsclk + WAIT [3]	–	ns
6	$\overline{\text{SS}}$ input low to first SCLK edge	T	–	ns
7	$\overline{\text{SS}}$ input pulse width	T	–	ns

1. T = CSPI system clock period (PERCLK2).
2. Tsclk = Period of SCLK.
3. WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

3.9 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *i.MX21S Reference Manual*.

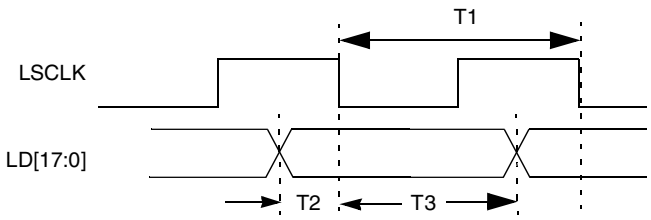


Figure 11. SCLK to LD Timing Diagram

Table 15. LCDC SCLK Timing Parameters

Symbol	Parameter	3.0 ± 0.3V		Unit
		Minimum	Maximum	
T1	SCLK period	23	2000	ns
T2	Pixel data setup time	11	–	ns
T3	Pixel data up time	11	–	ns
The pixel clock is equal to LCDC_CLK / (PCD + 1). When it is in CSTN, TFT or monochrome mode with bus width = 1, SCLK is equal to the pixel clock. When it is in monochrome with other bus width settings, SCLK is equal to the pixel clock divided by bus width. The polarity of SCLK and LD can also be programmed. Maximum frequency of SCLK is HCLK / 3 for TFT and CSTN, otherwise LD output will be incorrect.				

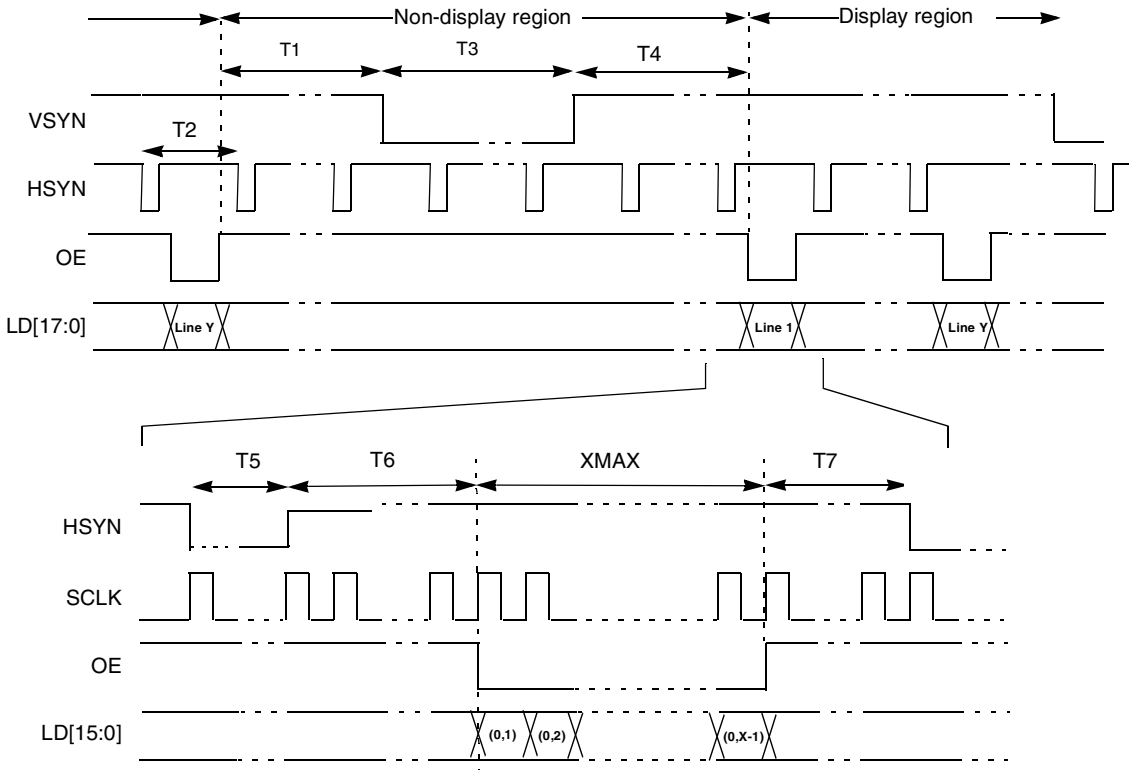


Figure 12. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Table 16. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	End of OE to beginning of VSYN	T5+T6+T7-1	(VWAIT1·T2)+T5+T6+T7-1	Ts
T2	HSYN period	–	XMAX+T5+T6+T7	Ts
T3	VSYN pulse width	T2	VWIDTH·T2	Ts
T4	End of VSYN to beginning of OE	1	(VWAIT2·T2)+1	Ts
T5	HSYN pulse width	1	HWIDTH+1	Ts
T6	End of HSYN to beginning to OE	3	HWAIT2+3	Ts
T7	End of OE to beginning of HSYN	1	HWAIT1+1	Ts

Note:
- Ts is the SCLK period.
- VSYN, HSYN and OE can be programmed as active high or active low. In Figure 12, all 3 signals are active low.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 12, SCLK is always active.
- XMAX is defined in number of pixels in one line.

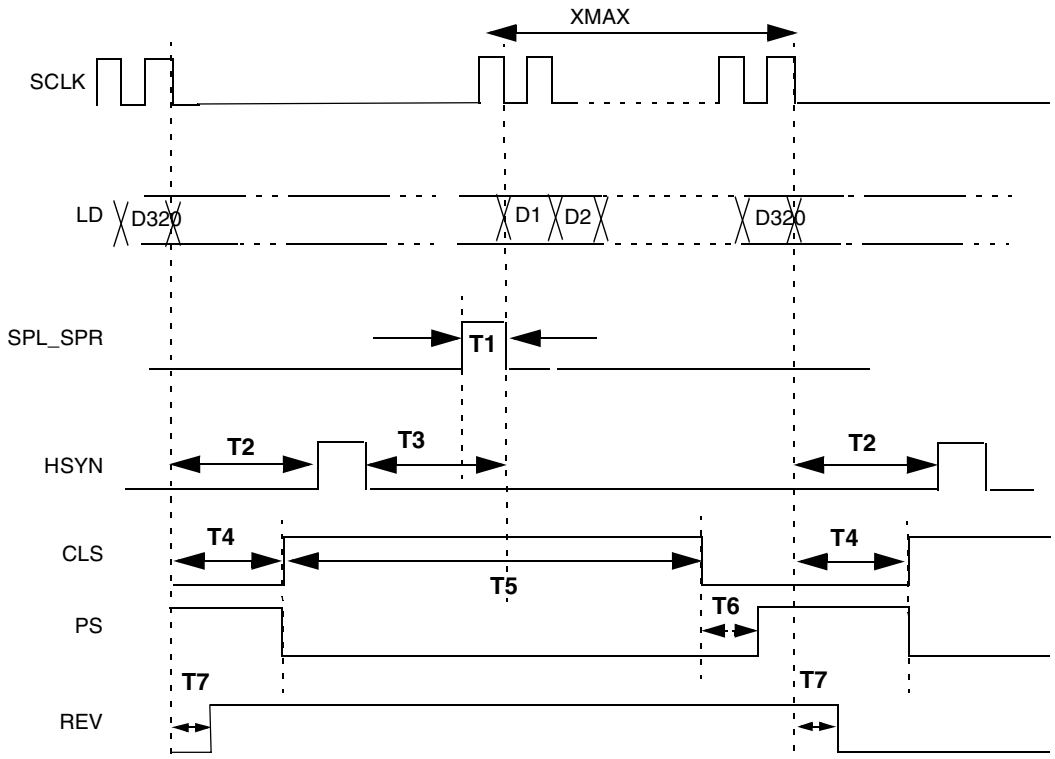


Figure 13. Sharp TFT Panel Timing

Table 17. Sharp TFT Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	SPL/SPR pulse width	–	1	Ts
T2	End of LD of line to beginning of HSYN	1	HWAIT1+1	Ts
T3	End of HSYN to beginning of LD of line	4	HWAIT2 + 4	Ts
T4	CLS rise delay from end of LD of line	3	CLS_RISE_DELAY+1	Ts
T5	CLS pulse width	1	CLS_HI_WIDTH+1	Ts
T6	PS rise delay from CLS negation	0	PS_RISE_DELAY	Ts
T7	REV toggle delay from last LD of line	1	REV_TOGGLE_DELAY+1	Ts

Note:
- Falling of SPL/SPR aligns with first LD of line.
- Falling of PS aligns with rising edge of CLS.
- REV toggles in every HSYN period.

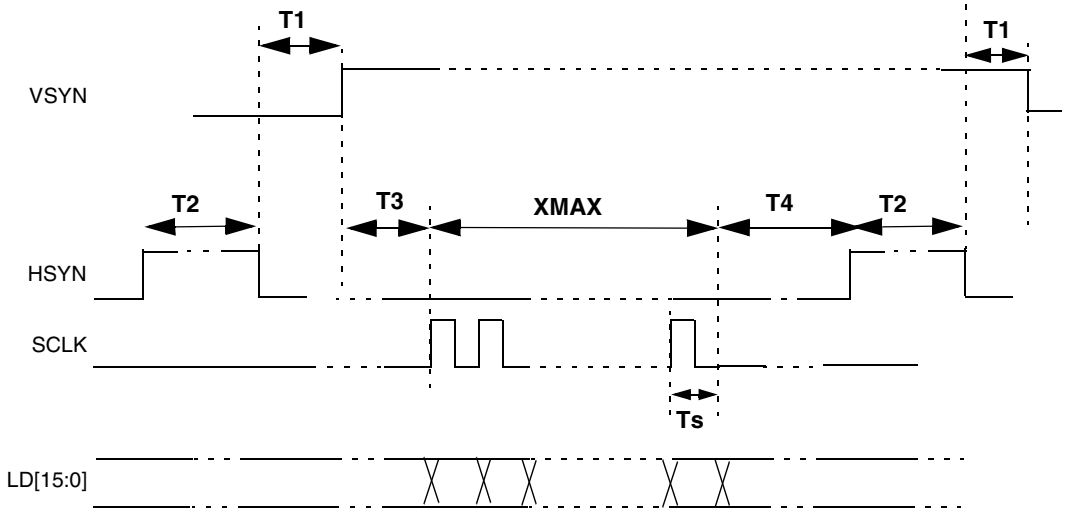


Figure 14. Non-TFT Mode Panel Timing

Table 18. Non-TFT Mode Panel Timing

Symbol	Description	Minimum	Value	Unit
T1	HSYN to VSYN delay	2	HWAIT2+2	Tpix
T2	HSYN pulse width	1	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	$0 \leq T3 \leq Ts$	–
T4	SCLK to HSYN	1	HWAIT1+1	Tpix

Note:
- Ts is the SCLK period while Tpix is the pixel clock period.
- VSYN, HSYN and SCLK can be programmed as active high or active low. In Figure 59, all these 3 signals are active high.
- When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts.
- When it is in monochrome mode with bus width = 2, 4, and 8, T3 = 1, 2 and 4 Tpix respectively.

3.10 Smart LCD Controller

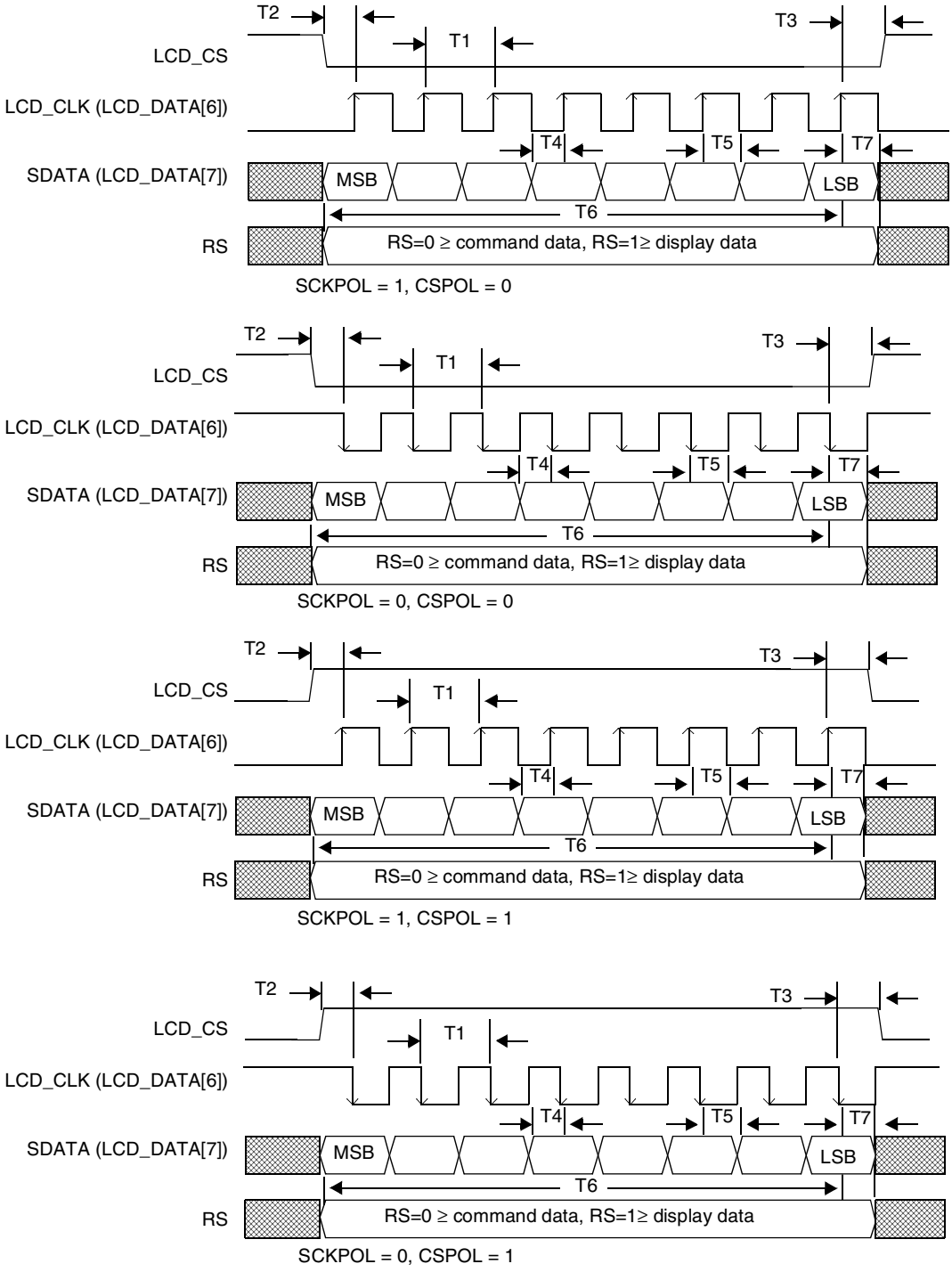


Figure 15. SLCDC Serial Transfer Timing