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Freescale Semiconductor
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Document Number: MC9328MXS
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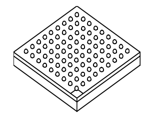
MC9328MXS



Package Information
Plastic Package
Case 1304B-01
(MAPBGA–225)

Ordering Information

See Table 1 on page 3

MC9328MXS

1 Introduction

The i.MX Family of applications processors provides a leap in performance with an ARM9™ microprocessor core and highly integrated system functions. The i.MX family specifically addresses the requirements of the personal, portable product market by providing intelligent integrated peripherals, an advanced processor core, and power management capabilities.

The MC9328MXS (i.MXS) processor features the advanced and power-efficient ARM920T™ core that operates at speeds up to 100 MHz. Integrated modules, which include a USB device and an LCD controller, support a suite of peripherals to enhance portable products. It is packaged in a 225-contact MAPBGA package. Figure 1 shows the functional block diagram of the i.MXS processor.

Contents

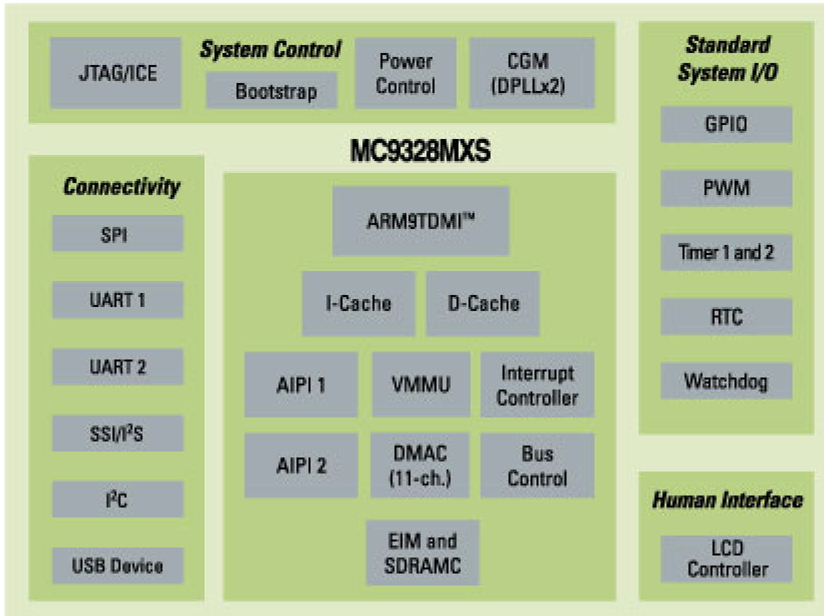


Figure 1. i.MXS Functional Block Diagram

1.1 Features

To support a wide variety of applications, the processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Two Universal Asynchronous Receiver/Transmitters (UART 1 and UART 2)
- Serial Peripheral Interface (SPI)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Direct Memory Access Controller (DMAC)
- Synchronous Serial Interface and an Inter-IC Sound (SSI/I^2S) Module
- Inter-IC (I^2C) Bus Module
- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode

- Power Management Features
- Operating Voltage Range: 1.7 V to 1.9 V core, 1.7 V to 3.3 V I/O
- 225-contact MAPBGA Package

1.2 Target Applications

The i.MXS applications processor is designed to meet the needs of medical instrumentation, low-end PDAs, point-of-sale terminals, security systems and other applications requiring a basic device based on ARM technology with support for open operating systems. Like other members of the i.MX family, the i.MXS is designed for high performance and low-power to maximize battery life.

1.3 Ordering Information

Table 1 provides ordering information.

Table 1. i.MXS Ordering Information

Package Type	Frequency	Temperature	Solderball Type	Order Number
225-contact MAPBGA	100 MHz	0°C to 70°C	Pb-free	MC9328MXSVP10(R2)
		-40°C to 85°C	Pb-free	MC9328MXSCVP10(R2)

1.4 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.
- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

2 Signals and Connections

Table 2 identifies and describes the i.MXS processor signals that are assigned to package pins. The signals are grouped by the internal module that they are connected to.

Table 2. i.MXS Signal Descriptions

Signal Name	Function/Notes
External Bus/Chip-Select (EIM)	
A[24:0]	Address bus signals
D[31:0]	Data bus signals
$\overline{EB0}$	MSB Byte Strobe—Active low external enable byte signal that controls D [31:24].
$\overline{EB1}$	Byte Strobe—Active low external enable byte signal that controls D [23:16].
$\overline{EB2}$	Byte Strobe—Active low external enable byte signal that controls D [15:8].
$\overline{EB3}$	LSB Byte Strobe—Active low external enable byte signal that controls D [7:0].
$\overline{OE}$	Memory Output Enable—Active low output enables external data bus.
$\overline{CS}$ [5:0]	Chip-Select—The chip-select signals $\overline{CS}$ [3:2] are multiplexed with $\overline{CSD}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR). By default $\overline{CSD}$ [1:0] is selected.
$\overline{ECB}$	Active low input signal sent by a flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
$\overline{LBA}$	Active low signal sent by a flash device causing the external burst device to latch the starting burst address.
BCLK (burst clock)	Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
$\overline{RW}$	$\overline{RW}$ signal—Indicates whether external access is a read (high) or write (low) cycle. Used as a $\overline{WE}$ input signal by external DRAM.
$\overline{DTACK}$	$\overline{DTACK}$ signal—The external input data acknowledge signal. When using the external DTACK signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external DTACK signal after 1022 clock counts have elapsed.
Bootstrap	
BOOT [3:0]	System Boot Mode Select—The operational system boot mode of the i.MXS processor upon system reset is determined by the settings of these pins.
SDRAM Controller	
SDBA [4:0]	SDRAM non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM cycles.
SDIBA [3:0]	SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles.
MA [11:10]	SDRAM address signals
MA [9:0]	SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles.
DQM [3:0]	SDRAM data enable
$\overline{CSD0}$	SDRAM Chip-select signal which is multiplexed with the $\overline{CS2}$ signal. These two signals are selectable by programming the system control register.

Table 2. i.MXS Signal Descriptions (Continued)

Signal Name	Function/Notes
CSD1	SDRAM Chip-select signal which is multiplexed with CS3 signal. These two signals are selectable by programming the system control register. By default, CSD1 is selected, so it can be used as boot chip-select by properly configuring BOOT [3:0] input pins.
RAS	SDRAM Row Address Select signal
CAS	SDRAM Column Address Select signal
SDWE	SDRAM Write Enable signal
SDCKE0	SDRAM Clock Enable 0
SDCKE1	SDRAM Clock Enable 1
SDCLK	SDRAM Clock
RESET_SF	Not Used
Clocks and Resets	
EXTAL16M	Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down.
XTAL16M	Crystal output
EXTAL32K	32 kHz crystal input
XTAL32K	32 kHz crystal output
CLKO	Clock Out signal selected from internal clock signals.
RESET_IN	Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset.
RESET_OUT	Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset (RESET_IN), and Watchdog time-out.
POR	Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event.
JTAG	
TRST	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
TDO	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
DMA	
DMA_REQ	DMA Request—external DMA request signal. Multiplexed with SPI1_SPI_RDY.
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to big endian. If it is driven logic-low at reset, the external chip-select space will be configured to little endian. This input must not change state after power-on reset negates or during chip operation.

Table 2. i.MXS Signal Descriptions (Continued)

Signal Name	Function/Notes
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIPESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIPESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with $\overline{\text{ECB}}$, $\overline{\text{LBA}}$, BCLK (burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SPI 1	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out
SPI1_$\overline{\text{SS}}$	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_$\overline{\text{SPI_RDY}}$	Serial Data Ready
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input

Table 2. i.MXS Signal Descriptions (Continued)

Signal Name	Function/Notes
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB Receive Data
USBD_ROE	USB OE
USBD_AFE	USB Analog Front End Enable
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
UART1_RTS	Request to Send
UART1_CTS	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
UART2_RTS	Request to Send
UART2_CTS	Clear to Send
UART2_DSR	Data Set Ready
UART2_RI	Ring Indicator
UART2_DCD	Data Carrier Detect
UART2_DTR	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^{2}S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I^{2}C	
I2C_SCL	I^{2}C Clock
I2C_SDA	I^{2}C Data
PWM	
PWMO	PWM Output
Test Function	
TRISTATE	Forces all I/O signals to high impedance for test purposes. For normal operation, terminate this input with a 1 k ohm resistor to ground. (TRI-STATE® is a registered trademark of National Semiconductor.)
General Purpose Input/Output	
PA[14:3]	Dedicated GPIO

Table 2. i.MXS Signal Descriptions (Continued)

Signal Name	Function/Notes
PB[13:8]	Dedicated GPIO
Digital Supply Pins	
NVDD	Digital Supply for the I/O pins
NVSS	Digital Ground for the I/O pins
Supply Pins – Analog Modules	
AVDD	Supply for analog blocks
Internal Power Supply	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Ground pins for silicon internal circuitry

2.1 I/O Pads Power Supply and Signal Multiplexing Scheme

This section describes detailed information about both the power supply for each I/O pin and its function multiplexing scheme. The user can reference information provided in Table 6 on page 17 to configure the power supply scheme for each device in the system (memory and external peripherals). The function multiplexing information also shown in Table 6 allows the user to select the function of each pin by configuring the appropriate GPIO registers when those pins are multiplexed to provide different functions.

Table 3. MC9328MXS Signal Multiplexing Scheme

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull -Up				
NVDD1	D2	A24	O		ETMTRACESYNC	O	PA0	69K	Reserved			A24
NVDD1	C1	D31	I/O	69K								
NVDD1	D1	A23	O		ETMTRACECLK	O	PA31	69K				A23
NVDD1	E3	D30	I/O	69K								
NVDD1	E2	A22	O		ETMPIPESTAT2	O	PA30	69K				A22
NVDD1	E4	D29	I/O	69K								
NVDD1	E1	A21	O		ETMPIPESTAT1	O	PA29	69K				A21
NVDD1	F3	D28	I/O	69K								
NVDD1	F1	A20	O		ETMPIPESTAT0	O	PA28	69K				A20
NVDD1	F4	D27	I/O	69K								
NVDD1	F2	A19	O		ETMTRACEPKT3	O	PA27	69K				A19
NVDD1	G3	D26	I/O	69K								

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull -Up				
NVDD1	G2	A18	O		ETMTRACEPKT2	O	PA26	69K				A18
NVDD1	G4	D25	I/O	69K								
NVDD1	G1	A17	O		ETMTRACEPKT1	O	PA25	69K				A17
NVDD1	H4	D24	I/O	69K								
NVDD1	H2	A16	O		ETMTRACEPKT0	O	PA24	69K				A16
NVDD1	H3	D23	I/O	69K								
NVDD1	H1	A15	O									
NVDD1	H5	D22	I/O	69K								
NVDD1	J1	A14	O									
NVDD1	J3	D21	I/O	69K								
NVDD1	K1	A13	O									
NVDD1	J4	D20	I/O	69K								
NVDD1	J2	A12	O									
NVDD1	K4	D19	I/O	69K								
NVDD1	K2	A11	O									
NVDD1	L4	D18	I/O	69K								
NVDD1	L1	A10	O									
NVDD1	L3	D17	I/O	69K								
NVDD1	L2	A9	O									
NVDD1	M1	D16	I/O	69K								
NVDD1	N1	A8	O									
NVDD1	M2	D15	I/O	69K								
NVDD1	N2	A7	O									
NVDD1	P1	D14	I/O	69K								
NVDD1	R1	A6	O									
NVDD1	M3	D13	I/O	69K								
NVDD1	P2	A5	O									
NVDD1	N3	D12	I/O	69K								
NVDD1	P3	A4	O									
NVDD1	R2	D11	I/O	69K								
NVDD1	N4	$\overline{EB0}$	O									
NVDD1	M4	D10	I/O	69K								
NVDD1	P4	A3	O									
NVDD1	R3	$\overline{EB1}$	O									
NVDD1	N5	D9	I/O	69K								
NVDD1	R4	$\overline{EB2}$	O									

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	P5	A2	O									
NVDD1	M5	EB3	O									
NVDD1	N6	D8	I/O	69K								
NVDD1	R5	OE	O									
NVDD1	P6	A1	O									
NVDD1	L7	CS5	O				PA23	69K				PA23
NVDD1	R6	D7	I/O	69K								
NVDD1	M7	CS4	O				PA22	69K				PA22
NVDD1	R7	A0	O				PA21	69K				A0
NVDD1	N7	CS3	O		CSD1							CSD1
NVDD1	P7	D6	I/O	69K								
NVDD1	K3	CS2	O		CSD0							CSD0
NVDD1	R8	SDCLK	O									
NVDD1	M8	CS1	O									
NVDD1	N8	CS0	O									
NVDD1	P8	D5	I/O	69K								
NVDD1	L9	ECB	I		ETMTRACEPKT7		PA20	69K				ECB
NVDD1	R9	D4	I/O	69K								
NVDD1	R10	LBA	O		ETMTRACEPKT6		PA19	69K				LBA
NVDD1	R11	D3	I/O	69K								
NVDD1	M9	BCLK			ETMTRACEPKT5		PA18	69K				BCLK
NVDD1	L8	D2	I/O	69K								
NVDD1	N9	PA17			ETMTRACEPKT4		PA17	69K	Reserved		DTACK	PA17
NVDD1	K10	D1	I/O	69K								
NVDD1	M10	RW										
NVDD1	P10	MA11	O									
NVDD1	P9	MA10	O									
NVDD1	N10	D0	I/O	69K								
NVDD1	R12	DQM3	O									
NVDD1	N11	DQM2	O									
NVDD1	P11	DQM1	O									
NVDD1	N12	DQM0	O									
NVDD1	P12	RAS	O									
NVDD1	R13	CAS	O									
NVDD1	R14	SDWE	O									

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	N13	SDCKE0	O									
NVDD1	P13	SDCKE1	O									
NVDD1	P15	$\overline{\text{RESET\_SF}}$	O									
NVDD1	P14	CLKO	O									
AVDD1	R15	AVDD1	Static									
QVDD2	M13	QVDD2	Static									
AVDD1	N15	$\overline{\text{TRST}}$	I	69K								
AVDD1	N14	TRISTATE[1]	I									
AVDD1	M15	EXTAL16M	I									
AVDD1	L14	XTAL16M	O									
AVDD1	L15	EXTAL32K	I									
AVDD1	K15	XTAL32K	O									
AVDD1	M14	$\overline{\text{RESET\_IN}}$[2]	I	69K								
AVDD1	K14	$\overline{\text{RESET\_OUT}}$	O									
AVDD1	L12	POR[2]	I									
AVDD1	K13	BIG_ENDIAN[3]	I									
AVDD1	M12	BOOT3[3]	I									
AVDD1	K11	BOOT2[3]	I									
AVDD1	J14	BOOT1[3]	I									
AVDD1	J15	BOOT0[3]	I									
NVDD2	J13	$\overline{\text{TDO}}$[4]	O									
NVDD2	H15	TMS	I	69K								
NVDD2	J12	TCK	I	69K								
NVDD2	K12	TDI	I	69K								
NVDD2	J11	I2C_SCL	O				PA16	69K				PA16
NVDD2	H14	I2C_SDA	I/O				PA15	69K				PA15
NVDD2	H13	Reserved	I				PA14	69K				PA14
NVDD2	G14	Reserved	I				PA13	69K				PA13
NVDD2	H12	Reserved	I				PA12	69K				PA12
NVDD2	G13	Reserved	I				PA11	69K				PA11
NVDD2	J10	Reserved	I				PA10	69K				PA10
NVDD2	G15	Reserved	I				PA9	69K				PA9

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary Signal	Primary Dir	Primary Pull-Up	Alternate Signal	Alternate Dir	GPIO Mux	GPIO Pull-Up	AIN	BIN	AOUT	Default
NVDD2	F15	Reserved	I				PA8	69K				PA8
NVDD2	G12	Reserved	I				PA7	69K				PA7
NVDD2	F14	Reserved	I				PA6	69K				PA6
NVDD2	H11	Reserved	I				PA5	69K				PA5
NVDD2	E14	Reserved	I				PA4	69K				PA4
NVDD2	E15	Reserved	O				PA3	69K				PA3
NVDD2	G11	PWMO	O				PA2	69K				PA2
NVDD2	E13	TIN	I				PA1	69K			Reserved	PA1
NVDD2	D14	TMR2OUT	O				PD31	69K		Reserved		PD31
NVDD2	F13	LD15	O				PD30	69K				PD30
NVDD2	F12	LD14	O				PD29	69K				PD29
NVDD2	D15	LD13	O				PD28	69K				PD28
NVDD2	C14	LD12	O				PD27	69K				PD27
NVDD2	D13	LD11	O				PD26	69K				PD26
NVDD2	E12	LD10	O				PD25	69K				PD25
NVDD2	C13	LD9	O				PD24	69K				PD24
NVDD2	C12	LD8	O				PD23	69K				PD23
NVDD2	B15	LD7	O				PD22	69K				PD22
NVDD2	B14	LD6	O				PD21	69K				PD21
NVDD2	A15	LD5	O				PD20	69K				PD20
NVDD2	A14	LD4	O				PD19	69K				PD19
NVDD2	B13	LD3	O				PD18	69K				PD18
NVDD2	A13	LD2	O				PD17	69K				PD17
NVDD2	D12	LD1	O				PD16	69K				PD16
NVDD2	B12	LD0	O				PD15	69K				PD15
NVDD2	C11	FLM/VSYNC	O				PD14	69K				PD14
NVDD2	D11	LP/HSYNC	O				PD13	69K				PD13
NVDD2	E11	ACD/OE	O				PD12	69K				PD12
NVDD2	C10	CONTRAST	O				PD11	69K				PD11
NVDD2	B11	SPL_SPR	O		$\overline{\text{UART2\_DSR}}$	O	PD10	69K	Reserved			PD10
NVDD2	A12	PS	O		$\overline{\text{UART2\_RI}}$	O	PD9	69K			Reserved	PD9
NVDD2	F10	CLS	O		$\overline{\text{UART2\_DCD}}$	O	PD8	69K	Reserved			PD8
NVDD2	A11	REV	O		$\overline{\text{UART2\_DTR}}$	I	PD7	69K	Reserved			PD7

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD2	B10	LSCLK	O				PD6	69K				PD6
NVDD3	D10	SPI1_MOSI	I/O				PC17	69K				PC17
NVDD3	E10	SPI1_MISO	I/O				PC16	69K				PC16
NVDD3	B9	SPI1_$\overline{\text{SS}}$	I/O				PC15	69K				PC15
NVDD3	A10	SPI1_SCLK	I/O				PC14	69K				PC14
NVDD3	A9	SPI1_$\overline{\text{SPI_RDY}}$	I/O				PC13	69K			$\overline{\text{DMA\_REQ}}$	PC13
NVDD3	E8	UART1_RXD	I				PC12	69K				PC12
NVDD3	B8	UART1_TXD	O				PC11	69K				PC11
NVDD3	C9	$\overline{\text{UART1\_RTS}}$	I				PC10	69K				PC10
NVDD3	E9	$\overline{\text{UART1\_CTS}}$	O				PC9	69K				PC9
NVDD3	A8	SSI_TXCLK	I/O				PC8	69K				PC8
NVDD3	C8	SSI_TXFS	I/O				PC7	69K				PC7
NVDD3	F9	SSI_TXDAT	O				PC6	69K				PC6
NVDD3	B7	SSI_RXDAT	I				PC5	69K				PC5
NVDD3	F8	SSI_RXCLK	I				PC4	69K				PC4
NVDD3	A7	SSI_RXFS	I				PC3	69K				PC3
NVDD4	C7	UART2_RXD	I				PB31	69K				PB31
NVDD4	D8	UART2_TXD	O				PB30	69K				PB30
NVDD4	E7	$\overline{\text{UART2\_RTS}}$	I				PB29	69K				PB29
NVDD4	F7	$\overline{\text{UART2\_CTS}}$	O				PB28	69K				PB28
NVDD4	B6	USBD_VMO	O				PB27	69K				PB27
NVDD4	C6	USBD_VPO	O				PB26	69K				PB26
NVDD4	A6	USBD_VM	I				PB25	69K				PB25
NVDD4	D6	USBD_VP	I				PB24	69K				PB24
NVDD4	A5	USBD_SUSPND	O				PB23	69K				PB23

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD4	B5	USBD_RCV	I/O				PB22	69K				PB22
NVDD4	A4	USBD_ROE	O				PB21	69K				PB21
NVDD4	B4	USBD_AFE	O				PB20	69K				PB20
NVDD4	A3	PB19	I/O					69K				PB19
NVDD4	C4	PB18	I/O					69K				PB18
NVDD4	D4	PB17	O					69K				PB17
NVDD4	B3	PB16	I					69K				PB16
NVDD4	A2	PB15	I					69K				PB15
NVDD4	C3	PB14	I					69K				PB14
NVDD4	A1	Reserved	I/O		Reserved		PB13	69K				PB13
NVDD4	B2	Reserved	O		Reserved		PB12	69K				PB12
NVDD4	B1	Reserved	I/O		Reserved		PB11	69K (pull down)				PB11
NVDD4	C5	Reserved	I/O		Reserved		PB10	69K				PB10
NVDD4	D3	Reserved	I/O		Reserved		PB9	69K				PB9
NVDD4	C2	Reserved	I/O		Reserved		PB8	69K				PB8
NVDD1	D5	NVDD1	Static									
	G6	NVSS	Static									
NVDD1	E5	NVDD1	Static									
	H6	NVSS	Static									
QVDD1	J8	QVDD1	Static									
	E6	QVSS	Static									
NVDD1	F5	NVDD	Static									
	J6	NVSS	Static									
NVDD1	G5	NVDD1	Static									
	K6	NVSS	Static									
NVDD1	J5	NVDD1	Static									
	H7	NVSS	Static									
NVDD1	K5	NVDD1	Static									
	J7	NVSS	Static									
NVDD1	L5	NVDD1	Static									
	G8	NVSS	Static									
NVDD1	L5	NVDD1	Static									
	H8	NVSS	Static									
	K7	QVSS	Static									

Table 3. MC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
		Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull -Up				
NVDD2	H10	NVDD2	Static									
	G9	NVSS	Static									
QVDD3	F11	QVDD3	Static									
	G10	QVSS	Static									
NVDD2	C15	NVDD2	Static									
	H9	NVSS	Static									
QVDD4	D7	QVDD4	Static									
	L13	QVSS	Static									
NVDD3	D9	NVDD3	Static									
	J9	NVSS	Static									
	K9	NVSS	Static									
NVDD4	G7	NVDD4	Static									
NVDD1	F6	NVDD1	Static									
NVDD1	L6	NVDD1	Static									
NVDD1	M6	NVDD1	Static									
NVDD1	K8	NVDD1	Static									
	L10	NVSS	Static									
	L11	NVSS	Static									
	M11	NVSS	Static									

1 Pull down this input with 1KΩ resistor to GND.

2 External circuit required to drive this input.

3 Tie this input high (to AVDD) or pull down with 1KΩ resistor to GND.

4 Pull up this output with a resistor to NVDD2.

3 Electrical Characteristics

This section contains the electrical specifications and timing diagrams for the i.MXS processor.

3.1 Maximum Ratings

Table 4 provides information on maximum ratings which are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits listed in Recommended Operating Range Table 5 on page 17 or the DC Characteristics table.

Table 4. Maximum Ratings

Symbol	Rating	Minimum	Maximum	Unit
NV_{DD}	DC I/O Supply Voltage	-0.3	3.3	V
QV_{DD}	DC Internal (core = 100 MHz) Supply Voltage	-0.3	1.9	V
AV_{DD}	DC Analog Supply Voltage	-0.3	3.3	V
$BTRFV_{DD}$	DC Bluetooth Supply Voltage	-0.3	3.3	V
VESD_HBM	ESD immunity with HBM (human body model)	–	2000	V
VESD_MM	ESD immunity with MM (machine model)	–	100	V
ILatchup	Latch-up immunity	–	200	mA
Test	Storage temperature	-55	150	°C
Pmax	Power Consumption	800[1]	1300[2]	mW

1 A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM® core-that is, 7x GPIO, 15x Data bus, and 8x Address bus.

2 A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core-that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at 100MHz, and where the whole image is running out of SDRAM. QVDD at 1.9V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

3.2 Recommended Operating Range

Table 5 provides the recommended operating ranges for the supply voltages and temperatures. The i.MXS processor has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.

Table 5. Recommended Operating Range

Symbol	Rating	Minimum	Maximum	Unit
T_A	Operating temperature range MC9328MXSVP10	0	70	°C
T_A	Operating temperature range MC9328MXSCVP10	-40	85	°C
NVDD	I/O supply voltage (if using SPI, LCD, and USBd which are only 3 V interfaces)	2.70	3.30	V
NVDD	I/O supply voltage (if not using the peripherals listed above)	1.70	3.30	V
QVDD	Internal supply voltage (Core = 100 MHz)	1.70	1.90	V
AVDD	Analog supply voltage	1.70	3.30	V

3.3 Power Sequence Requirements

For required power-up and power-down sequencing, please refer to the “Power-Up Sequence” section of application note AN2537 on the i.MX applications processor website.

3.4 DC Electrical Characteristics

Table 6 contains both maximum and minimum DC characteristics of the i.MXS processor.

Table 6. Maximum and Minimum DC Characteristics

Number or Symbol	Parameter	Min	Typical	Max	Unit
Iop	Full running operating current at 1.8V for QVDD, 3.3V for NVDD/AVDD (Core = 96 MHz, System = 96 MHz, driving TFT display panel, and OS with MMU enabled memory system is running on external SDRAM).	–	QVDD at 1.8V = 120mA; NVDD+AVDD at 3.0V = 30mA	–	mA
$Sidd_1$	Standby current (Core = 100 MHz, QVDD = 1.8V, temp = 25°C)	–	25	–	µA
$Sidd_2$	Standby current (Core = 100 MHz, QVDD = 1.8V, temp = 55°C)	–	45	–	µA
$Sidd_3$	Standby current (Core = 100 MHz, QVDD = 1.9V, temp = 25°C)	–	35	–	µA
$Sidd_4$	Standby current (Core = 100 MHz, QVDD = 1.9V, temp = 55°C)	–	60	–	µA
V_{IH}	Input high voltage	$0.7V_{DD}$	–	Vdd+0.2	V
V_{IL}	Input low voltage	–	–	0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0 mA)	$0.7V_{DD}$	–	Vdd	V
V_{OL}	Output low voltage (I_{OL} = -2.5 mA)	–	–	0.4	V
I_{IL}	Input low leakage current (V_{IN} = GND, no pull-up or pull-down)	–	–	±1	µA

Table 6. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Min	Typical	Max	Unit
I_{IH}	Input high leakage current ($V_{IN} = V_{DD}$, no pull-up or pull-down)	–	–	±1	μA
I_{OH}	Output high current ($V_{OH} = 0.8V_{DD}$, $V_{DD} = 1.8V$)	4.0	–	–	mA
I_{OL}	Output low current ($V_{OL} = 0.4V$, $V_{DD} = 1.8V$)	-4.0	–	–	mA
I_{OZ}	Output leakage current ($V_{out} = V_{DD}$, output is high impedance)	–	–	±5	μA
C_i	Input capacitance	–	–	5	pF
C_o	Output capacitance	–	–	5	pF

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 100 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading.

Table 7. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	–	20.8	ns

Table 8. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak)	–	5	20	ns
EXTAL32k startup time	800	–	–	ms
EXTAL16M input jitter (peak to peak) [1]	–	TBD	TBD	–
EXTAL16M startup time [1]	TBD	–	–	–

[1] The 16 MHz oscillator is not recommended for use in new designs.

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MXS.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

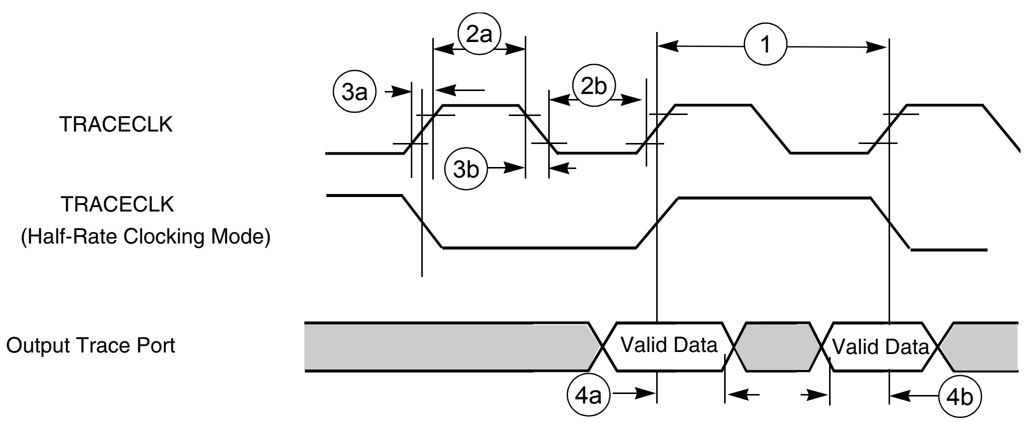


Figure 2. Trace Port Timing Diagram

Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns
4a	Output hold time	2.28	–	2	–	ns
4b	Output setup time	3.42	–	3	–	ns

4.2 DPLL Timing Specifications

Parameters of the DPLL are given in Table 10. In this table, T_{ref} is a reference clock period after the pre-divider and T_{dck} is the output double clock period.

Table 10. DPLL Specifications

Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
DPLL input clock freq range	Vcc = 1.8V	5	–	100	MHz
Pre-divider output clock freq range	Vcc = 1.8V	5	–	30	MHz
DPLL output clock freq range	Vcc = 1.8V	80	–	220	MHz
Pre-divider factor (PD)	–	1	–	16	–
Total multiplication factor (MF)	Includes both integer and fractional parts	5	–	15	–
MF integer part	–	5	–	15	–
MF numerator	Should be less than the denominator	0	–	1022	–
MF denominator	–	1	–	1023	–
Pre-multiplier lock-in time	–	–	–	312.5	µsec
Freq lock-in time after full reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	250	280 (56 µs)	300	T_{ref}
Freq lock-in time after partial reset	FOL mode for non-integer MF (does not include pre-multi lock-in time)	220	250 (50 µs)	270	T_{ref}
Phase lock-in time after full reset	FPL mode and integer MF (does not include pre-multi lock-in time)	300	350 (70 µs)	400	T_{ref}
Phase lock-in time after partial reset	FPL mode and integer MF (does not include pre-multi lock-in time)	270	320 (64 µs)	370	T_{ref}
Freq jitter (p-p)	–	–	0.005 (0.01%)	0.01	$2 \cdot T_{dck}$
Phase jitter (p-p)	Integer MF, FPL mode, Vcc=1.8V	–	1.0 (10%)	1.5	ns
Power supply voltage	–	1.7	–	2.5	V
Power dissipation	FOL mode, integer MF, f_{dck} = 100 MHz, Vcc = 1.8V	–	–	4	mW

4.3 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in Figure 3 and Figure 4.

NOTE

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

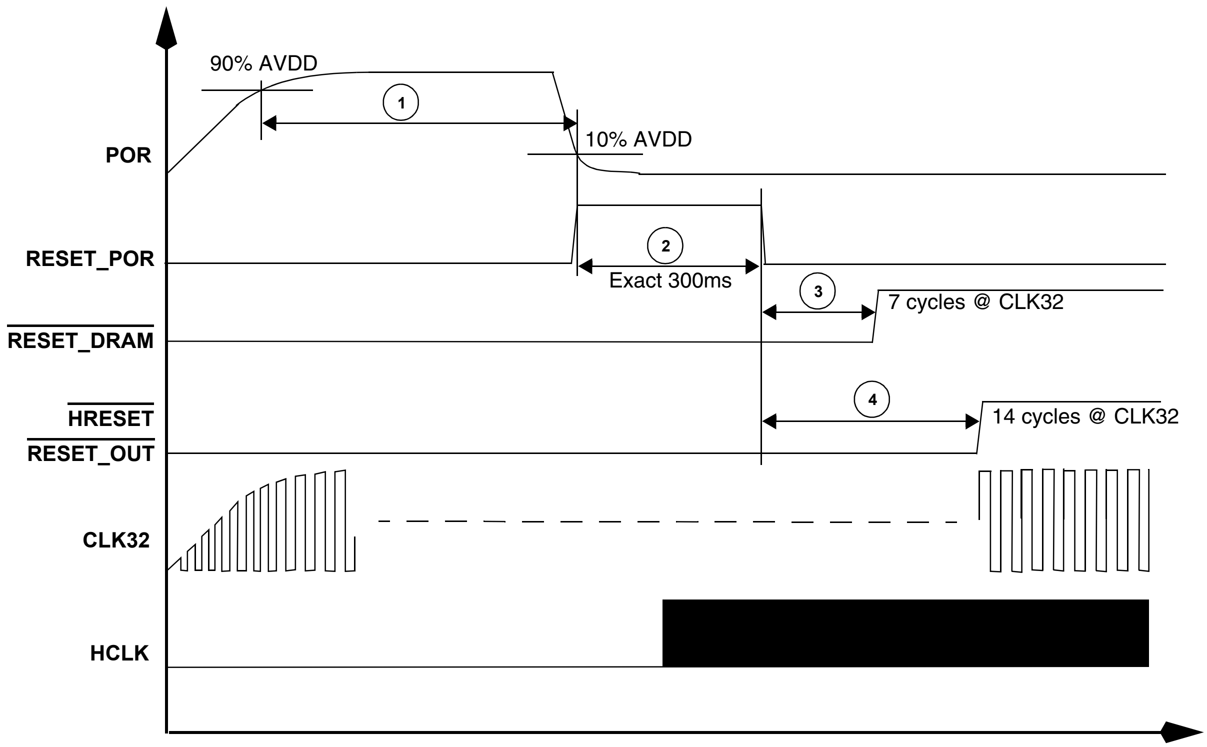


Figure 3. Timing Relationship with POR

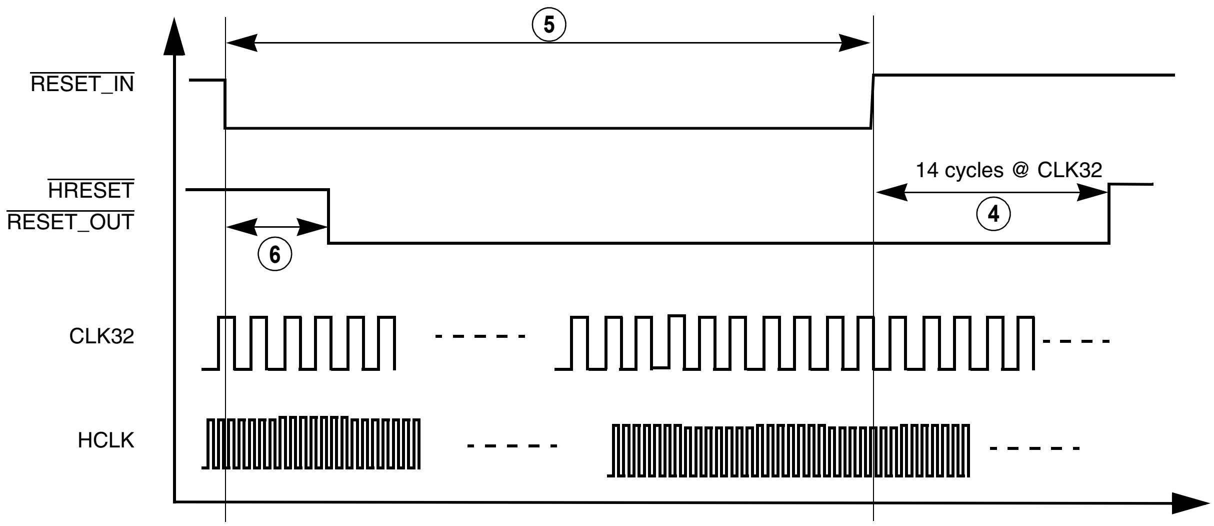


Figure 4. Timing Relationship with RESET_IN

Table 11. Reset Module Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	note[1]	–	note[1]	–	–
2	Width of internal $\overline{\text{POWER\_ON\_RESET}}$ (CLK32 at 32 kHz)	300	300	300	300	ms
3	7K to 32K-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14K to 32K-cycle stretcher for internal system reset $\overline{\text{HRESERT}}$ and output reset at pin $\overline{\text{RESET\_OUT}}$	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset $\overline{\text{RESET\_IN}}$	4	–	4	–	Cycles of CLK32
6	4K to 32K-cycle qualifier	4	4	4	4	Cycles of CLK32

[1] POR width is dependent on the 32 or 32.768 kHz crystal oscillator start-up time. Design margin should allow for crystal tolerance, i.MX chip variations, temperature impact, and supply voltage influence. Through the process of supplying crystals for use with CMOS oscillators, crystal manufacturers have developed a working knowledge of start-up time of their crystals. Typically, start-up times range from 400 ms to 1.2 seconds for this type of crystal.
If an external stable clock source (already running) is used instead of a crystal, the width of POR should be ignored in calculating timing for the start-up process.

4.4 External Interface Module

The External Interface Module (EIM) handles the interface to devices external to the i.MXS processor, including the generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.

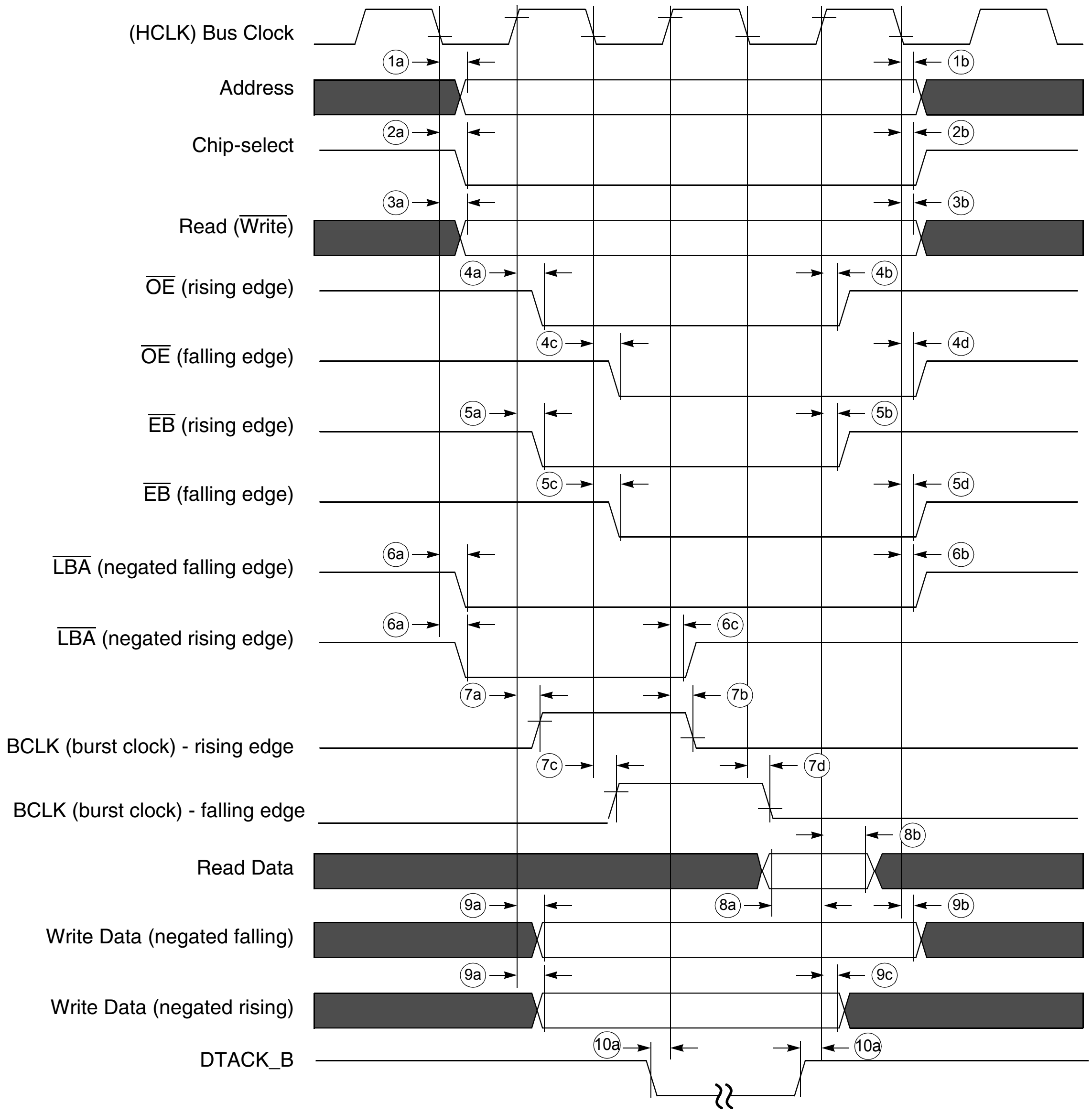


Figure 5. EIM Bus Timing Diagram

Table 12. EIM Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	2.48	3.31	9.11	2.4	3.2	8.8	ns
1b	Clock fall to address invalid	1.55	2.48	5.69	1.5	2.4	5.5	ns
2a	Clock fall to chip-select valid	2.69	3.31	7.87	2.6	3.2	7.6	ns
2b	Clock fall to chip-select invalid	1.55	2.48	6.31	1.5	2.4	6.1	ns
3a	Clock fall to Read (Write) Valid	1.35	2.79	6.52	1.3	2.7	6.3	ns
3b	Clock fall to Read (Write) Invalid	1.86	2.59	6.11	1.8	2.5	5.9	ns

Table 12. EIM Bus Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
4a	Clock[1] rise to Output Enable Valid	2.32	2.62	6.85	2.3	2.6	6.8	ns
4b	Clock[1] rise to Output Enable Invalid	2.11	2.52	6.55	2.1	2.5	6.5	ns
4c	Clock[1] fall to Output Enable Valid	2.38	2.69	7.04	2.3	2.6	6.8	ns
4d	Clock[1] fall to Output Enable Invalid	2.17	2.59	6.73	2.1	2.5	6.5	ns
5a	Clock[1] rise to Enable Bytes Valid	1.91	2.52	5.54	1.9	2.5	5.5	ns
5b	Clock[1] rise to Enable Bytes Invalid	1.81	2.42	5.24	1.8	2.4	5.2	ns
5c	Clock[1] fall to Enable Bytes Valid	1.97	2.59	5.69	1.9	2.5	5.5	ns
5d	Clock[1] fall to Enable Bytes Invalid	1.76	2.48	5.38	1.7	2.4	5.2	ns
6a	Clock[1] fall to Load Burst Address Valid	2.07	2.79	6.73	2.0	2.7	6.5	ns
6b	Clock[1] fall to Load Burst Address Invalid	1.97	2.79	6.83	1.9	2.7	6.6	ns
6c	Clock[1] rise to Load Burst Address Invalid	1.91	2.62	6.45	1.9	2.6	6.4	ns
7a	Clock[1] rise to Burst Clock rise	1.61	2.62	5.64	1.6	2.6	5.6	ns
7b	Clock[1] rise to Burst Clock fall	1.61	2.62	5.84	1.6	2.6	5.8	ns
7c	Clock[1] fall to Burst Clock rise	1.55	2.48	5.59	1.5	2.4	5.4	ns
7d	Clock[1] fall to Burst Clock fall	1.55	2.59	5.80	1.5	2.5	5.6	ns
8a	Read Data setup time	5.54	–	–	5.5	–	–	ns
8b	Read Data hold time	0	–	–	0	–	–	ns
9a	Clock[1] rise to Write Data Valid	1.81	2.72	6.85	1.8	2.7	6.8	ns
9b	Clock[1] fall to Write Data Invalid	1.45	2.48	5.69	1.4	2.4	5.5	ns
9c	Clock[1] rise to Write Data Invalid	1.63	–	–	1.62	–	–	ns
10a	$\overline{\text{DTACK}}$ setup time	2.52	–	–	2.5	–	–	ns

[1] Clock refers to the system clock signal, HCLK, generated from the System DPLL

4.4.1 $\overline{\text{DTACK}}$ Signal Description

The $\overline{\text{DTACK}}$ signal is the external input data acknowledge signal. When using the external $\overline{\text{DTACK}}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{\text{DTACK}}$ signal after 1022 HCLK counts have elapsed. Only the CS5 group supports DTACK signal function when the external DTACK signal is used for data acknowledgement.

4.4.2 $\overline{\text{DTACK}}$ Signal Timing

Figure 6 through Figure 9 show the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in the associated tables.

4.4.2.1 WAIT Read Cycle without DMA

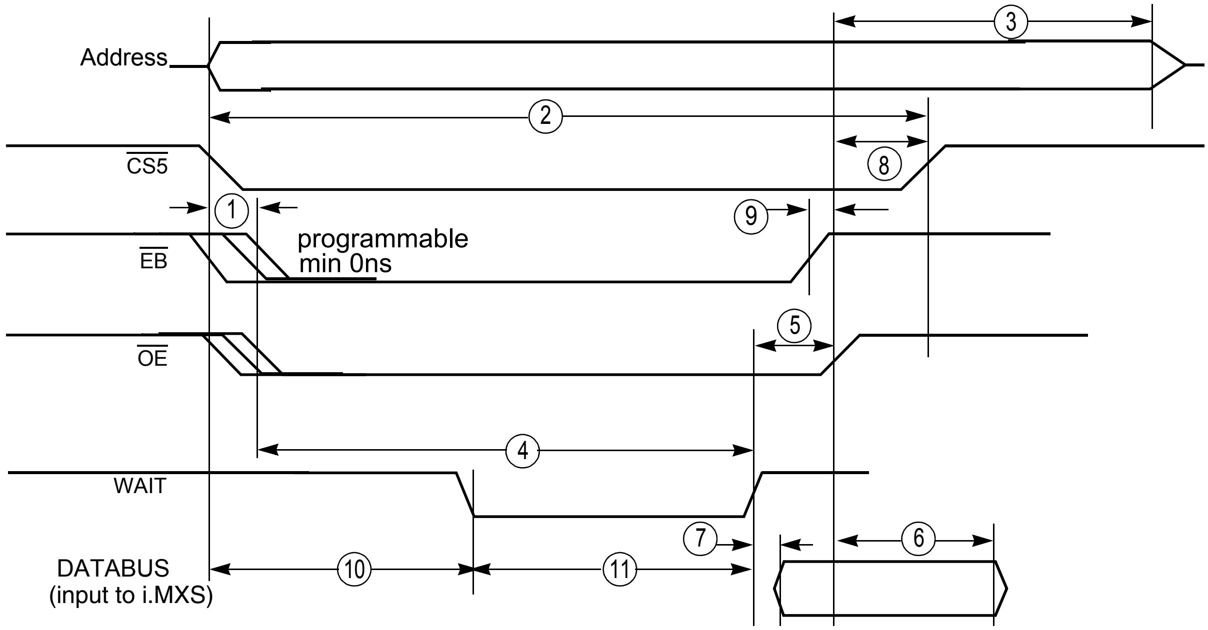


Figure 6. WAIT Read Cycle without DMA

Table 13. WAIT Read Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 2	–	ns
2	$\overline{CS5}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated to address inactive	56.81	57.28	ns
4	Wait asserted after $\overline{OE}$ asserted	–	1020T	ns
5	Wait asserted to $\overline{OE}$ negated	2T+1.57	3T+7.33	ns
6	Data hold timing after $\overline{OE}$ negated	T-1.49	–	ns
7	Data ready after wait asserted	0	T	ns
8	OE negated to CS negated	1.5T-0.68	1.5T-0.06	ns
9	OE negated after EB negated	0.06	0.18	ns
10	Become low after CS5 asserted	0	1019T	ns
11	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.