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Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

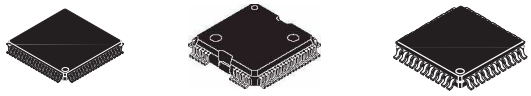
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08AC128
Rev. 4, 8/2011

MC9S08AC128 8-Bit Microcontroller Data Sheet

MC9S08AC128

917A-03 840B-01 824D-02



8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 20-MHz internal bus frequency
- HC08 instruction set with added BGND, CALL and RTC instructions
- Memory Management Unit to support paged memory.
- Linear Address Pointer to allow direct page data accesses of the entire memory map

Development Support

- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) Debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Supports both tag and force breakpoints.

Memory Options

- Up to 128K FLASH — read/program/erase over full operating voltage and temperature
- Up to 8K Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

Clock Source Options

- Clock source options include crystal, resonator, external clock, or internally generated clock with precision NVM trimming using ICG module

System Protection

- Optional computer operating properly (COP) reset with option to run from independent internal clock source or bus clock
- CRC module to support fast cyclic redundancy checks on system memory
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Master reset pin and power-on reset (POR)

Power-Saving Modes

- Wait plus two stops

Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5 μs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel
- **SCIx** — Two serial communications interface modules supporting LIN 2.0 Protocol and SAE J2602 protocols; Full duplex non-return to zero (NRZ); Master extended break generation; Slave extended break detection; Wakeup on active edge
- **SPIx** — One full and one master-only serial peripheral interface modules; Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Inter-integrated circuit bus module; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- **TPMx** — One 2-channel and two 6-channel 16-bit timer/pulse-width modulator (TPM) modules: Selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels
- **KBI** — 8-pin keyboard interrupt module

Input/Output

- Up to 70 general-purpose input/output pins
- Software selectable pullups on input port pins
- Software selectable drive strength and slew rate control on ports when used as outputs

Package Options

- 80-pin low-profile quad flat package (LQFP)
- 64-pin quad flat package (QFP)
- 48-pin quad flat no-lead package (QFN)
- 44-pin low-profile quad flat package (LQFP)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table of Contents

Related Documentation

MC9S08AC128 Series Reference Manual (MC9S08AC128RM)
contains extensive product information including modes of operartion, memory, resets and interrupts, register definitions, port pins, CPU, and all peripheral module information.

For the latest version of the documentation, check our website at:
http://www.freescale.com

Chapter 1
Device Overview

The MC9S08AC128 is a member of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). The MC9S08AC128 uses the enhanced HCS08 core.

1.1 MCU Block Diagram

The block diagram in Figure 1-1 shows the structure of the MC9S08AC128 Series MCU.

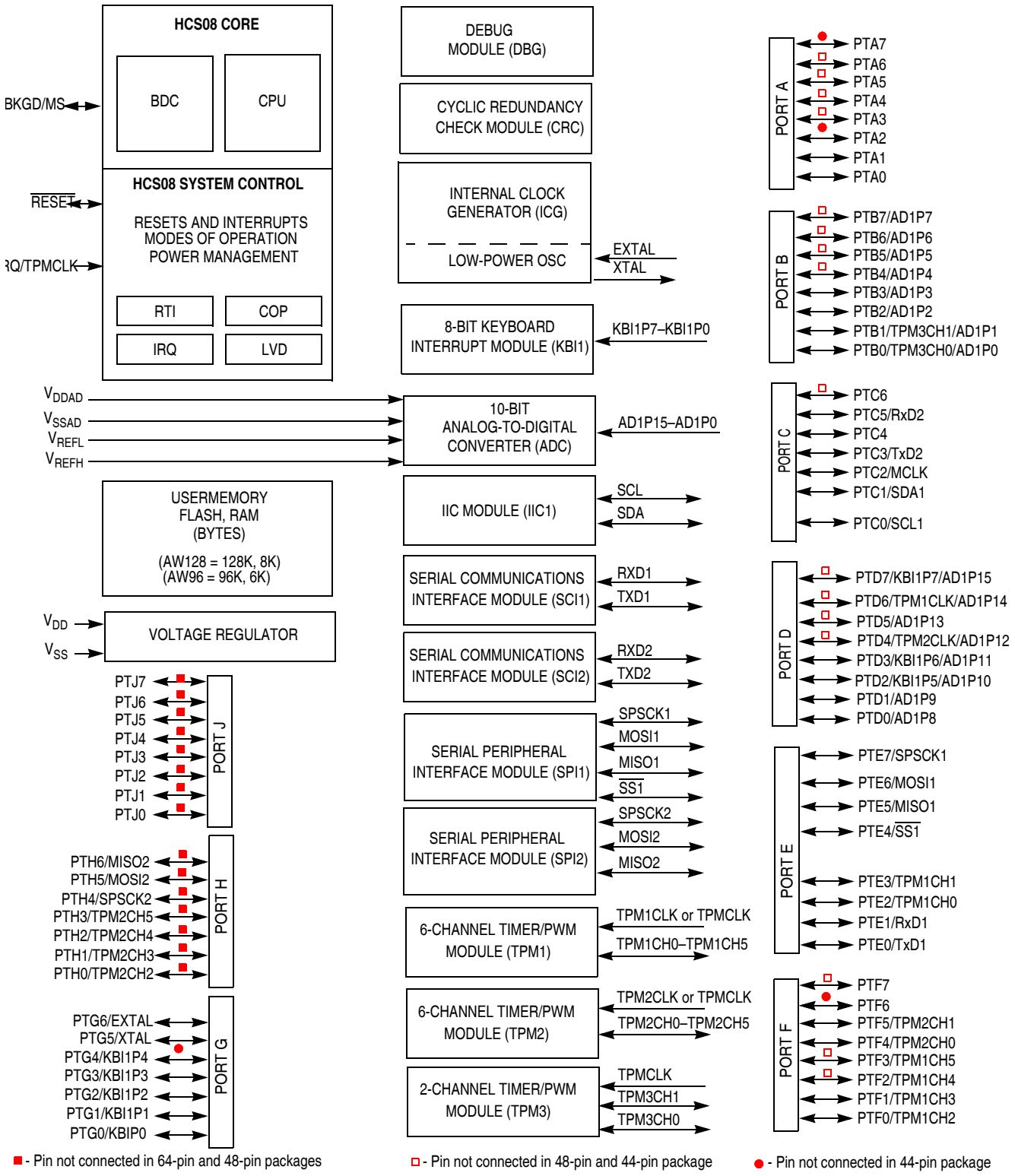


Figure 1-1. MC9S08AC128 Series Block Diagram

Chapter 2
Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

Figure 2-1 shows the 80-pin LQFP package pin assignments for the MC9S08AC128 Series device.

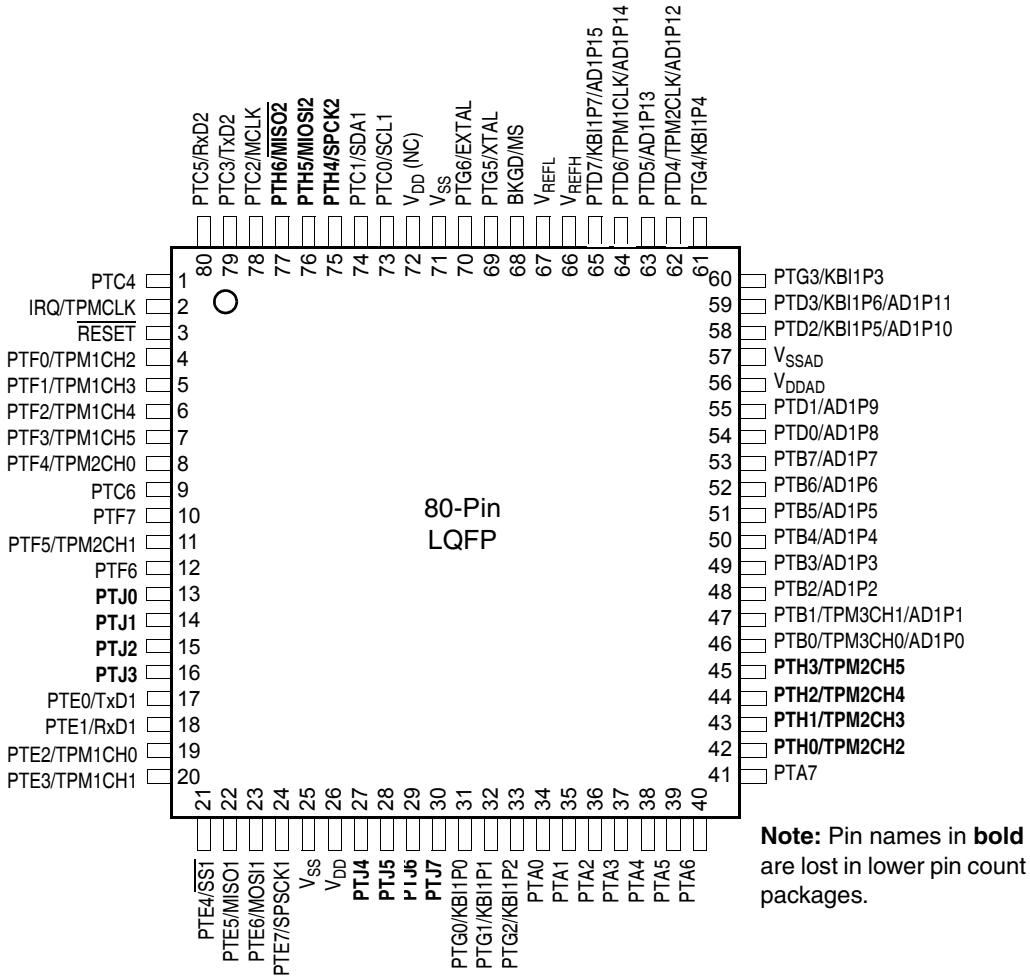


Figure 2-1. MC9S08AC128 Series in 80-Pin LQFP Package

Figure 2-2 shows the 64-pin package assignments for the MC9S08AC128 Series devices.

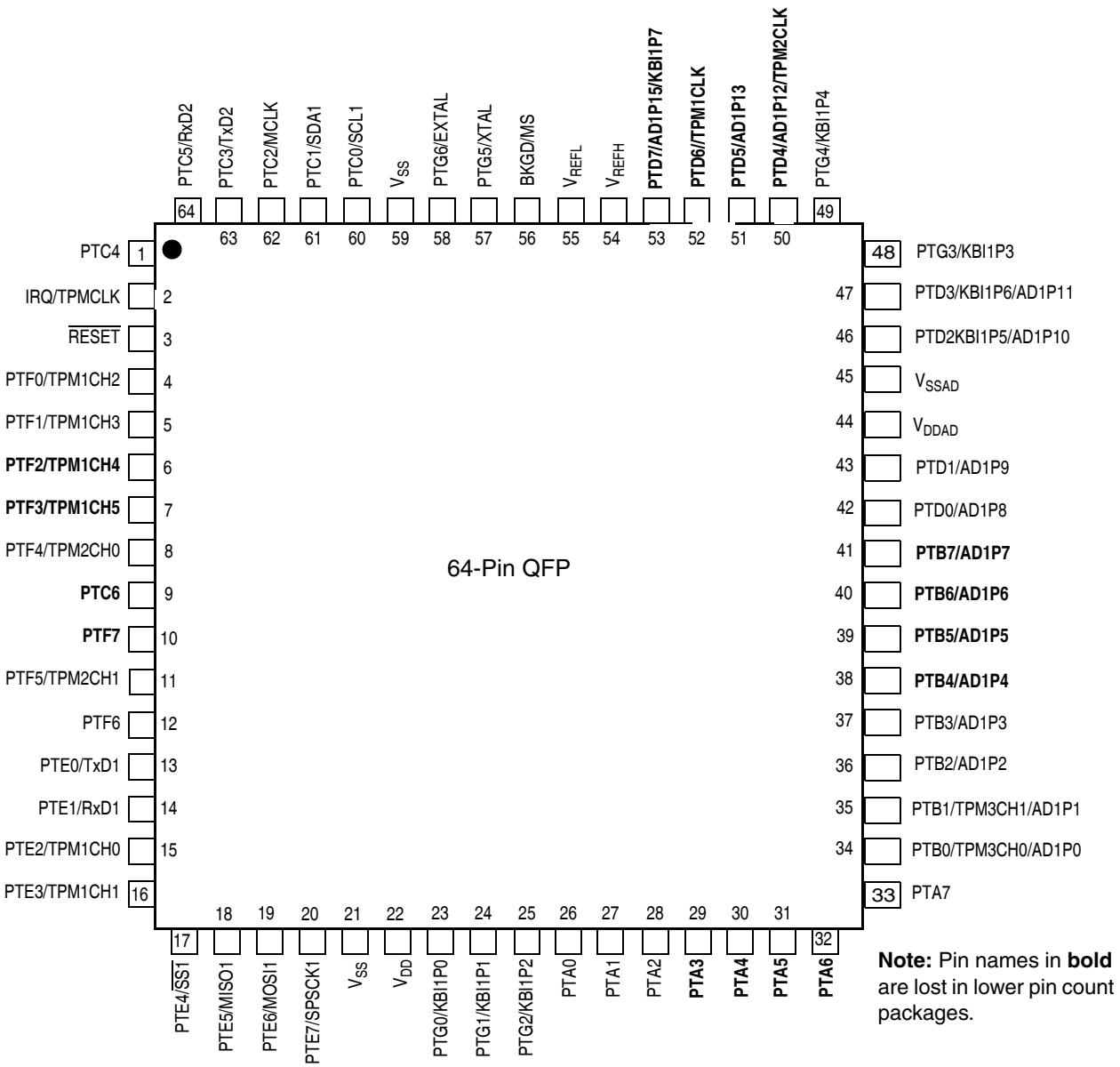
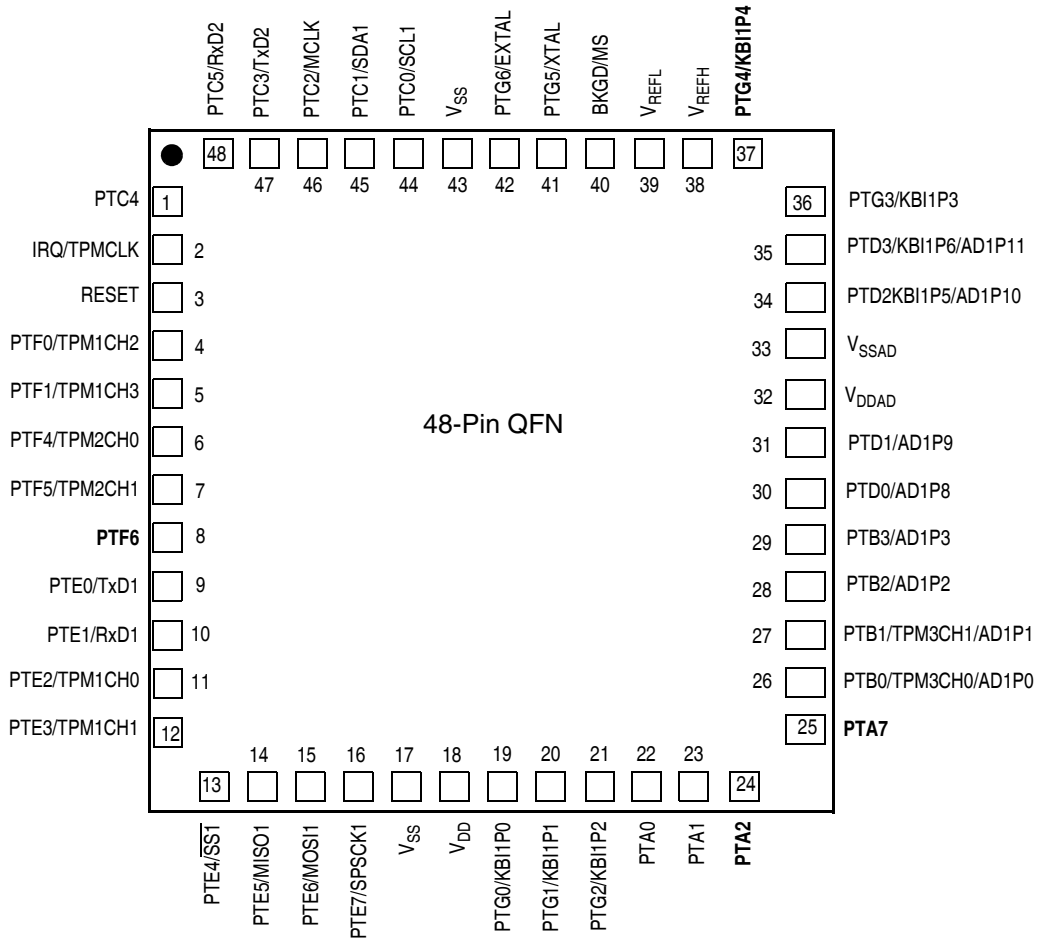


Figure 2-2. MC9S08AC128 Series in 64-Pin QFP Package

Figure 2-1 shows the 48-pin package assignments for the MC9S08AC128 Series devices.



Note: Pin names in **bold** are lost in lower pin count packages.

Figure 2-1. MC9S08AC128 Series in 48-Pin QFN Package

Figure 2-3 shows the 44-pin LQFP pin assignments for the MC9S08AC128 Series device.

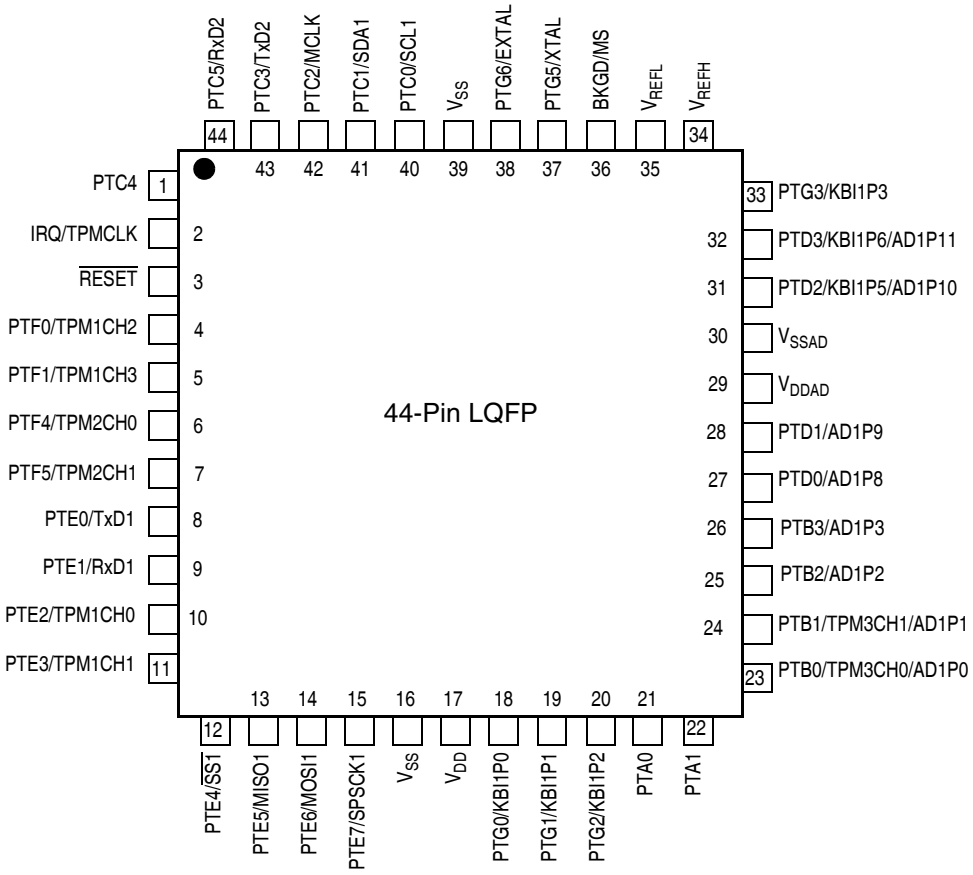


Figure 2-3. MC9S08AC128 Series in 44-Pin LQFP Package

Table 2-4. Pin Availability by Package Pin-Count

Pin Number				Lowest <-- Priority --> Highest		
80	64	48	44	Port Pin	Alt 1	Alt 2
1	1	1	1	PTC4		
2	2	2	2	IRQ	TPMCLK[1]	
3	3	3	3	RESET		
4	4	4	4	PTF0	TPM1CH2	
5	5	5	5	PTF1	TPM1CH3	
6	6	—	—	PTF2	TPM1CH4	
7	7	—	—	PTF3	TPM1CH5	
8	8	6	6	PTF4	TPM2CH0	
9	9	—	—	PTC6		
10	10	—	—	PTF7		
11	11	7	7	PTF5	TPM2CH1	
12	12	8	—	PTF6		

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
13	—	—	—	PTJ0		
14	—	—	—	PTJ1		
15	—	—	—	PTJ2		
16	—	—	—	PTJ3		
17	13	9	8	PTE0	TxD1	
18	14	10	9	PTE1	RxD1	
19	15	11	10	PTE2	TPM1CH0	
20	16	12	11	PTE3	TPM1CH1	
21	17	13	12	PTE4	$\overline{SS1}$	
22	18	14	13	PTE5	MISO1	
23	19	15	14	PTE6	MOSI1	
24	20	16	15	PTE7	SPSCK1	
25	21	17	16	V_{SS}		
26	22	18	17	V_{DD}		
27	—	—	—	PTJ4		
28	—	—	—	PTJ5		
29	—	—	—	PTJ6		
30	—	—	—	PTJ7		
31	23	19	18	PTG0	KBI1P0	
32	24	20	19	PTG1	KBI1P1	
33	25	21	20	PTG2	KBI1P2	
34	26	22	21	PTA0		
35	27	23	22	PTA1		
36	28	24	—	PTA2		
37	29	—	—	PTA3		
38	30	—	—	PTA4		
39	31	—	—	PTA5		
40	32	—	—	PTA6		
41	33	25	—	PTA7		
42	—	—	—	PTH0	TPM2CH2	
43	—	—	—	PTH1	TPM2CH3	
44	—	—	—	PTH2	TPM2CH4	
45	—	—	—	PTH3	TPM2CH5	
46	34	26	23	PTB0	TPM3CH0	AD1P0
47	35	27	24	PTB1	TPM3CH1	AD1P1
48	36	28	25	PTB2	AD1P2	
49	37	29	26	PTB3	AD1P3	
50	38	—	—	PTB4	AD1P4	
51	39	—	—	PTB5	AD1P5	
52	40	—	—	PTB6	AD1P6	
53	41	—	—	PTB7	AD1P7	

Table 2-4. Pin Availability by Package Pin-Count (continued)

Pin Number				Lowest <-- Priority --> Highest		
80	**64**	**48**	**44**	**Port Pin**	**Alt 1**	**Alt 2**
54	42	30	27	PTD0	AD1P8	
55	43	31	28	PTD1	AD1P9	
56	44	32	29	V_{DDAD}		
57	45	33	30	V_{SSAD}		
58	46	34	31	PTD2	KBI1P5	AD1P10
59	47	35	32	PTD3	KBI1P6	AD1P11
60	48	36	33	PTG3	KBI1P3	
61	49	37	—	PTG4	KBI1P4	
62	50	—	—	PTD4	TPM2CLK	AD1P12
63	51	—	—	PTD5	AD1P13	
64	52	—	—	PTD6	TPM1CLK	AD1P14
65	53	—	—	PTD7	KBI1P7	AD1P15
66	54	38	34	V_{REFH}		
67	55	39	35	V_{REFL}		
68	56	40	36	BKGD	MS	
69	57	41	37	PTG5	XTAL	
70	58	42	38	PTG6	EXTAL	
71	59	43	39	V_{SS}		
72	—	—	—	V_{DD}(NC)		
73	60	44	40	PTC0	SCL1	
74	61	45	41	PTC1	SDA1	
75	—	—	—	PTH4	SPSCK2	
76	—	—	—	PTH5	MOSI2	
77	—	—	—	PTH6	MISO2	
78	62	46	42	PTC2	MCLK	
79	63	47	43	PTC3	TxD2	
80	64	48	44	PTC5	RxD2	

[1] TPMCLK, TPM1CLK, and TPM2CLK options are configured via software; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively.

Chapter 3
Electrical Characteristics and Timing Specifications

3.1 Introduction

This section contains electrical and timing specifications.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3-1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3-2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 3-2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to + 5.8	V
Input voltage	V_{In}	− 0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1], [2], [3]	I_D	± 25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	−55 to +150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 3-3. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H –40 to 125	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s		61	
	2s2p		47	
64-pin QFP				
	1s		57	
	2s2p	θ_{JA}	43	°C/W
48-pin QFN				
	1s		81	
	2s2p		28	
44-pin LQFP				
	1s		73	
	2s2p		56	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s - Single Layer Board, one signal layer

4 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 3-1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 3-2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits and JEDEC Standard for Non-Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3-4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		– 2.5	V
	Maximum input voltage limit		7.5	V

Table 3-5. ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	± 2000	–	V
2	C	Machine Model (MM)	V_{MM}	± 200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	± 500	–	V
4	C	Latch-up Current at T_A = 125°C	I_{LAT}	± 100	–	mA

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 3-6. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	—	Operating Voltage	V_{DD}	2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA 5 V, I_{Load} = –0.4 mA 3 V, I_{Load} = –0.24 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
	P	Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA 5 V, I_{Load} = 0.4 mA 3 V, I_{Load} = 0.24 mA	V_{OL}	 — — — —	 — — — —	 1.5 1.5 0.8 0.8	V
	P	Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.4 mA		 — — — —	 — — — —	 1.5 1.5 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5V 3V	I_{OLT}	 — —	 — —	 100 60	mA
6	P	Input high voltage; all digital inputs — 2.7v ≤ V_{DD} 4.5v	V_{IH}	0.70xV_{DD}	—	—	V
		Input high voltage; all digital inputs — 4.5v ≤ V_{DD} ≤ 5.5v	V_{IH}	0.65xV_{DD}	—	—	
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 x V_{DD}	
8	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}			mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V
15	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
16	D	POR rearm time	t_{POR}	10	—	—	μs
17	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVDH}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
18	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVDL}	 2.48 2.54	 2.56 2.62	 2.64 2.7	V

Table 3-6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
19	P	Low-voltage warning threshold — high range V_{DD} falling V_{DD} rising	V_{LVWH}	4.2 4.3	4.3 4.4	4.4 4.5	V
20	P	Low-voltage warning threshold — low range V_{DD} falling V_{DD} rising	V_{LVWL}	2.48 2.54	2.56 2.62	2.64 2.7	V
21	P	Low-voltage inhibit reset/recover hysteresis 5V 3V	V_{hys}	— —	100 60	— —	mV
22	P	Bandgap Voltage Reference[5]	V_{BG}	1.170	1.200	1.230	V

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Factory trimmed at V_{DD} = 3.0 V, Temperature = 25 °C.

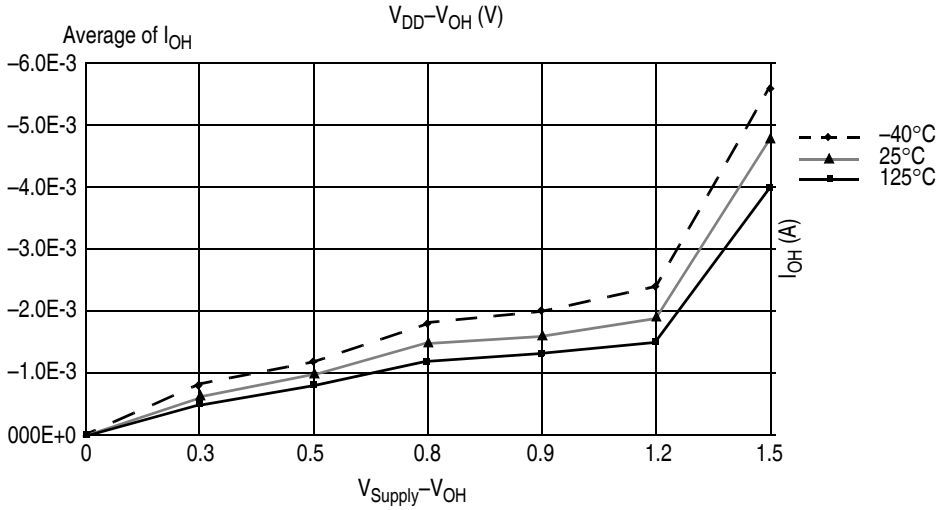


Figure 3-1. Typical I_{OH} (Low Drive) vs V_{DD}–V_{OH} at V_{DD} = 3 V

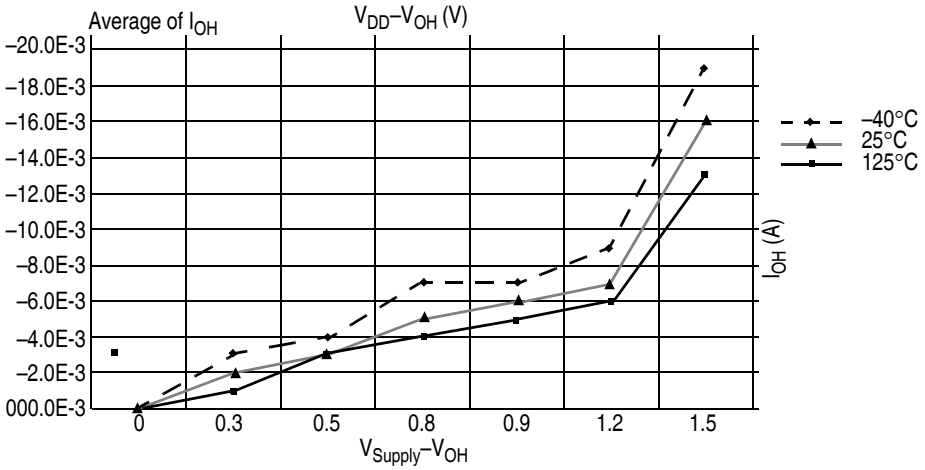


Figure 3-2. Typical I_{OH} (High Drive) vs $V_{DD}–V_{OH}$ at V_{DD} = 3 V

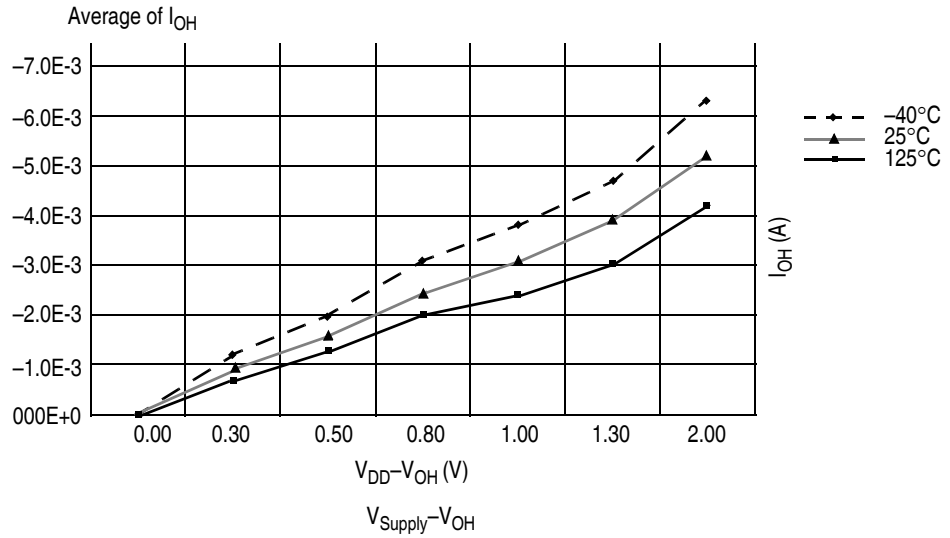


Figure 3-3. Typical I_{OH} (Low Drive) vs $V_{DD}–V_{OH}$ at V_{DD} = 5 V

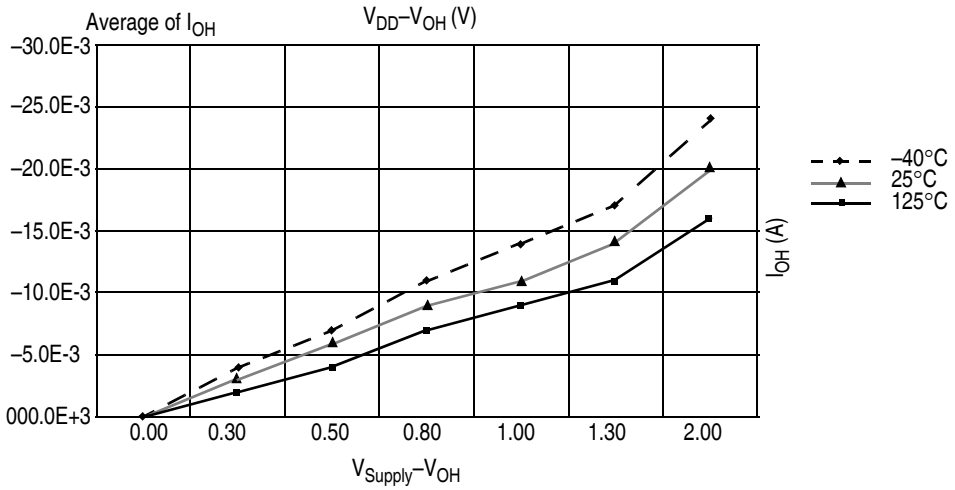


Figure 3-4. Typical I_{OH} (High Drive) vs $V_{DD}–V_{OH}$ at V_{DD} = 5 V

3.7 Supply Current Characteristics

Table 3-7. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current[2] measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	RI_{DD}	5	1.1	1.4[3]	mA	–40 to 125°C
				3	1.0	1.2		
2	C	Run supply current[4] measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)	RI_{DD}	5	6.7	8.0[5]	mA	–40 to 125°C
				3	6	7.5		
3	C	Stop2 mode supply current	$S2I_{DD}$	5	1.0	25 160	µA	–40 to 85°C –40 to 125°C
				3	0.8	23 150	µA	–40 to 85°C –40 to 125°C
4	C	Stop3 mode supply current	$S3I_{DD}$	5	1.2	27 180[3]	µA	–40 to 85°C –40 to 125°C
				3	1.0	25 170	µA	–40 to 85°C –40 to 125°C
5	C	RTI adder to stop2 or stop3[6]	$S23I_{DDRTI}$	5	300	500 500	nA	–40 to 85°C –40 to 125°C
				3	300	500 500	nA	–40 to 85°C –40 to 125°C
6	C	LVD adder to stop3 (LVDE = LVDSE = 1)	$S3I_{DDLVD}$	5	110	180 180	µA	–40 to 85°C –40 to 125°C
				3	90	160 160	µA	–40 to 85°C –40 to 125°C
7	C	Adder to stop3 for oscillator enabled[7] (OSCSTEN =1)	$S3I_{DDOSC}$	5,3	5	8 8	µA µA	–40 to 85°C –40 to 125°C

1 Typical values are based on characterization data at 25°C unless otherwise stated. See Figure 3-5 through Figure 3-7 for typical curves across voltage/temperature.

2 All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

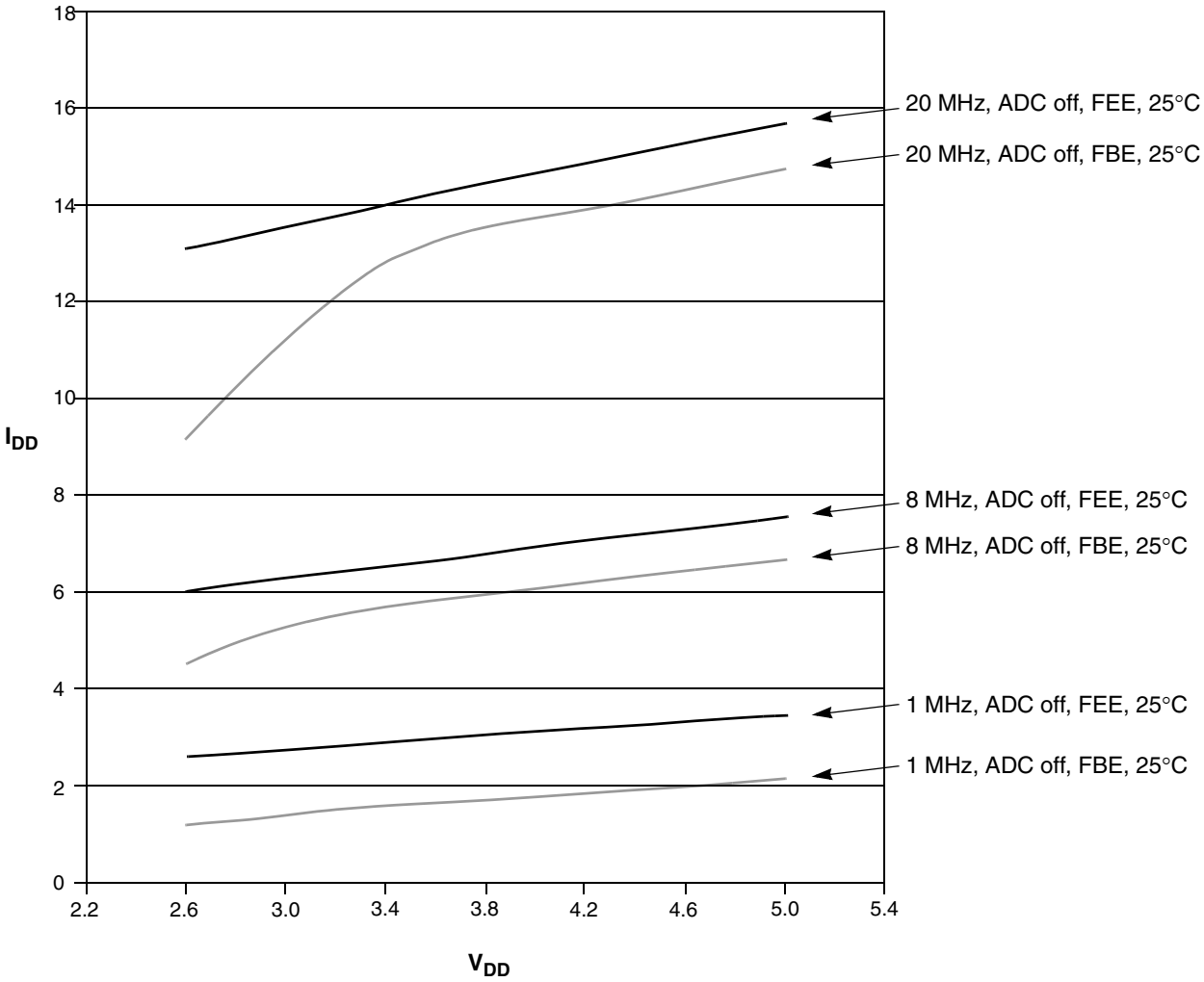
3 Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

4 All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

5 Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

6 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 560 µA at 3 V with f_{Bus} = 1 MHz.

7 Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal, low power mode (HGO = 0), clock monitor disabled (LOCD = 1).



Note: External clock is square wave supplied by function generator. For FEE mode, external reference frequency is 4 MHz

Figure 3-5. Typical Run I_{DD} for FBE and FEE Modes, I_{DD} vs. V_{DD}

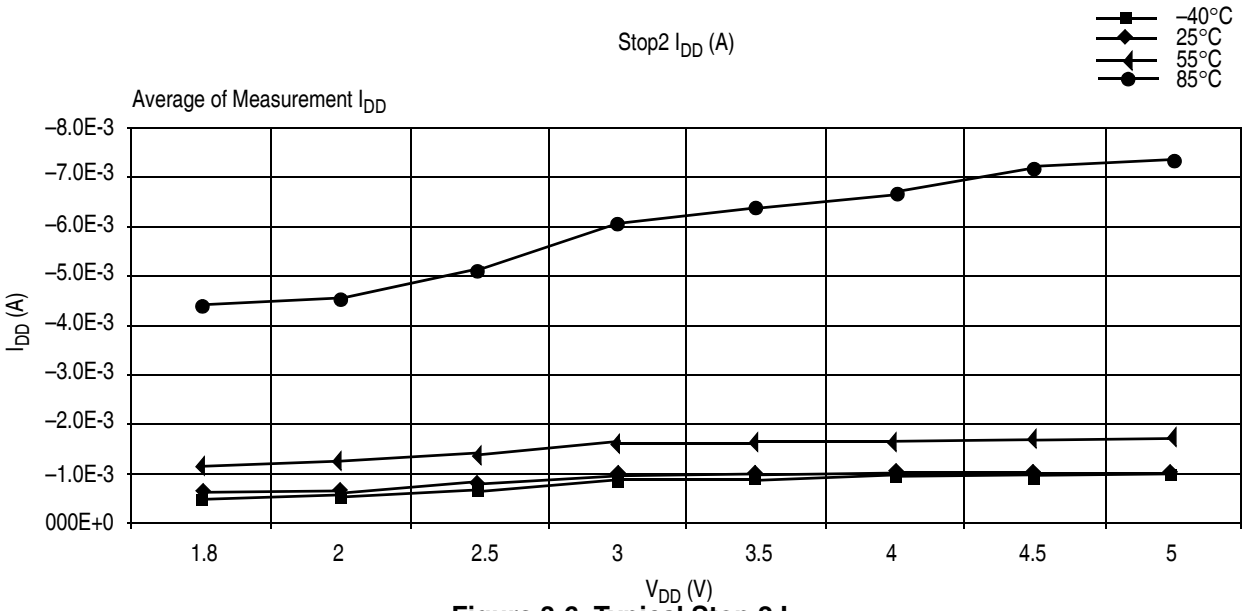


Figure 3-6. Typical Stop 2 I_{DD}

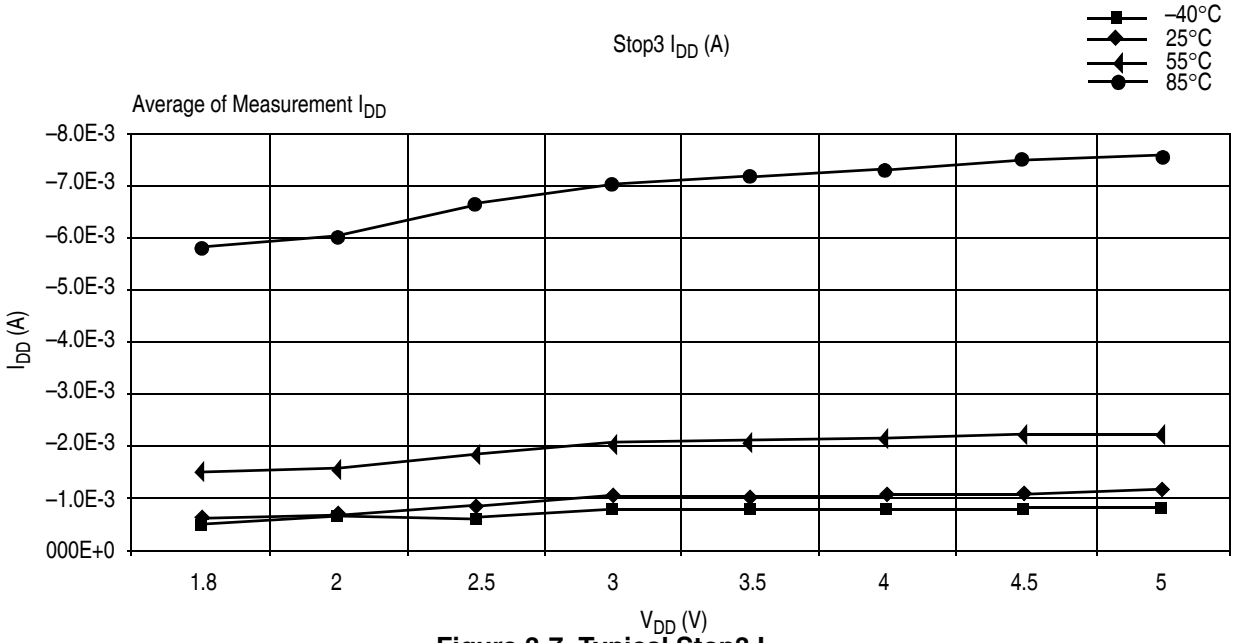


Figure 3-7. Typical Stop3 I_{DD}

3.8 ADC Characteristics

Table 3-8. 5 Volt 10-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V
	Delta to V_{DD} (V_{DD}–V_{DDAD})[2]	ΔV_{DDAD}	–100	0	+100	mV
Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSAD})[2]	ΔV_{SSAD}	–100	0	+100	mV
Ref voltage high		V_{REFH}	2.7	V_{DDAD}	V_{DDAD}	V
Ref voltage low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V
Supply current	Stop, reset, module off	I_{DDAD}	—	0.011	1	μA
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input capacitance		C_{ADIN}	—	4.5	5.5	pF
Input resistance		R_{ADIN}	—	3	5	kΩ
Analog source resistance External to MCU	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ
	8-bit mode (all valid f_{ADCK})		—	—	10	
ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz
	Low power (ADLPC = 1)		0.4	—	4.0	
Temp Sensor Slope	–40°C to 25°C	m	—	3.266	—	mV/°C
	25°C to 125°C			3.638	—	
Temp Sensor Voltage	25°C	V_{TEMP25}	—	1.396	—	V

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 dc potential difference.

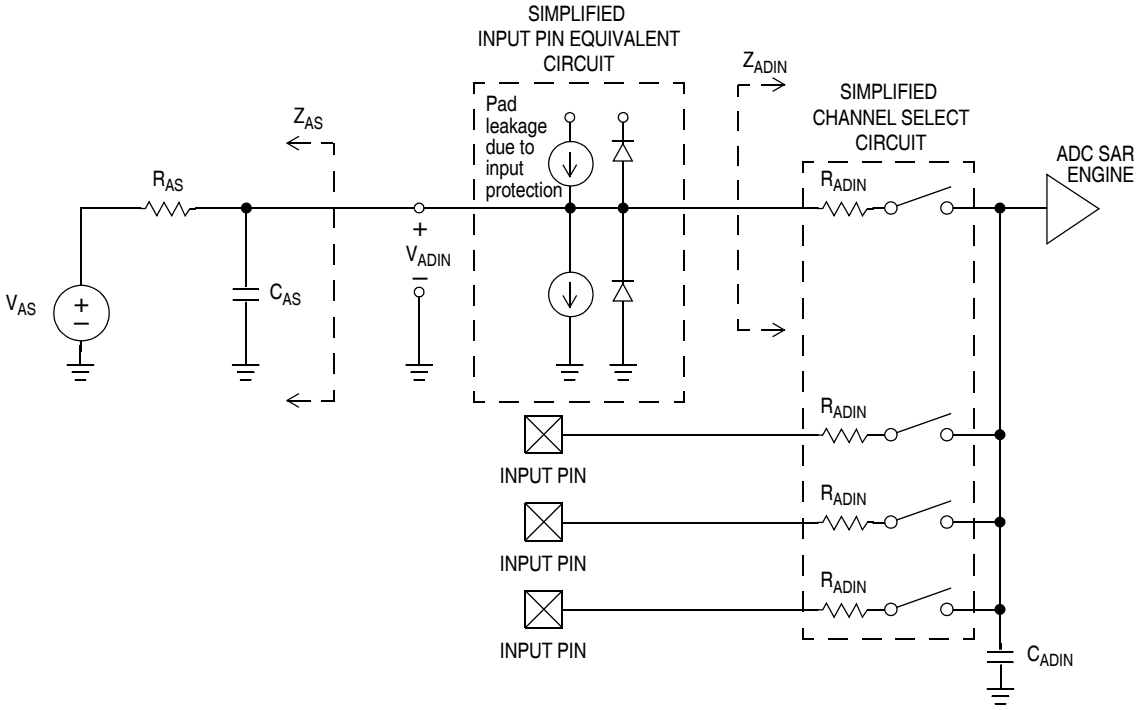


Figure 3-8. ADC Input Impedance Equivalency Diagram

Table 3-9. 5 Volt 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDAD}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDAD}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	—	μA
	$V_{DDAD} \leq 5.5$ V	P		—	—	1	mA
ADC asynchronous clock source $t_{ADACK} = 1/f_{ADACK}$	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (Including sample time)	Short sample (ADLSMP = 0)	P	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	P	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted error Includes quantization	10-bit mode	P	E_{TUE}	—	±1	±2.5	LSB[2]
	8-bit mode			—	±0.5	±1.0	
Differential non-linearity	10-bit mode	P	DNL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
	Monotonicity and no-missing-codes guaranteed						
Integral non-linearity	10-bit mode	C	INL	—	±0.5	±1.0	LSB[2]
	8-bit mode			—	±0.3	±0.5	
Zero-scale error $V_{ADIN} = V_{SSA}$	10-bit mode	P	E_{ZS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Full-scale error $V_{ADIN} = V_{DDA}$	10-bit mode	P	E_{FS}	—	±0.5	±1.5	LSB[2]
	8-bit mode			—	±0.5	±0.5	
Quantization error	10-bit mode	D	E_Q	—	—	±0.5	LSB[2]
	8-bit mode			—	—	±0.5	