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Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC9S08AC16
MC9S08AC8
MC9S08AW16A
MC9S08AW8A

Data Sheet

HCS08
Microcontrollers

MC9S08AC16
Rev. 9
8/2011

freescale.com

MC9S08AC16 Series Features

MC9S08AC16 Series Devices

- Consumer & Industrial
  - MC9S08AC16
  - MC9S08AC8
- Automotive
  - MC9S08AW16A
  - MC9S08AW8A

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 20-MHz internal bus frequency
- HC08 instruction set with added BGND instruction
- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources

Memory Options

- Up to 16 KB of on-chip in-circuit programmable FLASH memory with block protection and security options
- Up to 1 KB of on-chip RAM

Clock Source Options

- Clock source options include crystal, resonator, external clock, or internally generated clock with precision NVM trimming

System Protection

- Optional computer operating properly (COP) reset with option to run from independent internal clock source or bus clock
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Illegal address detection with reset

Power-Saving Modes

- Wait plus two stops

Peripherals

- **ADC** — 8-channel, 10-bit analog-to-digital converter with automatic compare function
- **SCI** — Two serial communications interface modules with optional 13-bit break
- **SPI** — Serial peripheral interface module
- **IIC** — Inter-integrated circuit bus module to operate at up to 100 kbps with maximum bus loading; capable of higher baud rates with reduced loading
- **Timers** — Three 16-bit timer/pulse-width modulator (TPM) modules — Two 2-channel and one 4-channel; each has selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels
- **KBI** — 7-pin keyboard interrupt module

Input/Output

- Up to 38 general-purpose input/output (I/O) pins
- Software selectable pullups on ports when used as inputs
- Software selectable slew rate control on ports when used as outputs
- Software selectable drive strength on ports when used as outputs
- Master reset pin and power-on reset (POR)
- Internal pullup on $\overline{\text{RESET}}$, IRQ, and BKGD/MS pins to reduce customer system cost

Package Options

- 48-pin quad flat no-lead package (QFN)
- 44-pin low-profile quad flat package (LQFP)
- 42-pin shrink dual-in-line package (SDIP)
- 32-pin low-profile quad flat package (LQFP)

MC9S08AC16 Series Data Sheet

Covers MC9S08AC16

MC9S08AC8

MC9S08AW16A

MC9S08AW8A

MC9S08AC16
Rev. 9
8/2011

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision Number	Revision Date	Description of Changes
0	12/2007	Initial Release.
1	12/2007	Updated the package designators for the 32 LQFP and 44 LQFP to be LC and LD respectively.
2	2/2008	Corrected the SPI block module to be V3.
3	3/2008	AC market launch.Verified that the ADC Temp Sensor values were correct.
4	5/2008	Incorporated general release edits and updates, revised the Stop2 and Stop3 max values, added the RoHS logo, and updated the back cover addresses.
5	6/2008	Corrected the note in the TPM introduction.
6	7/2008	Changed all instances of S9S08AWxxA to MC9S08AWxxA except in Appendix B. Added 42SDIP package option.
7	5/2009	Corrected SPI registers in Table 4-2. Added V_{BG} in Table A-6. Corrected title of Table 6-3, Figure 6-13, Figure 6-14, Table 6-5 and Figure 6-19. Added errata for the following sections: • Throughout (remove stop1 instances) • Table 4-1 • Table 4-2 • Section 9.2, “Keyboard Pin Sharing” • Section 9.3, “Features • Table A-6 • Table A-7 • Figure A-12
8	11/20/2009	Updated the whole document for MC9S08AW16A/MC9S08AW8A to support the third TPM module. Updated the TPM 1 channel to 4 for the 32-pin packages in the Table 1-1. Updated the bit 2 of IRQSC register in the Table 4-2. Updated the Temp Sensor Voltage in the Table A-9.
9	8/12/2011	Corrected the address of SPI1D to 0x0055 in the Table 4-2. Updated the RI_{DD} in the Table A-7. Updated the t_{RTI} in the Table A-12 for MC9S08ACxx.

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Chapter 1
Introduction

1.1 Overview

The MC9S08AC16 Series devices are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types. Refer to Table 1-1 for memory sizes and package types.

NOTE

- The **MC9S08AC16** and **MC9S08AC8** devices are qualified for, and are intended to be used in, *consumer and industrial* applications.
- The **MC9S08AW16A** and **MC9S08AW8A** devices are qualified for, and are intended to be used in, *automotive* applications.

Table 1-1 summarizes the feature set available in the MCUs.

Table 1-1. Features by MCU and Package

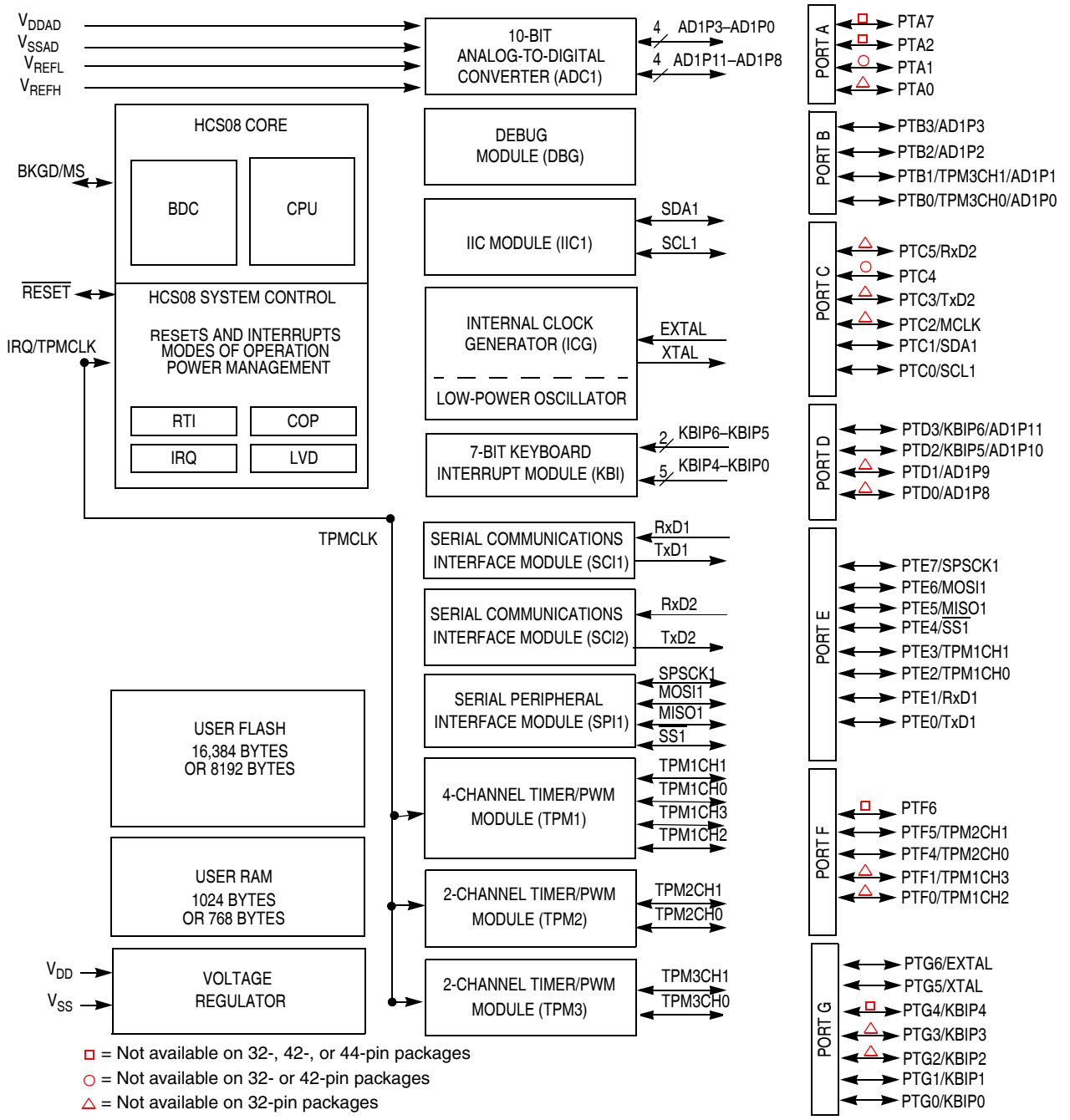
Consumer and Industrial "AC" Devices								
Feature	**MC9S08AC16**				**MC9S08AC8**			
FLASH size (bytes)	16K				8K			
RAM size (bytes)	1024				768			
Pin quantity	**48**	**44**	**42**	**32**	**48**	**44**	**42**	**32**
ADC channels	8	8	8	6	8	8	8	6
TPM1 channels[1]	4	4	4	4	4	4	4	4
TPM2 channels	2	2	2	2	2	2	2	2
TPM3 channels	2	2	2	2	2	2	2	2
KBI pins	7	6	6	4	7	6	6	4
GPIO pins	38	34	32	22	38	34	32	22
Consumer & Industrial Qualified	yes				yes			
Automotive Qualified	no				no			

Automotive "AW" Devices						
Feature	**MC9S08AW16A**			**MC9S08AW8A**		
FLASH size (bytes)	16K			8K		
RAM size (bytes)	1024			768		
Pin quantity	**48**	**44**	**32**	**48**	**44**	**32**
ADC channels	8	8	6	8	8	6
TPM1 channels[1]	4	4	4	4	4	4
TPM2 channels	2	2	2	2	2	2
TPM3 channels	2	2	2	2	2	2
KBI pins	7	6	4	7	6	4
GPIO pins	38	34	22	38	34	22
Consumer & Industrial Qualified	no			no		
Automotive Qualified	yes			yes		

[1] There are 4 channels on TPM1 but two of them (TPM1CH2 and TPM1CH3) are not bonded to 32-pin LQFP package. These two channels can be used for soft timer function.

1.2 MCU Block Diagrams

The block diagram shows the structure of the MC9S08AC16 Series MCU.



Notes:

1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ is enabled (IRQPE = 1). Pulldown is enabled if rising edge detect is selected (IRQEDG = 1)
3. IRQ does not have a clamp diode to V_{DD}. IRQ should not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. PTD3, PTD2, and PTG4 contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).

Figure 1-1. MC9S08AC16 Block Diagram

Table 1-2 lists the functional versions of the on-chip modules.

Table 1-2. Versions of On-Chip Modules

Module		Version
Analog-to-Digital Converter	(ADC)	1
Internal Clock Generator	(ICG)	4
Inter-Integrated Circuit	(IIC)	2
Keyboard Interrupt	(KBI)	1
Serial Communications Interface	(SCI)	4
Serial Peripheral Interface	(SPI)	3
Timer Pulse-Width Modulator	(TPM)	3
Central Processing Unit	(CPU)	2

1.3 System Clock Distribution

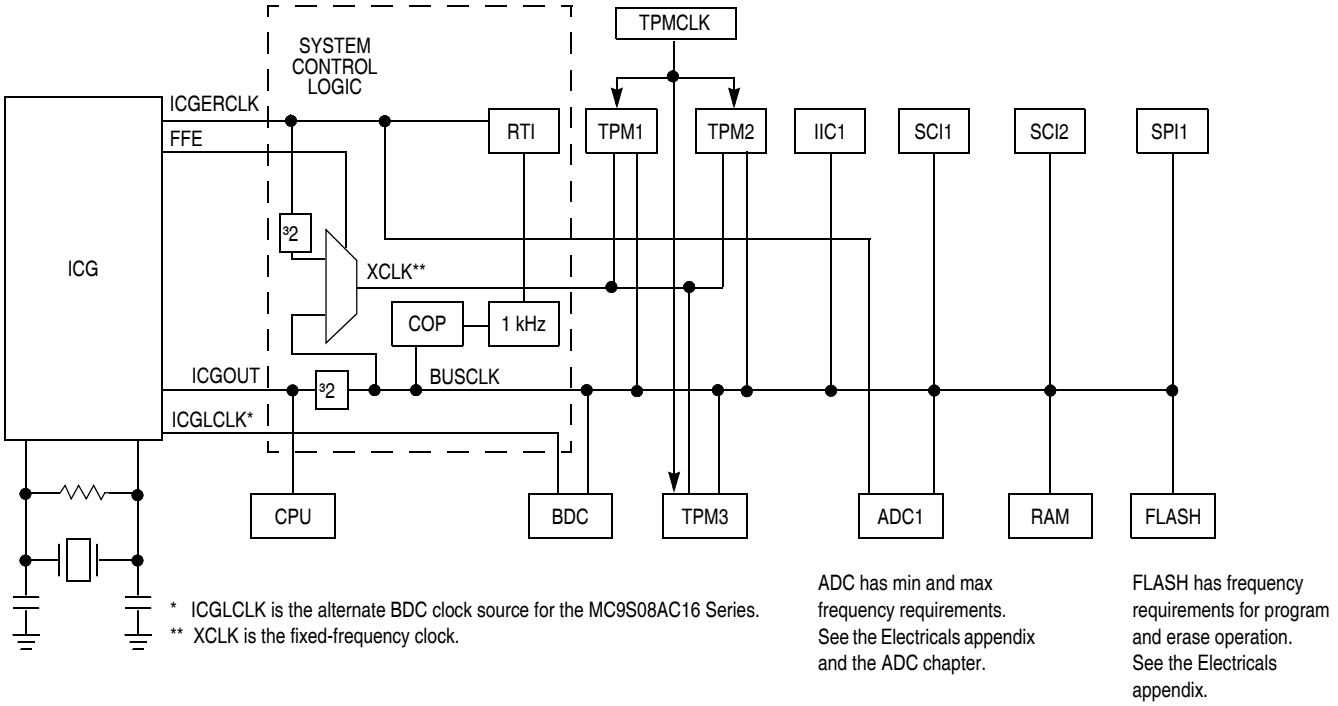


Figure 1-2. System Clock Distribution Diagram

Some of the modules inside the MCU have clock source choices. Figure 1-2 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
  - The external crystal oscillator
  - An external clock source
  - The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module

— Control bits inside the ICG determine which source is connected.

- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT > 4 × the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be ICGERCLK/2. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source. Can also be used as the ALTCLK input to the ADC module.