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Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC9S08AC60
MC9S08AC48
MC9S08AC32

Data Sheet

HCS08
Microcontrollers

MC9S08AC60
Rev. 3
8/2011

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MC9S08AC60 Series Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 20-MHz internal bus frequency
- HC08 instruction set with added BGND instruction

Development Support

- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources

Memory Options

- Up to 60 KB of on-chip FLASH memory with security options
- Up to 2 KB of on-chip RAM

Clock Source Options

- Clock source options include crystal, resonator, external clock, or internally generated clock with precision NVM trimming using ICG module

System Protection

- Optional watchdog computer operating properly (COP) reset with option to run from independent 1kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Cyclic Redundancy Check (CRC) Module to support fast cyclic redundancy checks on memory.

Power-Saving Modes

- Wait plus two stops

Peripherals

- **ADC** — Up to 16-channel, 10-bit analog-to-digital converter with automatic compare function
- **SCI** — Two serial communications interface modules with optional 13-bit break. supports LIN 2.0 Protocol and SAE J2602; Master extended break generation; Slave extended break detection
- **SPI** — Serial peripheral interface module
- **IIC** — Inter-integrated circuit bus module to operate at up to 100 kbps with maximum bus loading; capable of higher baudrates with reduced loading. 10-bit address extension option.
- **Timers** — Up to two 2-channel and one 6-channel 16-bit timer/pulse-width modulator (TPM) module: Selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels
- **KBI** — Up to 8-pin keyboard interrupt module
- **CRC** - Hardware CRC generation using a 16-bit shift register

Input/Output

- Up to 54 general-purpose input/output (I/O) pins
- Software selectable pullups on ports when used as inputs
- Software selectable slew rate control on ports when used as outputs
- Software selectable drive strength on ports when used as outputs
- Master reset pin and power-on reset (POR)
- Internal pullup on $\overline{\text{RESET}}$, IRQ, and BKGD/MS pins to reduce customer system cost

Package Options

- 64-pin quad flat package (QFP)
- 64-pin low-profile quad flat package (LQFP)
- 48-pin quad flat pack no lead package (QFN)
- 44-pin low-profile quad flat package (LQFP)
- 32-pin low-profile quad flat package (LQFP)

MC9S08AC60 Series Data Sheet

Covers MC9S08AC60
MC9S08AC48
MC9S08AC32

MC9S08AC60 Series
Rev. 3
8/2011

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision Number	Revision Date	Description of Changes
1	2/2008	Preliminary customer release.
2	3/2008	Market Launch Release.
3	8/2011	Added V_{BG} and I_{IC} in the Table A-6. Added two figures of Figure 4-2 and Figure 4-3 to replace the old figure of “FLASH Program and Erase Flowchart”. Updated Table 15-8. Updated RI_{DD} in the Table A-7. Updated t_{RTI} in the Table A-12.

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Chapter 1
Introduction

1.1 Overview

The MC9S08AC60 Series are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types. Refer to Table 1-1 for memory sizes and package types.

Table 1-1. Devices in the MC9S08AC60 Series

Device	FLASH	RAM	Package
MC9S08AC60	63,280	2048	64 QFP 64 LQFP 48 QFN 44 LQFP 32 LQFP
MC9S08AC48	49,152		64 QFP 64 LQFP 48 QFN 44 LQFP 32 LQFP
MC9S08AC32	32,768		64 QFP 64 LQFP 48 QFN 44 LQFP 32 LQFP

Table 1-2 summarizes the feature set available in the MC9S08AC60 Series of MCUs.

Table 1-2. MC9S08AC60 Series Peripherals Available per Package Type

	MC9S08AC60/48/32			
Feature	**64-pin**	**48-pin**	**44-pin**	**32-pin**
CRC	yes			
ADC	16-ch	8-ch		6-ch
IIC	yes			
IRQ	yes			
KBI1	8	7	6	4
SCI1	yes			

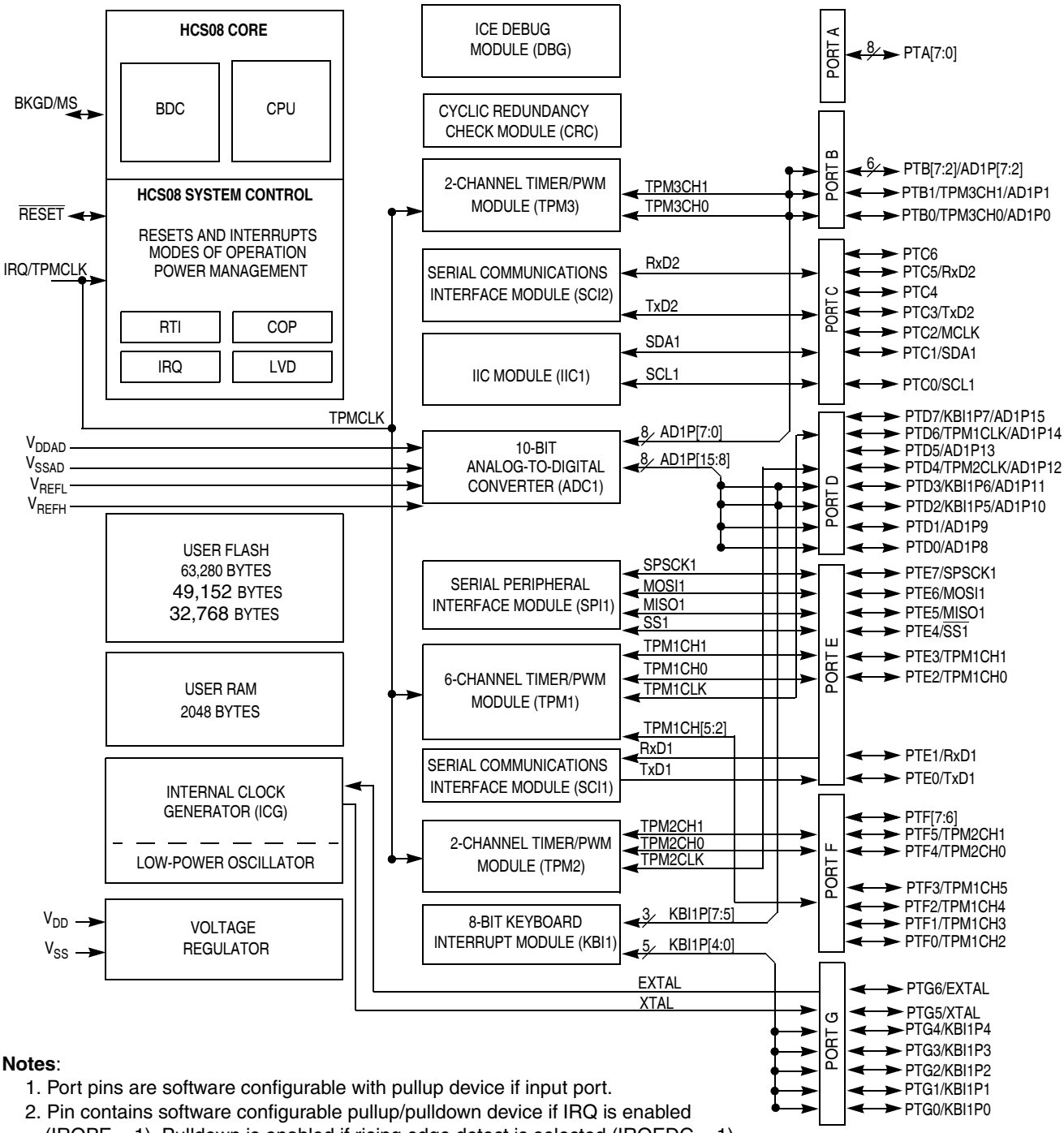
Table 1-2. MC9S08AC60 Series Peripherals Available per Package Type

	MC9S08AC60/48/32			
Feature	**64-pin**	**48-pin**	**44-pin**	**32-pin**
SCI2	yes			no
SPI1	yes			
TPM1	6-ch	4-ch		2-ch
TPM1CLK[1]	yes	no		
TPM2	2-ch			
TPM2CLK[1]	yes	no		
TPM3	2-ch			
TPMCLK [1]	yes			
I/O pins	54	38	34	22

[1] TPMCLK, TPM1CLK, and TPM2CLK options are configured via software using the TPMCCFG bit; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively. Reference the TPM chapter for a functional description of the TPMxCLK signal.

1.2 MCU Block Diagrams

The block diagram shows the structure of the MC9S08AC60 Series MCU.



Notes:

1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ is enabled (IRQPE = 1). Pulldown is enabled if rising edge detect is selected (IRQEDG = 1)
3. Pin contains integrated pullup device.
4. PTD3, PTD2, PTD7, and PTG4 contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).
5. TPMCLK, TPM1CLK, and TPM2CLK options are configured via software; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively.

Figure 1-1. MC9S08AC60 Series Block Diagram

Table 1 lists the functional versions of the on-chip modules.

Table 1. Versions of On-Chip Modules

Module		Version
Cyclic Redundancy Check Generator	(CRC)	1
Analog-to-Digital Converter	(ADC)	1
Internal Clock Generator	(ICG)	4
Inter-Integrated Circuit	(IIC)	2
Keyboard Interrupt	(KBI)	1
Serial Communications Interface	(SCI)	4
Serial Peripheral Interface	(SPI)	3
Timer Pulse-Width Modulator	(TPM)	3
Central Processing Unit	(CPU)	2
Debug Module	(DBG)	2

1.3 System Clock Distribution

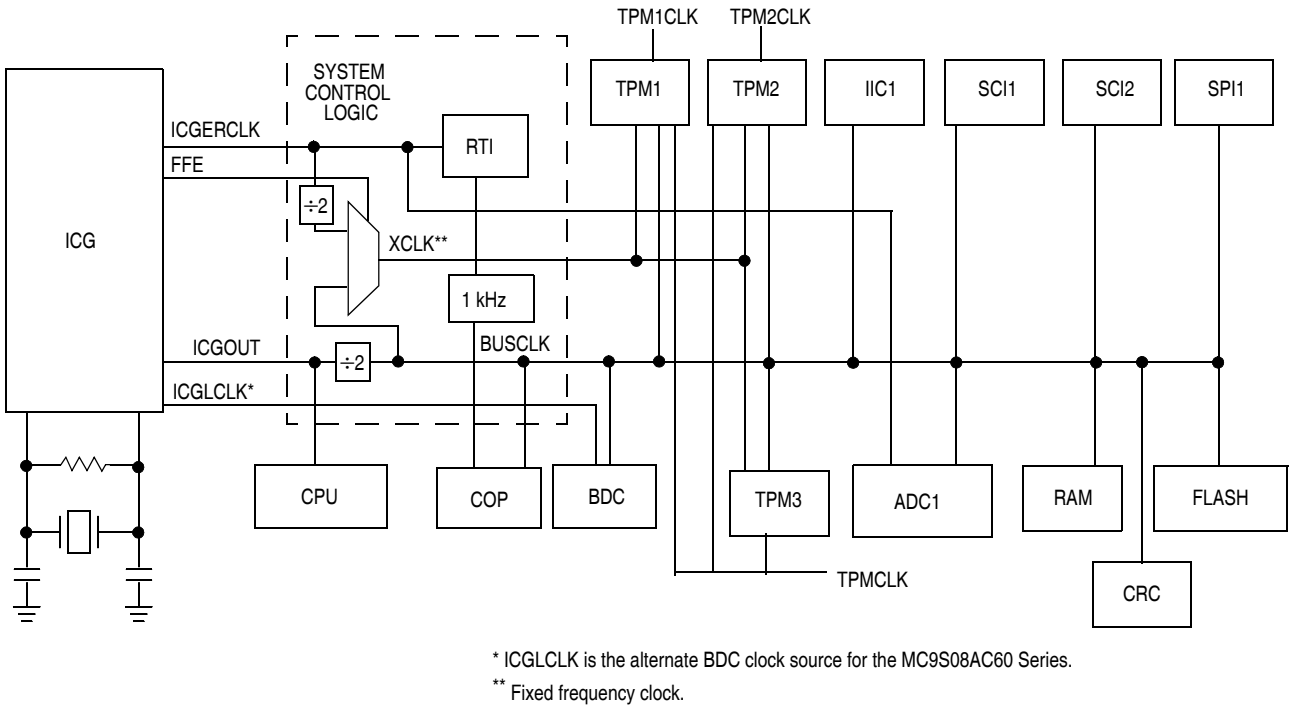


Figure 1-2. System Clock Distribution Diagram

Some of the modules inside the MCU have clock source choices. Figure 1-2 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
  - The external crystal oscillator

  - An external clock source
  - The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module
  - Control bits inside the ICG determine which source is connected.
- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT > 4 × the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be ICGERCLK/2. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source. Can also be used as the ALTCLK input to the ADC module.