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Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC9S08AC60
MC9S08AC48
MC9S08AC32

Data Sheet

HCS08
Microcontrollers

MC9S08AC60
Rev. 3
8/2011

freescale.com

MC9S08AC60 Series Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 20-MHz internal bus frequency
- HC08 instruction set with added BGND instruction

Development Support

- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources

Memory Options

- Up to 60 KB of on-chip FLASH memory with security options
- Up to 2 KB of on-chip RAM

Clock Source Options

- Clock source options include crystal, resonator, external clock, or internally generated clock with precision NVM trimming using ICG module

System Protection

- Optional watchdog computer operating properly (COP) reset with option to run from independent 1kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Cyclic Redundancy Check (CRC) Module to support fast cyclic redundancy checks on memory.

Power-Saving Modes

- Wait plus two stops

Peripherals

- **ADC** — Up to 16-channel, 10-bit analog-to-digital converter with automatic compare function
- **SCI** — Two serial communications interface modules with optional 13-bit break. supports LIN 2.0 Protocol and SAE J2602; Master extended break generation; Slave extended break detection
- **SPI** — Serial peripheral interface module
- **IIC** — Inter-integrated circuit bus module to operate at up to 100 kbps with maximum bus loading; capable of higher baudrates with reduced loading. 10-bit address extension option.
- **Timers** — Up to two 2-channel and one 6-channel 16-bit timer/pulse-width modulator (TPM) module: Selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels
- **KBI** — Up to 8-pin keyboard interrupt module
- **CRC** - Hardware CRC generation using a 16-bit shift register

Input/Output

- Up to 54 general-purpose input/output (I/O) pins
- Software selectable pullups on ports when used as inputs
- Software selectable slew rate control on ports when used as outputs
- Software selectable drive strength on ports when used as outputs
- Master reset pin and power-on reset (POR)
- Internal pullup on $\overline{\text{RESET}}$, IRQ, and BKGD/MS pins to reduce customer system cost

Package Options

- 64-pin quad flat package (QFP)
- 64-pin low-profile quad flat package (LQFP)
- 48-pin quad flat pack no lead package (QFN)
- 44-pin low-profile quad flat package (LQFP)
- 32-pin low-profile quad flat package (LQFP)

MC9S08AC60 Series Data Sheet

Covers MC9S08AC60
MC9S08AC48
MC9S08AC32

MC9S08AC60 Series
Rev. 3
8/2011

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision Number	Revision Date	Description of Changes
1	2/2008	Preliminary customer release.
2	3/2008	Market Launch Release.
3	8/2011	Added V_{BG} and I_{IC} in the Table A-6 . Added two figures of Figure 4-2 and Figure 4-3 to replace the old figure of “FLASH Program and Erase Flowchart”. Updated Table 15-8 . Updated R_{IDD} in the Table A-7 . Updated t_{RTI} in the Table A-12 .

List of Chapters

Chapter	Title	Page
Chapter 1	Introduction.....	19
Chapter 2	Pins and Connections	25
Chapter 3	Modes of Operation	35
Chapter 4	Memory	41
Chapter 5	Resets, Interrupts, and System Configuration	67
Chapter 6	Parallel Input/Output	85
Chapter 7	Central Processor Unit (S08CPUV2)	109
Chapter 8	Cyclic Redundancy Check (S08CRCV1).....	129
Chapter 9	Analog-to-Digital Converter (S08ADC10V1).....	137
Chapter 10	Internal Clock Generator (S08ICGV4)	165
Chapter 11	Inter-Integrated Circuit (S08IICV2)	193
Chapter 12	Keyboard Interrupt (S08KBIV1).....	211
Chapter 13	Serial Communications Interface (S08SCIV4).....	217
Chapter 14	Serial Peripheral Interface (S08SPIV3)	237
Chapter 15	Timer/PWM (S08TPMV3)	253
Chapter 16	Development Support	283
Appendix A	Electrical Characteristics and Timing Specifications	305
Appendix B	Ordering Information and Mechanical Drawings.....	333

Contents

Section Number	Title	Page
Chapter 1		
Introduction		
1.1	Overview	19
1.2	MCU Block Diagrams	20
1.3	System Clock Distribution	22
Chapter 2		
Pins and Connections		
2.1	Introduction	25
2.2	Device Pin Assignment	25
2.3	Recommended System Connections	29
2.3.1	Power (V_{DD} , V_{SS} , V_{DDAD} , V_{SSAD})	31
2.3.2	Oscillator (XTAL, EXTAL)	31
2.3.3	$\overline{\text{RESET}}$ Pin	31
2.3.4	Background/Mode Select (BKGD/MS)	32
2.3.5	ADC Reference Pins (V_{REFH} , V_{REFL})	32
2.3.6	External Interrupt Pin (IRQ)	32
2.3.7	General-Purpose I/O and Peripheral Ports	33
Chapter 3		
Modes of Operation		
3.1	Introduction	35
3.2	Features	35
3.3	Run Mode	35
3.4	Active Background Mode	35
3.5	Wait Mode	36
3.6	Stop Modes	36
3.6.1	Stop2 Mode	37
3.6.2	Stop3 Mode	38
3.6.3	Active BDM Enabled in Stop Mode	38
3.6.4	LVD Enabled in Stop Mode	39
3.6.5	On-Chip Peripheral Modules in Stop Modes	39
Chapter 4		
Memory		
4.1	MC9S08AC60 Series Memory Map	41
4.1.1	Reset and Interrupt Vector Assignments	43

Section Number	Title	Page
4.2	Register Addresses and Bit Assignments	44
4.3	RAM	50
4.4	FLASH	51
4.4.1	Features	51
4.4.2	Program and Erase Times	51
4.4.3	Program and Erase Command Execution	52
4.4.4	Burst Program Execution	54
4.4.5	Access Errors	57
4.4.6	FLASH Block Protection	57
4.4.7	Vector Redirection	58
4.5	Security	58
4.6	FLASH Registers and Control Bits	59
4.6.1	FLASH Clock Divider Register (FCDIV)	59
4.6.2	FLASH Options Register (FOPT and NVOPT)	61
4.6.3	FLASH Configuration Register (FCNFG)	61
4.6.4	FLASH Protection Register (FPROT and NVPROT)	63
4.6.5	FLASH Status Register (FSTAT)	63
4.6.6	FLASH Command Register (FCMD)	64

Chapter 5 Resets, Interrupts, and System Configuration

5.1	Introduction	67
5.2	Features	67
5.3	MCU Reset	67
5.4	Computer Operating Properly (COP) Watchdog	68
5.5	Interrupts	69
5.5.1	Interrupt Stack Frame	70
5.5.2	External Interrupt Request (IRQ) Pin	70
5.5.3	Interrupt Vectors, Sources, and Local Masks	71
5.6	Low-Voltage Detect (LVD) System	73
5.6.1	Power-On Reset Operation	73
5.6.2	LVD Reset Operation	73
5.6.3	LVD Interrupt Operation	73
5.6.4	Low-Voltage Warning (LVW)	73
5.7	Real-Time Interrupt (RTI)	73
5.8	MCLK Output	74
5.9	Reset, Interrupt, and System Control Registers and Control Bits	74
5.9.1	Interrupt Pin Request Status and Control Register (IRQSC)	75
5.9.2	System Reset Status Register (SRS)	76
5.9.3	System Background Debug Force Reset Register (SBDFFR)	77
5.9.4	System Options Register (SOPT)	77
5.9.5	System MCLK Control Register (SMCLK)	78

Section Number	Title	Page
5.9.6	System Device Identification Register (SDIDH, SDIDL)	79
5.9.7	System Real-Time Interrupt Status and Control Register (SRTISC)	80
5.9.8	System Power Management Status and Control 1 Register (SPMSC1)	81
5.9.9	System Power Management Status and Control 2 Register (SPMSC2)	82
5.9.10	System Options Register 2 (SOPT2)	83

Chapter 6 Parallel Input/Output

6.1	Introduction	85
6.2	Pin Descriptions	85
6.3	Parallel I/O Control	85
6.4	Pin Control	86
6.4.1	Internal Pullup Enable	87
6.4.2	Output Slew Rate Control Enable	87
6.4.3	Output Drive Strength Select	87
6.5	Pin Behavior in Stop Modes	88
6.6	Parallel I/O and Pin Control Registers	88
6.6.1	Port A I/O Registers (PTAD and PTADD)	88
6.6.2	Port A Pin Control Registers (PTAPE, PTASE, PTADS)	89
6.6.3	Port B I/O Registers (PTBD and PTBDD)	91
6.6.4	Port B Pin Control Registers (PTBPE, PTBSE, PTBDS)	92
6.6.5	Port C I/O Registers (PCD and PCDD)	94
6.6.6	Port C Pin Control Registers (PCPE, PCSE, PCDS)	95
6.6.7	Port D I/O Registers (PTDD and PTDDD)	97
6.6.8	Port D Pin Control Registers (PTDPE, PTDSE, PTDDS)	98
6.6.9	Port E I/O Registers (PTED and PTEDD)	100
6.6.10	Port E Pin Control Registers (PTEPE, PTESE, PTEDS)	101
6.6.11	Port F I/O Registers (PTFD and PTFDD)	103
6.6.12	Port F Pin Control Registers (PTFPE, PTFSE, PTFDS)	104
6.6.13	Port G I/O Registers (PTGD and PTGDD)	106
6.6.14	Port G Pin Control Registers (PTGPE, PTGSE, PTGDS)	107

Chapter 7 Central Processor Unit (S08CPUV2)

7.1	Introduction	109
7.1.1	Features	109
7.2	Programmer's Model and CPU Registers	110
7.2.1	Accumulator (A)	110
7.2.2	Index Register (H:X)	110
7.2.3	Stack Pointer (SP)	111
7.2.4	Program Counter (PC)	111
7.2.5	Condition Code Register (CCR)	111

Section Number	Title	Page
7.3	Addressing Modes	112
7.3.1	Inherent Addressing Mode (INH)	113
7.3.2	Relative Addressing Mode (REL)	113
7.3.3	Immediate Addressing Mode (IMM)	113
7.3.4	Direct Addressing Mode (DIR)	113
7.3.5	Extended Addressing Mode (EXT)	113
7.3.6	Indexed Addressing Mode	113
7.4	Special Operations	114
7.4.1	Reset Sequence	115
7.4.2	Interrupt Sequence	115
7.4.3	Wait Mode Operation	116
7.4.4	Stop Mode Operation	116
7.4.5	BGND Instruction	116
7.5	HCS08 Instruction Set Summary	117

Chapter 8 Cyclic Redundancy Check (S08CRCV1)

8.1	Introduction	129
8.1.1	Features	129
8.1.2	Modes of Operation	131
8.1.3	Block Diagram	131
8.2	External Signal Description	131
8.3	Register Definition	132
8.3.1	Memory Map	132
8.3.2	Register Descriptions	132
8.4	Functional Description	133
8.4.1	ITU-T (CCITT) recommendations & expected CRC results	134
8.5	Initialization Information	134

Chapter 9 Analog-to-Digital Converter (S08ADC10V1)

9.1	Overview	137
9.2	Channel Assignments	137
9.2.1	Alternate Clock	138
9.2.2	Hardware Trigger	138
9.2.3	Temperature Sensor	139
9.2.4	Features	141
9.2.5	Block Diagram	141
9.3	External Signal Description	142
9.3.1	Analog Power (V_{DDAD})	143
9.3.2	Analog Ground (V_{SSAD})	143
9.3.3	Voltage Reference High (V_{REFH})	143

Section Number	Title	Page
9.3.4	Voltage Reference Low (V_{REFL})	143
9.3.5	Analog Channel Inputs (AD _x)	143
9.4	Register Definition	143
9.4.1	Status and Control Register 1 (ADCSC1)	143
9.4.2	Status and Control Register 2 (ADCSC2)	145
9.4.3	Data Result High Register (ADCRH)	146
9.4.4	Data Result Low Register (ADCRL)	146
9.4.5	Compare Value High Register (ADCCVH)	147
9.4.6	Compare Value Low Register (ADCCVL)	147
9.4.7	Configuration Register (ADCCFG)	147
9.4.8	Pin Control 1 Register (APCTL1)	149
9.4.9	Pin Control 2 Register (APCTL2)	150
9.4.10	Pin Control 3 Register (APCTL3)	151
9.5	Functional Description	152
9.5.1	Clock Select and Divide Control	152
9.5.2	Input Select and Pin Control	153
9.5.3	Hardware Trigger	153
9.5.4	Conversion Control	153
9.5.5	Automatic Compare Function	156
9.5.6	MCU Wait Mode Operation	156
9.5.7	MCU Stop3 Mode Operation	156
9.5.8	MCU Stop1 and Stop2 Mode Operation	157
9.6	Initialization Information	157
9.6.1	ADC Module Initialization Example	157
9.7	Application Information	159
9.7.1	External Pins and Routing	159
9.7.2	Sources of Error	161

Chapter 10 Internal Clock Generator (S08ICGV4)

10.1	Introduction	165
10.1.1	Features	168
10.1.2	Modes of Operation	168
10.1.3	Block Diagram	169
10.2	External Signal Description	170
10.2.1	EXTAL — External Reference Clock / Oscillator Input	170
10.2.2	XTAL — Oscillator Output	170
10.2.3	External Clock Connections	170
10.2.4	External Crystal/Resonator Connections	170
10.3	Register Definition	171
10.3.1	ICG Control Register 1 (ICGC1)	171
10.3.2	ICG Control Register 2 (ICGC2)	173

Section Number	Title	Page
10.3.3	ICG Status Register 1 (ICGS1)	174
10.3.4	ICG Status Register 2 (ICGS2)	175
10.3.5	ICG Filter Registers (ICGFLTU, ICGFLTL)	175
10.3.6	ICG Trim Register (ICGTRM)	176
10.4	Functional Description	176
10.4.1	Off Mode (Off)	177
10.4.2	Self-Clocked Mode (SCM)	177
10.4.3	FLL Engaged, Internal Clock (FEI) Mode	178
10.4.4	FLL Engaged Internal Unlocked	179
10.4.5	FLL Engaged Internal Locked	179
10.4.6	FLL Bypassed, External Clock (FBE) Mode	179
10.4.7	FLL Engaged, External Clock (FEE) Mode	179
10.4.8	FLL Lock and Loss-of-Lock Detection	180
10.4.9	FLL Loss-of-Clock Detection	181
10.4.10	Clock Mode Requirements	182
10.4.11	Fixed Frequency Clock	183
10.4.12	High Gain Oscillator	183
10.5	Initialization/Application Information	183
10.5.1	Introduction	183
10.5.2	Example #1: External Crystal = 32 kHz, Bus Frequency = 4.19 MHz	185
10.5.3	Example #2: External Crystal = 4 MHz, Bus Frequency = 20 MHz	187
10.5.4	Example #3: No External Crystal Connection, 5.4 MHz Bus Frequency	189
10.5.5	Example #4: Internal Clock Generator Trim	191

Chapter 11 Inter-Integrated Circuit (S08IICV2)

11.1	Introduction	193
11.1.1	Features	195
11.1.2	Modes of Operation	195
11.1.3	Block Diagram	195
11.2	External Signal Description	196
11.2.1	SCL — Serial Clock Line	196
11.2.2	SDA — Serial Data Line	196
11.3	Register Definition	196
11.3.1	IIC Address Register (IICA)	197
11.3.2	IIC Frequency Divider Register (IICF)	197
11.3.3	IIC Control Register (IICC1)	200
11.3.4	IIC Status Register (IICS)	200
11.3.5	IIC Data I/O Register (IICD)	201
11.3.6	IIC Control Register 2 (IICC2)	202
11.4	Functional Description	203
11.4.1	IIC Protocol	203

Section Number	Title	Page
11.4.2	10-bit Address	206
11.4.3	General Call Address	207
11.5	Resets	207
11.6	Interrupts	207
11.6.1	Byte Transfer Interrupt	207
11.6.2	Address Detect Interrupt	208
11.6.3	Arbitration Lost Interrupt	208
11.7	Initialization/Application Information	209

Chapter 12 Keyboard Interrupt (S08KBIV1)

12.1	Introduction	211
12.1.1	Features	211
12.1.2	KBI Block Diagram	213
12.2	Register Definition	213
12.2.1	KBI Status and Control Register (KBISC)	214
12.2.2	KBI Pin Enable Register (KBIPE)	215
12.3	Functional Description	215
12.3.1	Pin Enables	215
12.3.2	Edge and Level Sensitivity	215
12.3.3	KBI Interrupt Controls	216

Chapter 13 Serial Communications Interface (S08SCIV4)

13.1	Introduction	217
13.1.1	Features	219
13.1.2	Modes of Operation	219
13.1.3	Block Diagram	220
13.2	Register Definition	222
13.2.1	SCI Baud Rate Registers (SCIxBDH, SCIxBDL)	222
13.2.2	SCI Control Register 1 (SCIxC1)	223
13.2.3	SCI Control Register 2 (SCIxC2)	224
13.2.4	SCI Status Register 1 (SCIxS1)	225
13.2.5	SCI Status Register 2 (SCIxS2)	227
13.2.6	SCI Control Register 3 (SCIxC3)	228
13.2.7	SCI Data Register (SCIxD)	229
13.3	Functional Description	229
13.3.1	Baud Rate Generation	229
13.3.2	Transmitter Functional Description	230
13.3.3	Receiver Functional Description	231
13.3.4	Interrupts and Status Flags	233
13.3.5	Additional SCI Functions	234

Section Number	Title	Page
Chapter 14		
Serial Peripheral Interface (S08SPIV3)		
14.1	Introduction	237
14.1.1	Features	239
14.1.2	Block Diagrams	239
14.1.3	SPI Baud Rate Generation	241
14.2	External Signal Description	242
14.2.1	SPSCK — SPI Serial Clock	242
14.2.2	MOSI — Master Data Out, Slave Data In	242
14.2.3	MISO — Master Data In, Slave Data Out	242
14.2.4	SS — Slave Select	242
14.3	Modes of Operation	243
14.3.1	SPI in Stop Modes	243
14.4	Register Definition	243
14.4.1	SPI Control Register 1 (SPIC1)	243
14.4.2	SPI Control Register 2 (SPIC2)	244
14.4.3	SPI Baud Rate Register (SPIBR)	245
14.4.4	SPI Status Register (SPIS)	246
14.4.5	SPI Data Register (SPID)	247
14.5	Functional Description	248
14.5.1	SPI Clock Formats	248
14.5.2	SPI Interrupts	251
14.5.3	Mode Fault Detection	251

Chapter 15
Timer/PWM (S08TPMV3)

15.1	Introduction	253
15.2	Features	253
15.3	TPMV3 Differences from Previous Versions	255
15.3.1	Migrating from TPMV1	257
15.3.2	Features	258
15.3.3	Modes of Operation	258
15.3.4	Block Diagram	259
15.4	Signal Description	261
15.4.1	Detailed Signal Descriptions	261
15.5	Register Definition	265
15.5.1	TPM Status and Control Register (TPMxSC)	265
15.5.2	TPM-Counter Registers (TPMxCNTH:TPMxCNTL)	266
15.5.3	TPM Counter Modulo Registers (TPMxMODH:TPMxMODL)	267
15.5.4	TPM Channel n Status and Control Register (TPMxCnSC)	268
15.5.5	TPM Channel Value Registers (TPMxCnVH:TPMxCnVL)	270
15.6	Functional Description	271

Section Number	Title	Page
15.6.1	Counter	271
15.6.2	Channel Mode Selection	274
15.7	Reset Overview	277
15.7.1	General	277
15.7.2	Description of Reset Operation	277
15.8	Interrupts	277
15.8.1	General	277
15.8.2	Description of Interrupt Operation	278
15.9	The Differences from TPM v2 to TPM v3	279

Chapter 16 Development Support

16.1	Introduction	283
16.1.1	Features	284
16.2	Background Debug Controller (BDC)	284
16.2.1	BKGD Pin Description	285
16.2.2	Communication Details	286
16.2.3	BDC Commands	290
16.2.4	BDC Hardware Breakpoint	292
16.3	On-Chip Debug System (DBG)	293
16.3.1	Comparators A and B	293
16.3.2	Bus Capture Information and FIFO Operation	293
16.3.3	Change-of-Flow Information	294
16.3.4	Tag vs. Force Breakpoints and Triggers	294
16.3.5	Trigger Modes	295
16.3.6	Hardware Breakpoints	297
16.4	Register Definition	297
16.4.1	BDC Registers and Control Bits	297
16.4.2	System Background Debug Force Reset Register (SBDFR)	299
16.4.3	DBG Registers and Control Bits	300

Appendix A Electrical Characteristics and Timing Specifications

A.1	Introduction	305
A.2	Parameter Classification	305
A.3	Absolute Maximum Ratings	306
A.4	Thermal Characteristics	307
A.5	ESD Protection and Latch-Up Immunity	308
A.6	DC Characteristics	310
A.7	Supply Current Characteristics	314
A.8	ADC Characteristics	317
A.9	Internal Clock Generation Module Characteristics	320

Section Number	Title	Page
A.9.1	ICG Frequency Specifications	321
A.10	AC Characteristics	323
A.10.1	Control Timing	323
A.10.2	Timer/PWM (TPM) Module Timing	324
A.11	SPI Characteristics	326
A.12	FLASH Specifications	329
A.13	EMC Performance	330
A.13.1	Conducted Transient Susceptibility	330

Appendix B
Ordering Information and Mechanical Drawings

B.1	Ordering Information	333
B.2	Orderable Part Numbering System	333
B.3	Mechanical Drawings	333

Chapter 1

Introduction

1.1 Overview

The MC9S08AC60 Series are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types. Refer to [Table 1-1](#) for memory sizes and package types.

Table 1-1. Devices in the MC9S08AC60 Series

Device	FLASH	RAM	Package
MC9S08AC60	63,280	2048	64 QFP 64 LQFP 48 QFN 44 LQFP 32 LQFP
MC9S08AC48	49,152		64 QFP 64 LQFP 48 QFN 44 LQFP 32 LQFP
MC9S08AC32	32,768		64 QFP 64 LQFP 48 QFN 44 LQFP 32 LQFP

[Table 1-2](#) summarizes the feature set available in the MC9S08AC60 Series of MCUs.

Table 1-2. MC9S08AC60 Series Peripherals Available per Package Type

Feature	MC9S08AC60/48/32			
	64-pin	48-pin	44-pin	32-pin
CRC	yes			
ADC	16-ch	8-ch		6-ch
IIC	yes			
IRQ	yes			
KBI1	8	7	6	4
SCI1	yes			

Table 1-2. MC9S08AC60 Series Peripherals Available per Package Type

Feature	MC9S08AC60/48/32			
	64-pin	48-pin	44-pin	32-pin
SCI2	yes			no
SPI1	yes			
TPM1	6-ch	4-ch		2-ch
TPM1CLK ¹	yes	no		
TPM2	2-ch			
TPM2CLK ¹	yes	no		
TPM3	2-ch			
TPMCLK ¹	yes			
I/O pins	54	38	34	22

¹ TPMCLK, TPM1CLK, and TPM2CLK options are configured via software using the TPMCCFG bit; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively. Reference the TPM chapter for a functional description of the TPMxCLK signal.

1.2 MCU Block Diagrams

The block diagram shows the structure of the MC9S08AC60 Series MCU.

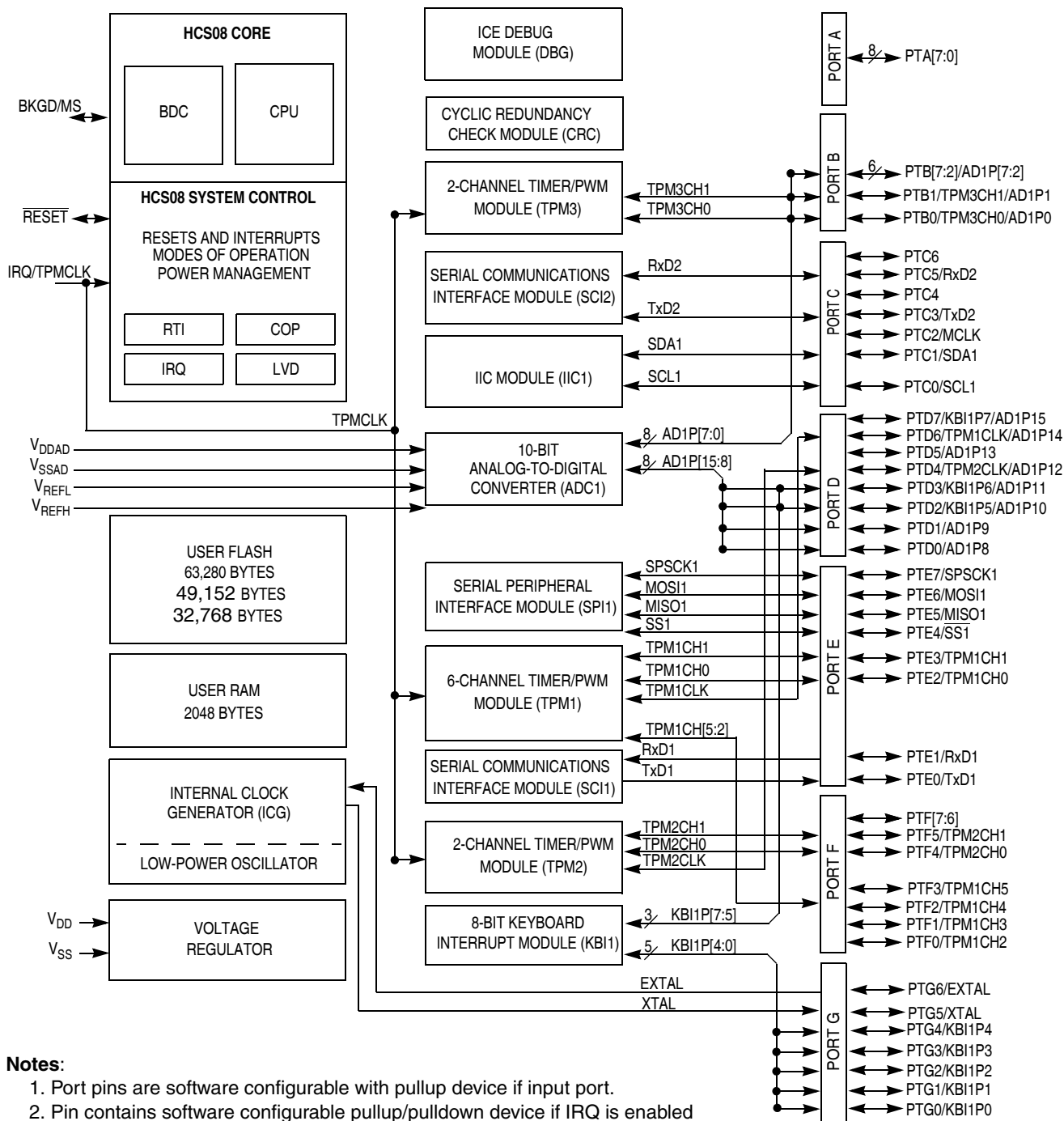


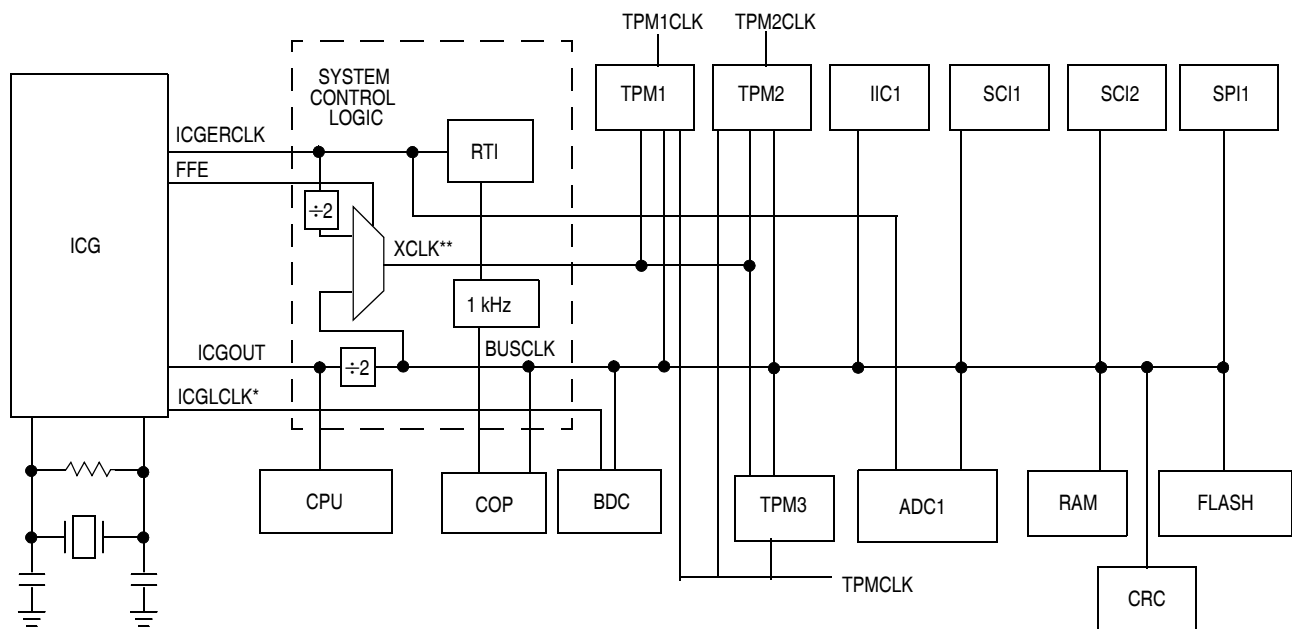
Figure 1-1. MC9S08AC60 Series Block Diagram

Table 1 lists the functional versions of the on-chip modules.

Table 1. Versions of On-Chip Modules

Module	Version
Cyclic Redundancy Check Generator (CRC)	1
Analog-to-Digital Converter (ADC)	1
Internal Clock Generator (ICG)	4
Inter-Integrated Circuit (IIC)	2
Keyboard Interrupt (KBI)	1
Serial Communications Interface (SCI)	4
Serial Peripheral Interface (SPI)	3
Timer Pulse-Width Modulator (TPM)	3
Central Processing Unit (CPU)	2
Debug Module (DBG)	2

1.3 System Clock Distribution



* ICGLCLK is the alternate BDC clock source for the MC9S08AC60 Series.

** Fixed frequency clock.

Figure 1-2. System Clock Distribution Diagram

Some of the modules inside the MCU have clock source choices. Figure 1-2 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
 - The external crystal oscillator

- An external clock source
- The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module
- Control bits inside the ICG determine which source is connected.
- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT $> 4 \times$ the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be ICGERCLK/2. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source. Can also be used as the ALTCLK input to the ADC module.