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Freescale Semiconductor, Inc.
Data Sheet

Document Number: MC9S08DZ128
Rev. 2, 07/2015

MC9S08DZ128 Series Data Sheet with Addenda

Rev.2 of the MC9S08DZ128 Series Data Sheet has three parts:

- The revision 2 of the addendum to revision 1 of the data sheet, immediately following this cover page.
- The revision 1 of the addendum to revision 1 of the data sheet, following the revision 2 of the addendum.
- Revision 1 of the data sheet, following the addendum revision 1. The changes described in the addenda have not been implemented in the specified pages.

Freescale Semiconductor, Inc.
Data Sheet Addendum

Document Number: MC9S08DZ128AD
Rev. 2, 07/2015

Addendum Rev.2 to Rev. 1 of the MC9S08DZ128 Series Data Sheet

This addendum identifies changes to Rev. 1 of the MC9S08DZ128 Series Data Sheet. The changes described in this addendum have not been implemented in the specified pages.

1 MCG Control Register 3 Field Descriptions

Location:	Table 8-7, Page 176

The last sentence of bit 4 (DIV32) description should be changed from "Writes to this bit are ignored if PLLS bit is set." to "DIV32 must be cleared when the PLL is selected." The correct description should be:

Field	Description
4 DIV32	**Divide-by-32 Enable** — Controls an additional divide-by-32 factor to the external reference clock for the FLL when RANGE bit is set. When the RANGE bit is 0, this bit has no effect. DIV32 must be cleared when the PLL is selected. 0 Divide-by-32 is disabled. 1 Divide-by-32 is enabled when RANGE=1.

2 Initializing the MCG

Location:	Section 8.5.1.1, Page 186

The last sentence in the note after step 6 should be removed. The note should be

NOTE

Setting DIV32 (bit 4) in MCGC3 is strongly recommended for FLL external modes when using a high frequency range (RANGE = 1) external reference clock.

3 Example # 1: Moving from FEI to PEE Mode: External Crystal = 8 MHz, Bus Frequency = 16 MHz

Location:	Section 8.5.3.1, Page 189

The first statement in step 2b should be “BLPE/PBE: MCGC3 = 0x48 (%01001000)”, and the second bullet in step 2b should be "DIV32 (bit 4) must be cleared when PLLS is set." The correct content should be:

a) BLPE: If a transition through BLPE mode is desired, first set LP (bit 3) in MCGC2 to 1.

b) BLPE/PBE: MCGC3 = 0x48 (%01001000)

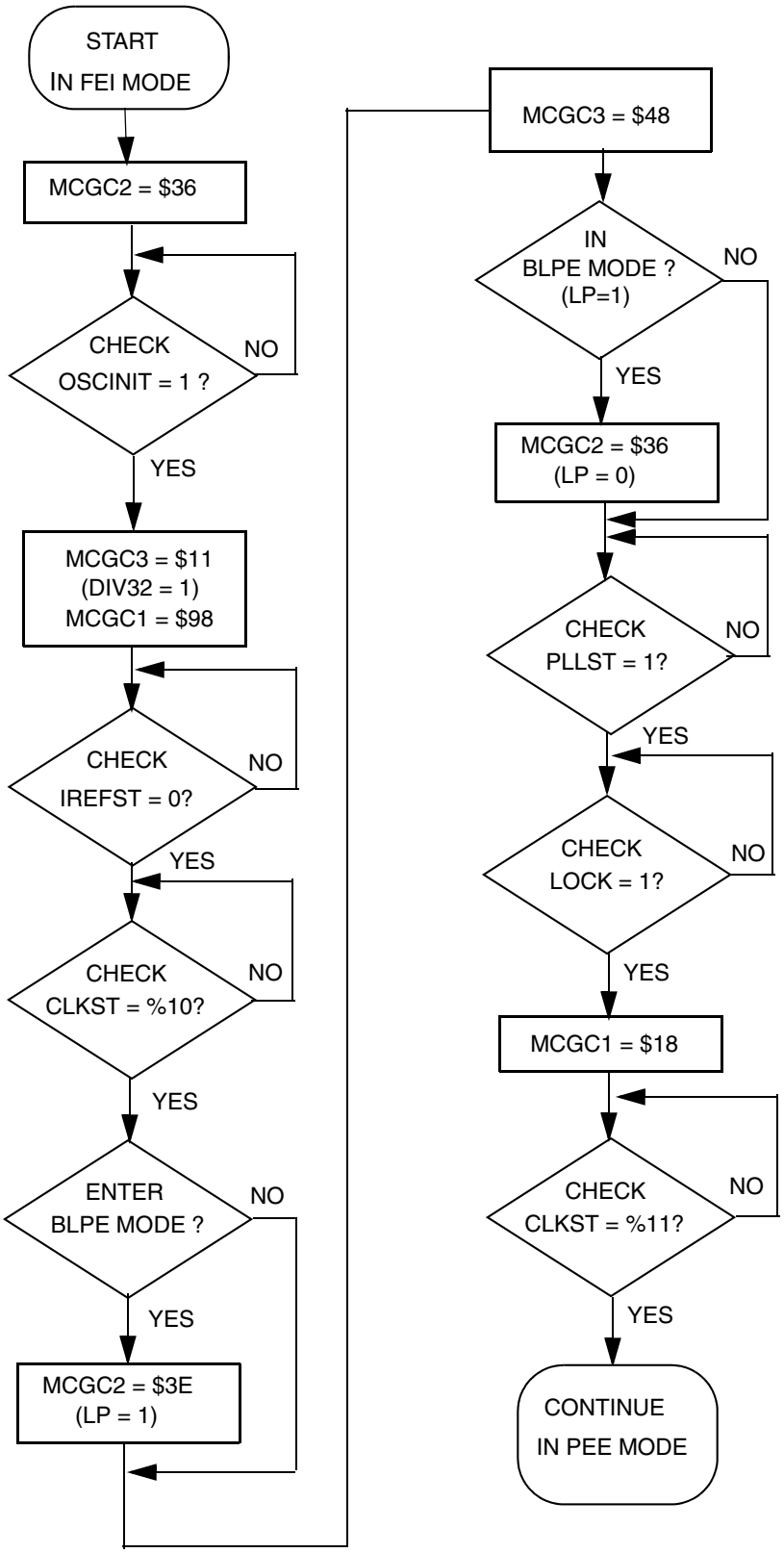
- PLLS (bit 6) set to 1, selects the PLL. At this time, with an RDIV value of %011, the FLL reference divider of 256 is switched to the PLL reference divider of 8 (see Table 8-3), resulting in a reference frequency of 8 MHz/ 8 = 1 MHz. In BLPE mode,changing the PLLS bit only prepares the MCG for PLL usage in PBE mode
- DIV32 (bit 4) must be cleared when PLLS is set.
- VDIV (bits 3-0) set to %1000, or multiply-by-32 because 1 MHz reference * 32= 32MHz. In BLPE mode, the configuration of the VDIV bits does not matter because the PLL is disabled. Changing them only sets up the multiply value for PLL usage in PBE mode

4 Flowchart of FEI to PEE Mode Transition using an 8 MHz crystal

Location:	Section 8.5.3.1, Page 190

The "MCGC3 = $58" in top right box of flowchart should be"MCGC3 = $48". The correct figure should be:

Flowchart of FEI to PEE Mode Transition using an 8 MHz crystal



5 DC Characteristics

Location:	Table A-6 Page 424

The minimum value in parameter 24, Bandgap Voltage Reference, from 1.19V to 1.18V. Remove "Temp = 25 °C" from footnote 10. The correct rating and footnote 10 should be:

Num	C	Characteristic	Symbol	Condition	Min	Typ	Max	Unit
24	P	Bandgap Voltage Reference [10]	V_{BG}		1.18	1.20	1.21	V

10 Factory trimmed at V_{DD} = 5.0 V.

6 Oscillator Electrical Specifications

Location:	Table A-11 Page 435

- Update the parameter 1, Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1), as shown below, to correct the maximum high range oscillator frequencies with respect to the HGO bit setting.
- Replace parameter 6, Square wave input clock frequency (EREFS = 0, ERCLKEN = 1), as shown below to correct the maximum square wave input clock frequency for FEE or FBE modes.
- Replace footnotes 1 and 2 as shown below to correct the typical characterization voltage and add the DIV32 divisor.

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1, HGO = 1) [2,3]	f_{hi-hgo}	1	—	16	MHz
		High range (RANGE = 1, HGO = 0)[2,3]	f_{hi-lp}	1	—	8	MHz

6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					
		FEE or FBE mode [2]	f_{extal}	0.03125	—	16	MHz
		PEE or PBE mode[3]		1	—	16	
		BLPE mode		0	—	40	

1 Data in Typical column was characterized at 5.0 V, 25° C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV and DIV32 to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

7 MCG Specifications

Location:	Table A-12 Page 436

The f_{int_ut} in the rating of the f_{dco_t} should be f_{int_t}. The correct rating should be:

Num	C	Rating		Symbol	Min	Typical	Max	Unit
6	P	DCO output frequency range - trimmed[2]	Low range (DRS=0, DMX32=0) $f_{dco\_t} = 512 \times f_{int\_t}$	f_{dco_t}	16	—	20	MHz
	P		Mid range (DRS=1, DMX32=0) $f_{dco\_t} = 1024 \times f_{int\_t}$		32	—	40	

Freescale Semiconductor, Inc.
Data Sheet Addendum

Document Number: MC9S08DZ128AD
Rev.1, 07/2011

Addendum Rev.1 to Rev. 1 of the MC9S08DZ128 Series Data Sheet

This addendum identifies changes to Rev. 1 of the MC9S08DZ128 Series Data Sheet. The changes described in this addendum have not been implemented in the specified pages.

1 Pin Availability by Package Pin-Count

Location:	Table 2-1, Page 34

Pin assignments for rows numbered 9— 15 in table 2-1 required updating. The correct information should be:

Pin Number			<-- Lowest **Priority** --> Highest			
100	**64**	**48**	**Port Pin/Interrupt**		**Alt 1**	**Alt 2**
9	7	4				V_{DD}
10	8	5				V_{SS}
11	9	6	PTG0		EXTAL	
12	10	7	PTG1		XTAL	
13	11	8				$\overline{\text{RESET}}$
14	—	—	PTJ2	PIJ2	TPM3CH2	
15	—	—	PTJ3	PIJ3	TPM3CH3	

2 Edge-Aligned PWM Mode

Location:	Section 16.4.2.3, Page 373

The following text should be added to the end of Section 16.4.2.3:

Writing to TPMxSC cancels any values written to TPMxMODH and/or TPMxMODL and resets the coherency mechanism for the modulo registers. Writing to TPMxCnSC cancels any values written to the channel value registers and resets the coherency mechanism for TPMxCnVH:TPMxCnVL.

MC9S08DZ128
MC9S08DZ96
MC9S08DV128
MC9S08DV96

Data Sheet

HCS08
Microcontrollers

MC9S08DZ128
Rev. 1
5/2008

freescale.com

MC9S08DZ128 Series Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (20-MHz bus)
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

On-Chip Memory

- FLASH read/program/erase over full operating voltage and temperature
- EEPROM in-circuit programmable memory; 8-byte single-page or 4-byte dual-page erase sector; Program and Erase while executing FLASH; Erase abort
- Random-access memory (RAM)

	MC9S08 DZ128	MC9S08 DZ96	MC9S08 DV128	MC9S08 DV96
FLASH	128K	96K	128K	96K
EEPROM	2K	2K	—	—
RAM	8K	6K	6K	4K

Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode
- Very low power real time interrupt for use in run, wait, and stop

Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Multi-purpose Clock Generator (MCG) — PLL and FLL modes; reference clock with nonvolatile trim (0.2% resolution, 1.5% tolerance over temperature with internal temperature compensation); External reference with oscillator/resonator options

System Protection

- Watchdog computer operating properly (COP) reset with option to run from backup dedicated 1-kHz internal clock source or bus clock; with optional windowed operation
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH and EEPROM block protect
- Loss-of-lock protection

Development Support

- Single-wire background debug interface
- On-chip, in-circuit emulation (ICE) with real-time bus capture

Peripherals

- **ADC** — 24-channel, 12-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel
- **ACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; runs in stop3 mode
- **MSCAN** — CAN protocol - Version 2.0 A, B; standard and extended data frames; Support for remote frames; Five receive buffers with FIFO storage scheme; Flexible identifier acceptance filters programmable as: 2 x 32-bit, 4 x 16-bit, or 8 x 8-bit
- **SCIx** — Two SCIs supporting LIN 2.0 Protocol and SAE J2602 protocols; Full duplex non-return to zero (NRZ); Master extended break generation; Slave extended break detection; Wakeup on active edge
- **SPIx** — Up to two SPIs; Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IICx** — Up to two IICs; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; General Call Address; Interrupt driven byte-by-byte data transfer
- **TPMx** — One 6-channel (TPM1), one 2-channel (TPM2) and one 4-channel (TPM3); Selectable input capture, output compare, or buffered edge- and center-aligned PWM on each channel.
- **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; Real-time clock capabilities using external crystal and RTC for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components

Input/Output

- Up to 87 general-purpose input/output (I/O) pins and 1 input-only pin
- Up to 32 interrupt pins with selectable polarity on each pin
- Hysteresis and configurable pull device on all input pins.
- Configurable slew rate and drive strength on all output pins.

Package Options

- 100-pin low-profile quad flat-pack(LQFP) — 14x14 mm
- 64-pin low-profile quad flat-pack (LQFP) — 10x10 mm
- 48-pin low-profile quad flat-pack (LQFP) — 7x7 mm

MC9S08DZ128 Series Data Sheet

Covers: MC9S08DZ128
MC9S08DZ96
MC9S08DV128
MC9S08DV96

MC9S08DZ128
Rev. 1
5/2008

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	4/2008	Initial Release

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