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Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC9S08GB60A
MC9S08GB32A
MC9S08GT60A
MC9S08GT32A

Data Sheet

HCS08
Microcontrollers

MC9S08GB60A
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MC9S08GB60A Data Sheet

Covers: MC9S08GB60A
MC9S08GB32A
MC9S08GT60A
MC9S08GT32A

MC9S08GB60A
Rev. 2
07/2008

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1.00	07/14/2005	Initial public release.
1.01	09/04/2007	Added a footnote to RTI of Table 3.2; Added RTI description to Section 3.5.6; Added a sentence "If active BDM mode is enabled in stop3, the internal RTI clock is not available." to the Section 5.7 Real Time Interrupt.
1.02	02/25/2008	Changed the Maximun Low Power of FBE and FEE in Table A-9 to 10 MHz. Changed the Title of Table 13-2 from “IIC1A Register Field Descriptions” to “IIC1F Register Field Descriptions”
2	7/30/2008	Added 42-pin SDIP information. Changed “However, when HGO=0, the maximum frequency is 8 MHz in FEE and FBE modes.” to “However, when HGO=0, the maximum frequency is 10 MHz in FEE and FBE modes.” in Appendix B5. Updated the “How to reach us” at backpage.

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Chapter 1
Device Overview

1.1 Overview

The MC9S08GBxxA/GTxxA are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.2 Features

Features have been organized to reflect:

- Standard features of the HCS08 Family
- Features of the MC9S08GBxxA/GTxxA MCU

1.2.1 Standard Features of the HCS08 Family

- 40-MHz HCS08 CPU (central processor unit)
- HC08 instruction set with added BGND instruction
- Background debugging system (see also Chapter 15, “Development Support”)
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources
- Power-saving modes: wait plus three stops
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset (some devices don’t have illegal addresses)

1.2.2 Features of MC9S08GBxxA/GTxxA Series of MCUs

- On-chip in-circuit programmable flash memory:
  - Fully read/write functional across voltage and temperature ranges
  - Block protection and security options
  - (see Table 1-1 for device-specific information)
- On-chip random-access memory (RAM) (see Table 1-1 for device specific information)
- 8-channel, 10-bit analog-to-digital converter (ATD)
- Two serial communications interface modules (SCI)
- Serial peripheral interface module (SPI)
- Multiple clock source options:
  - Internally generated clock with ±0.2% trimming resolution and ±0.5% deviation across voltage
  - Crystal
  - Resonator
  - External clock
- Inter-integrated circuit bus module to operate up to 100 kbps (IIC)
- One 3-channel and one 5-channel 16-bit timer/pulse width modulator (TPM) modules with selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels (TPMx).
- 8-pin keyboard interrupt module (KBI)
- 16 high-current pins (limited by package dissipation)
- Software selectable pullups on ports when used as input. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullup on $\overline{\text{RESET}}$ and IRQ pin to reduce customer system cost
- Up to 56 general-purpose input/output (I/O) pins, depending on package selection
- 64-pin low-profile quad flat package (LQFP) — MC9S08GBxxA
- 48-pin quad flat package, no lead (QFN) — MC9S08GTxxA
- 44-pin quad flat package (QFP) — MC9S08GTxxA
- 42-pin skinny dual in-line package (SDIP) — MC9S08GTxxA

1.2.3 Devices in the MC9S08GBxxA/GTxxA Series

Table 1-1 lists the devices available in the MC9S08GBxxA/GTxxA series and summarizes the differences among them.

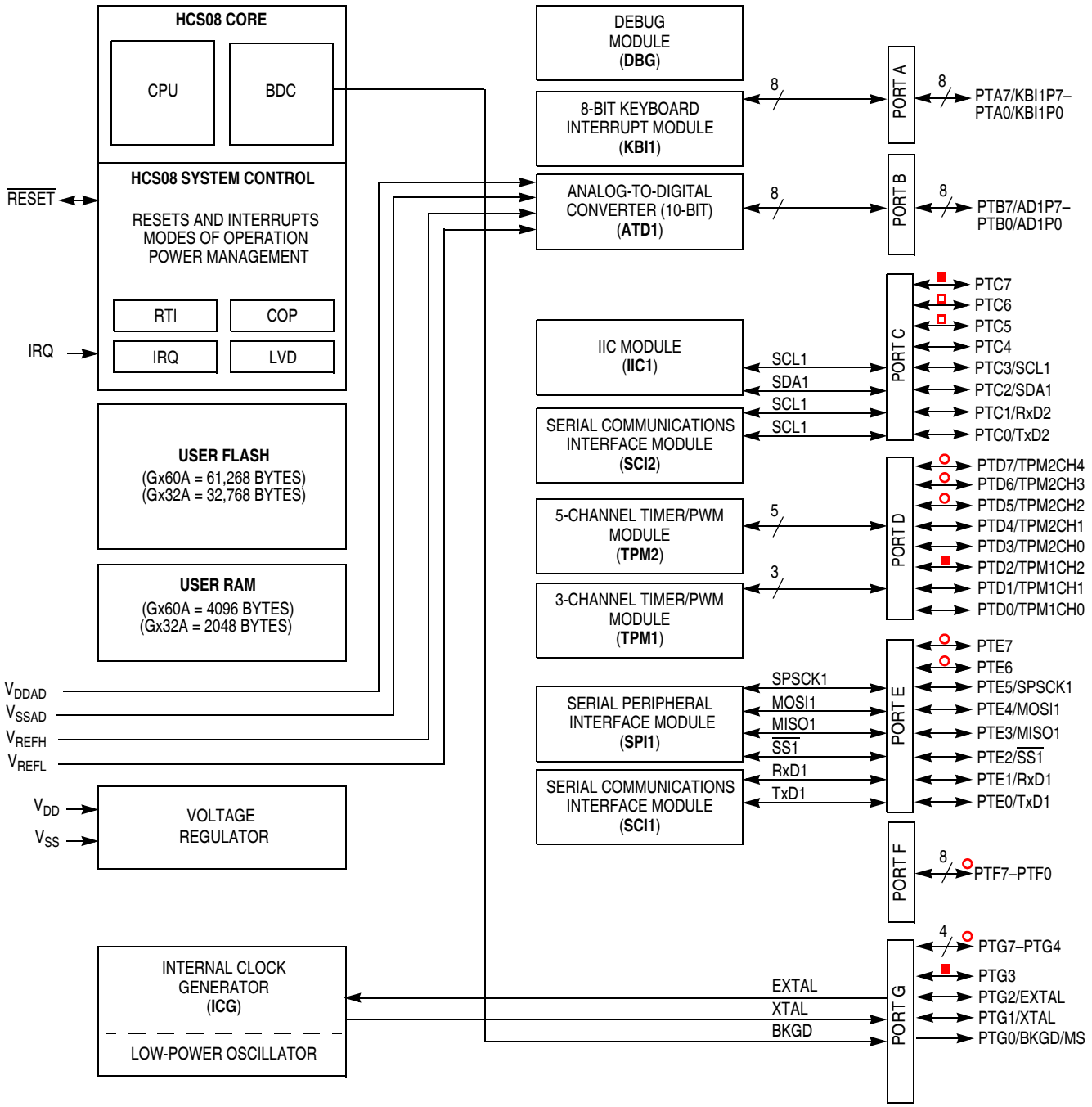
Table 1-1. Devices in the MC9S08GBxxA/GTxxA Series

Device	Flash	RAM	TPM	I/O	Packages
MC9S08GB60A	60K	4K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GB32A	32K	2K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GT60A	60K	4K	Two 2-channel, 16-bit timers	39 36 33	48 QFN[1] 44 QFP 42 SDIP
MC9S08GT32A	32K	2K	Two 2-channel, 16-bit timers	39 36 33	48 QFN(1) 44 QFP 42 SDIP

1 The 48-pin QFN package has one 3-channel and one 2-channel 16-bit TPM.

1.3 MCU Block Diagrams

These block diagrams show the structure of the MC9S08GBxxA/GTxxA MCUs.



Note: Not all pins are bonded out in all packages. See Table 2-2 for complete details.

Block Diagram Symbol Key:
○ = Not connected in 48-, 44-, and 42-pin packages
■ = Not connected in 44- and 42-pin packages
□ = Not connected in 42-pin packages

Figure 1-1. MC9S08GBxxA/GTxxA Block Diagram

Table 1-2 lists the functional versions of the on-chip modules.

Table 1-2. Block Versions

Module	Version
Analog-to-Digital Converter (ATD)	3
Internal Clock Generator (ICG)	2
Inter-Integrated Circuit (IIC)	1
Keyboard Interrupt (KBI)	1
Serial Communications Interface (SCI)	1
Serial Peripheral Interface (SPI)	3
Timer Pulse-Width Modulator (TPM)	1
Central Processing Unit (CPU)	2

1.4 System Clock Distribution

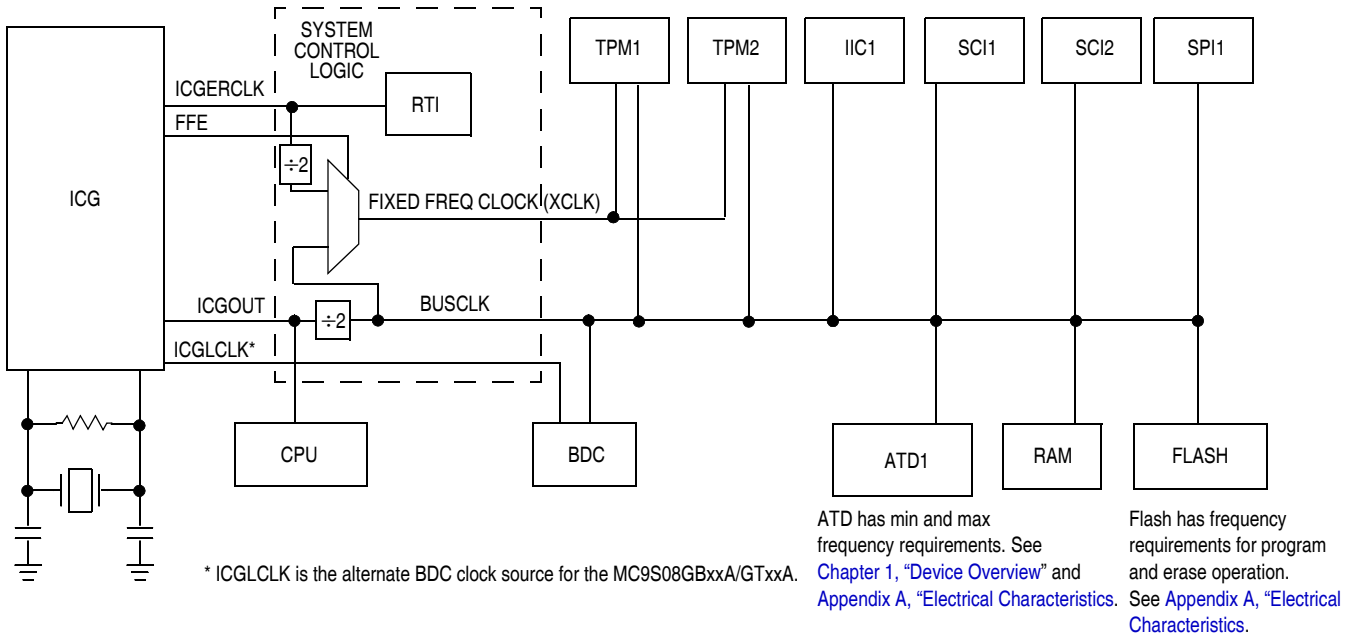


Figure 1-2. System Clock Distribution Diagram

Some of the modules inside the MCU have clock source choices. Figure 1-2 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
  - The external crystal oscillator
  - An external clock source
  - The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module

  Control bits inside the ICG determine which source is connected.

- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT > 4 × the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be the ICGERCLK. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source.

Chapter 2
Pins and Connections

2.1 Introduction

This section describes signals that connect to package pins. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals.