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# Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to [Freescale.com](http://Freescale.com) and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

**MC9S08GB60A**  
**MC9S08GB32A**  
**MC9S08GT60A**  
**MC9S08GT32A**

Data Sheet

***HCS08***  
***Microcontrollers***

MC9S08GB60A  
Rev. 2  
07/2008

[freescale.com](http://freescale.com)



# MC9S08GB60A Data Sheet

Covers: MC9S08GB60A  
MC9S08GB32A  
MC9S08GT60A  
MC9S08GT32A

MC9S08GB60A  
Rev. 2  
07/2008

# Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com>

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1.00	07/14/2005	Initial public release.
1.01	09/04/2007	Added a footnote to RTI of Table 3.2; Added RTI description to Section 3.5.6; Added a sentence "If active BDM mode is enabled in stop3, the internal RTI clock is not available." to the Section 5.7 Real Time Interrupt.
1.02	02/25/2008	Changed the Maximum Low Power of FBE and FEE in Table A-9 to 10 MHz. Changed the Title of Table 13-2 from "IIC1A Register Field Descriptions" to "IIC1F Register Field Descriptions"
2	7/30/2008	Added 42-pin SDIP information. Changed "However, when HGO=0, the maximum frequency is 8 MHz in FEE and FBE modes." to "However, when HGO=0, the maximum frequency is 10 MHz in FEE and FBE modes." in Appendix B5. Updated the "How to reach us" at backpage.

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## List of Chapters

Chapter Number	Title	Page
Chapter 1	Device Overview .....	17
Chapter 2	Pins and Connections .....	23
Chapter 3	Modes of Operation .....	35
Chapter 4	Memory .....	43
Chapter 5	Resets, Interrupts, and System Configuration .....	65
Chapter 6	Parallel Input/Output .....	81
Chapter 7	Internal Clock Generator (S08ICGV2) .....	103
Chapter 8	Central Processor Unit (S08CPUV2) .....	129
Chapter 9	Keyboard Interrupt (S08KBIV1) .....	149
Chapter 10	Timer/PWM (S08TPMV1) .....	155
Chapter 11	Serial Communications Interface (S08SCIV1).....	171
Chapter 12	Serial Peripheral Interface (S08SPIV3).....	189
Chapter 13	Inter-Integrated Circuit (S08IICV1) .....	205
Chapter 14	Analog-to-Digital Converter (S08ATDV3) .....	223
Chapter 15	Development Support .....	239
Appendix A	Electrical Characteristics.....	261
Appendix B	EB652: Migrating from the GB60 Series to the GB60A Series .....	283
Appendix C	Ordering Information and Mechanical Drawings.....	287





# Contents

Section Number	Title	Page
<b>Chapter 1</b>		
<b>Device Overview</b>		
1.1	Overview .....	17
1.2	Features .....	17
1.2.1	Standard Features of the HCS08 Family .....	17
1.2.2	Features of MC9S08GBxxA/GTxxA Series of MCUs .....	18
1.2.3	Devices in the MC9S08GBxxA/GTxxA Series .....	19
1.3	MCU Block Diagrams .....	19
1.4	System Clock Distribution .....	21
<b>Chapter 2</b>		
<b>Pins and Connections</b>		
2.1	Introduction .....	23
2.2	Device Pin Assignment .....	24
2.3	Recommended System Connections .....	27
2.3.1	Power .....	29
2.3.2	Oscillator .....	29
2.3.3	Reset .....	29
2.3.4	Background / Mode Select (PTG0/BKGD/MS) .....	30
2.3.5	General-Purpose I/O and Peripheral Ports .....	30
2.3.6	Signal Properties Summary .....	32
<b>Chapter 3</b>		
<b>Modes of Operation</b>		
3.1	Introduction .....	35
3.2	Features .....	35
3.3	Run Mode .....	35
3.4	Active Background Mode .....	35
3.5	Wait Mode .....	36
3.6	Stop Modes .....	36
3.6.1	Stop1 Mode .....	37
3.6.2	Stop2 Mode .....	37
3.6.3	Stop3 Mode .....	38
3.6.4	Active BDM Enabled in Stop Mode .....	38
3.6.5	LVD Enabled in Stop Mode .....	39
3.6.6	On-Chip Peripheral Modules in Stop Modes .....	39

Section Number	Title	Page
<b>Chapter 4</b>		
<b>Memory</b>		
4.1	MC9S08GBxxA/GTxxA Memory Map .....	43
4.1.1	Reset and Interrupt Vector Assignments .....	43
4.2	Register Addresses and Bit Assignments .....	45
4.3	RAM .....	50
4.4	Flash .....	50
4.4.1	Features .....	51
4.4.2	Program and Erase Times .....	51
4.4.3	Program and Erase Command Execution .....	52
4.4.4	Burst Program Execution .....	53
4.4.5	Access Errors .....	55
4.4.6	Flash Block Protection .....	55
4.4.7	Vector Redirection .....	56
4.5	Security .....	56
4.6	Flash Registers and Control Bits .....	57
4.6.1	Flash Clock Divider Register (FCDIV) .....	57
4.6.2	Flash Options Register (FOPT and NVOPT) .....	59
4.6.3	Flash Configuration Register (FCNFG) .....	60
4.6.4	Flash Protection Register (FPROT and NVPROT) .....	60
4.6.5	Flash Status Register (FSTAT) .....	62
4.6.6	Flash Command Register (FCMD) .....	63
<b>Chapter 5</b>		
<b>Resets, Interrupts, and System Configuration</b>		
5.1	Introduction .....	65
5.2	Features .....	65
5.3	MCU Reset .....	65
5.4	Computer Operating Properly (COP) Watchdog .....	66
5.5	Interrupts .....	66
5.5.1	Interrupt Stack Frame .....	67
5.5.2	External Interrupt Request (IRQ) Pin .....	68
5.5.2.1	Pin Configuration Options .....	68
5.5.2.2	Edge and Level Sensitivity .....	69
5.5.3	Interrupt Vectors, Sources, and Local Masks .....	69
5.6	Low-Voltage Detect (LVD) System .....	71
5.6.1	Power-On Reset Operation .....	71
5.6.2	LVD Reset Operation .....	71
5.6.3	LVD Interrupt Operation .....	71
5.6.4	Low-Voltage Warning (LVW) .....	71
5.7	Real-Time Interrupt (RTI) .....	71
5.8	Reset, Interrupt, and System Control Registers and Control Bits .....	72
5.8.1	Interrupt Pin Request Status and Control Register (IRQSC) .....	73

Section Number	Title	Page
5.8.2	System Reset Status Register (SRS) .....	74
5.8.3	System Background Debug Force Reset Register (SBDFR) .....	75
5.8.4	System Options Register (SOPT) .....	76
5.8.5	System Device Identification Register (SDIDH, SDIDL) .....	77
5.8.6	System Real-Time Interrupt Status and Control Register (SRTISC) .....	78
5.8.7	System Power Management Status and Control 1 Register (SPMSC1) .....	79
5.8.8	System Power Management Status and Control 2 Register (SPMSC2) .....	80

## Chapter 6 Parallel Input/Output

6.1	Introduction .....	81
6.2	Features .....	83
6.3	Pin Descriptions .....	83
6.3.1	Port A and Keyboard Interrupts .....	83
6.3.2	Port B and Analog to Digital Converter Inputs .....	84
6.3.3	Port C and SCI2, IIC, and High-Current Drivers .....	84
6.3.4	Port D, TPM1 and TPM2 .....	85
6.3.5	Port E, SCI1, and SPI .....	85
6.3.6	Port F and High-Current Drivers .....	86
6.3.7	Port G, BKGD/MS, and Oscillator .....	86
6.4	Parallel I/O Controls .....	87
6.4.1	Data Direction Control .....	87
6.4.2	Internal Pullup Control .....	87
6.4.3	Slew Rate Control .....	87
6.5	Stop Modes .....	88
6.6	Parallel I/O Registers and Control Bits .....	88
6.6.1	Port A Registers (PTAD, PTAPE, PTASE, and PTADD) .....	88
6.6.2	Port B Registers (PTBD, PTBPE, PTBSE, and PTBDD) .....	91
6.6.3	Port C Registers (PTCD, PTCPE, PTCSE, and PTCDD) .....	93
6.6.4	Port D Registers (PTDD, PTDPE, PTDSE, and PTDDD) .....	95
6.6.5	Port E Registers (PTED, PTEPE, PTESE, and PTEDD) .....	97
6.6.6	Port F Registers (PTFD, PTFPE, PTFSE, and PTFDD) .....	99
6.6.7	Port G Registers (PTGD, PTGPE, PTGSE, and PTGDD) .....	100

## Chapter 7 Internal Clock Generator (S08ICGV2)

7.1	Introduction .....	105
7.1.1	Features .....	106
7.1.2	Modes of Operation .....	107
7.2	Oscillator Pins .....	107
7.2.1	EXTAL— External Reference Clock / Oscillator Input .....	107
7.2.2	XTAL— Oscillator Output .....	107

Section Number	Title	Page
7.2.3	External Clock Connections .....	108
7.2.4	External Crystal/Resonator Connections .....	108
7.3	Functional Description .....	109
7.3.1	Off Mode (Off) .....	109
7.3.1.1	BDM Active .....	109
7.3.1.2	OSCSTEN Bit Set .....	109
7.3.1.3	Stop/Off Mode Recovery .....	109
7.3.2	Self-Clocked Mode (SCM) .....	109
7.3.3	FLL Engaged, Internal Clock (FEI) Mode .....	111
7.3.3.1	FLL Engaged Internal Unlocked .....	111
7.3.3.2	FLL Engaged Internal Locked .....	111
7.3.4	FLL Bypassed, External Clock (FBE) Mode .....	111
7.3.5	FLL Engaged, External Clock (FEE) Mode .....	111
7.3.5.1	FLL Engaged External Unlocked .....	112
7.3.5.2	FLL Engaged External Locked .....	112
7.3.6	FLL Lock and Loss-of-Lock Detection .....	112
7.3.7	FLL Loss-of-Clock Detection .....	113
7.3.8	Clock Mode Requirements .....	114
7.3.9	Fixed Frequency Clock .....	115
7.3.10	High Gain Oscillator .....	115
7.4	Initialization/Application Information .....	115
7.4.1	Introduction .....	115
7.4.2	Example #1: External Crystal = 32 kHz, Bus Frequency = 4.19 MHz .....	118
7.4.3	Example #2: External Crystal = 4 MHz, Bus Frequency = 20 MHz .....	119
7.4.4	Example #3: No External Crystal Connection, 5.4 MHz Bus Frequency .....	121
7.4.5	Example #4: Internal Clock Generator Trim .....	122
7.5	ICG Registers and Control Bits .....	123
7.5.1	ICG Control Register 1 (ICGC1) .....	124
7.5.2	ICG Control Register 2 (ICGC2) .....	125
7.5.3	ICG Status Register 1 (ICGS1) .....	126
7.5.4	ICG Status Register 2 (ICGS2) .....	127
7.5.5	ICG Filter Registers (ICGFLTU, ICGFLTL) .....	127
7.5.6	ICG Trim Register (ICGTRM) .....	128

## Chapter 8 Central Processor Unit (S08CPUV2)

8.1	Introduction .....	129
8.1.1	Features .....	129
8.2	Programmer's Model and CPU Registers .....	130
8.2.1	Accumulator (A) .....	130
8.2.2	Index Register (H:X) .....	130
8.2.3	Stack Pointer (SP) .....	131
8.2.4	Program Counter (PC) .....	131
8.2.5	Condition Code Register (CCR) .....	131

Section Number	Title	Page
8.3	Addressing Modes .....	133
8.3.1	Inherent Addressing Mode (INH) .....	133
8.3.2	Relative Addressing Mode (REL) .....	133
8.3.3	Immediate Addressing Mode (IMM) .....	133
8.3.4	Direct Addressing Mode (DIR) .....	133
8.3.5	Extended Addressing Mode (EXT) .....	134
8.3.6	Indexed Addressing Mode .....	134
8.3.6.1	Indexed, No Offset (IX) .....	134
8.3.6.2	Indexed, No Offset with Post Increment (IX+) .....	134
8.3.6.3	Indexed, 8-Bit Offset (IX1) .....	134
8.3.6.4	Indexed, 8-Bit Offset with Post Increment (IX1+) .....	134
8.3.6.5	Indexed, 16-Bit Offset (IX2) .....	134
8.3.6.6	SP-Relative, 8-Bit Offset (SP1) .....	134
8.3.6.7	SP-Relative, 16-Bit Offset (SP2) .....	135
8.4	Special Operations .....	135
8.4.1	Reset Sequence .....	135
8.4.2	Interrupt Sequence .....	135
8.4.3	Wait Mode Operation .....	136
8.4.4	Stop Mode Operation .....	136
8.4.5	BGND Instruction .....	137
8.5	HCS08 Instruction Set Summary .....	138

## Chapter 9 Keyboard Interrupt (S08KBIV1)

9.1	Introduction .....	149
9.1.1	Port A and Keyboard Interrupt Pins .....	149
9.2	Features .....	149
9.2.1	KBI Block Diagram .....	151
9.3	Register Definition .....	151
9.3.1	KBI Status and Control Register (KBI1SC) .....	152
9.3.2	KBI Pin Enable Register (KBI1PE) .....	153
9.4	Functional Description .....	153
9.4.1	Pin Enables .....	153
9.4.2	Edge and Level Sensitivity .....	153
9.4.3	KBI Interrupt Controls .....	154

## Chapter 10 Timer/PWM (S08TPMV1)

10.1	Introduction .....	155
10.2	Features .....	155
10.3	TPM Block Diagram .....	157
10.4	Pin Descriptions .....	158
10.4.1	External TPM Clock Sources .....	158
10.4.2	TPMxCHn — TPMx Channel n I/O Pins .....	158
10.5	Functional Description .....	158

Section Number	Title	Page
10.5.1	Counter .....	159
10.5.2	Channel Mode Selection .....	160
10.5.2.1	Input Capture Mode .....	160
10.5.2.2	Output Compare Mode .....	160
10.5.2.3	Edge-Aligned PWM Mode .....	160
10.5.3	Center-Aligned PWM Mode .....	161
10.6	TPM Interrupts .....	163
10.6.1	Clearing Timer Interrupt Flags .....	163
10.6.2	Timer Overflow Interrupt Description .....	163
10.6.3	Channel Event Interrupt Description .....	163
10.6.4	PWM End-of-Duty-Cycle Events .....	164
10.7	TPM Registers and Control Bits .....	164
10.7.1	Timer x Status and Control Register (TPMxSC) .....	165
10.7.2	Timer x Counter Registers (TPMxCNTH:TPMxCNTL) .....	166
10.7.3	Timer x Counter Modulo Registers (TPMxMODH:TPMxMODL) .....	167
10.7.4	Timer x Channel n Status and Control Register (TPMxCnSC) .....	168
10.7.5	Timer x Channel Value Registers (TPMxCnVH:TPMxCnVL) .....	169

## Chapter 11

### Serial Communications Interface (S08SCIV1)

11.1	Introduction .....	171
11.1.1	Features .....	173
11.1.2	Modes of Operation .....	173
11.1.3	Block Diagram .....	174
11.2	Register Definition .....	176
11.2.1	SCI Baud Rate Registers (SCIxBDH, SCIxBHL) .....	176
11.2.2	SCI Control Register 1 (SCIxC1) .....	177
11.2.3	SCI Control Register 2 (SCIxC2) .....	178
11.2.4	SCI Status Register 1 (SCIxS1) .....	179
11.2.5	SCI Status Register 2 (SCIxS2) .....	181
11.2.6	SCI Control Register 3 (SCIxC3) .....	181
11.2.7	SCI Data Register (SCIxD) .....	182
11.3	Functional Description .....	183
11.3.1	Baud Rate Generation .....	183
11.3.2	Transmitter Functional Description .....	183
11.3.2.1	Send Break and Queued Idle .....	184
11.3.3	Receiver Functional Description .....	184
11.3.3.1	Data Sampling Technique .....	185
11.3.3.2	Receiver Wakeup Operation .....	185
11.3.4	Interrupts and Status Flags .....	186
11.3.5	Additional SCI Functions .....	187
11.3.5.1	8- and 9-Bit Data Modes .....	187
11.3.5.2	Stop Mode Operation .....	187
11.3.5.3	Loop Mode .....	188

Section Number	Title	Page
11.3.5.4	Single-Wire Operation .....	188

## Chapter 12 Serial Peripheral Interface (S08SPIV3)

12.1	Introduction .....	189
12.1.1	Features .....	191
12.1.2	Block Diagrams .....	191
12.1.2.1	SPI System Block Diagram .....	191
12.1.2.2	SPI Module Block Diagram .....	192
12.1.3	SPI Baud Rate Generation .....	193
12.2	External Signal Description .....	194
12.2.1	SPSCK — SPI Serial Clock .....	194
12.2.2	MOSI — Master Data Out, Slave Data In .....	194
12.2.3	MISO — Master Data In, Slave Data Out .....	194
12.2.4	$\overline{SS}$ — Slave Select .....	194
12.3	Modes of Operation .....	195
12.3.1	SPI in Stop Modes .....	195
12.4	Register Definition .....	195
12.4.1	SPI Control Register 1 (SPI1C1) .....	195
12.4.2	SPI Control Register 2 (SPI1C2) .....	196
12.4.3	SPI Baud Rate Register (SPI1BR) .....	197
12.4.4	SPI Status Register (SPI1S) .....	198
12.4.5	SPI Data Register (SPI1D) .....	199
12.5	Functional Description .....	200
12.5.1	SPI Clock Formats .....	200
12.5.2	SPI Interrupts .....	203
12.5.3	Mode Fault Detection .....	203

## Chapter 13 Inter-Integrated Circuit (S08IICV1)

13.1	Introduction .....	205
13.1.1	Features .....	207
13.1.2	Modes of Operation .....	207
13.1.3	Block Diagram .....	208
13.2	External Signal Description .....	208
13.2.1	SCL — Serial Clock Line .....	208
13.2.2	SDA — Serial Data Line .....	208
13.3	Register Definition .....	208
13.3.1	IIC Address Register (IIC1A) .....	209
13.3.2	IIC Frequency Divider Register (IIC1F) .....	209
13.3.3	IIC Control Register (IIC1C) .....	212



Section Number	Title	Page
13.3.4	IIC Status Register (IIC1S) .....	213
13.3.5	IIC Data I/O Register (IIC1D) .....	214
13.4	Functional Description .....	215
13.4.1	IIC Protocol .....	215
13.4.1.1	START Signal .....	216
13.4.1.2	Slave Address Transmission .....	216
13.4.1.3	Data Transfer .....	216
13.4.1.4	STOP Signal .....	217
13.4.1.5	Repeated START Signal .....	217
13.4.1.6	Arbitration Procedure .....	217
13.4.1.7	Clock Synchronization .....	217
13.4.1.8	Handshaking .....	218
13.4.1.9	Clock Stretching .....	218
13.5	Resets .....	218
13.6	Interrupts .....	218
13.6.1	Byte Transfer Interrupt .....	219
13.6.2	Address Detect Interrupt .....	219
13.6.3	Arbitration Lost Interrupt .....	219
13.7	Initialization/Application Information .....	220

## Chapter 14

### Analog-to-Digital Converter (S08ATDV3)

14.1	Introduction .....	225
14.1.1	Features .....	225
14.1.2	Modes of Operation .....	225
14.1.2.1	Stop Mode .....	225
14.1.2.2	Power Down Mode .....	225
14.1.3	Block Diagram .....	225
14.2	Signal Description .....	226
14.2.1	Overview .....	226
14.2.1.1	Channel Input Pins — AD1P7–AD1P0 .....	227
14.2.1.2	ATD Reference Pins — $V_{REFH}$ , $V_{REFL}$ .....	227
14.2.1.3	ATD Supply Pins — $V_{DDAD}$ , $V_{SSAD}$ .....	227
14.3	Functional Description .....	227
14.3.1	Mode Control .....	227
14.3.2	Sample and Hold .....	228
14.3.3	Analog Input Multiplexer .....	230
14.3.4	ATD Module Accuracy Definitions .....	230
14.4	Resets .....	233
14.5	Interrupts .....	233
14.6	ATD Registers and Control Bits .....	233
14.6.1	ATD Control (ATDC) .....	234
14.6.2	ATD Status and Control (ATD1SC) .....	236
14.6.3	ATD Result Data (ATD1RH, ATD1RL) .....	237

Section Number	Title	Page
14.6.4	ATD Pin Enable (ATD1PE) .....	238

## Chapter 15 Development Support

15.1	Introduction .....	239
15.1.1	Features .....	240
15.2	Background Debug Controller (BDC) .....	240
15.2.1	BKGD Pin Description .....	241
15.2.2	Communication Details .....	242
15.2.3	BDC Commands .....	246
15.2.4	BDC Hardware Breakpoint .....	248
15.3	On-Chip Debug System (DBG) .....	249
15.3.1	Comparators A and B .....	249
15.3.2	Bus Capture Information and FIFO Operation .....	249
15.3.3	Change-of-Flow Information .....	250
15.3.4	Tag vs. Force Breakpoints and Triggers .....	250
15.3.5	Trigger Modes .....	251
15.3.6	Hardware Breakpoints .....	253
15.4	Register Definition .....	253
15.4.1	BDC Registers and Control Bits .....	253
15.4.1.1	BDC Status and Control Register (BDCSCR) .....	254
15.4.1.2	BDC Breakpoint Match Register (BDCBKPT) .....	255
15.4.2	System Background Debug Force Reset Register (SBD FR) .....	255
15.4.3	DBG Registers and Control Bits .....	256
15.4.3.1	Debug Comparator A High Register (DBGCAH) .....	256
15.4.3.2	Debug Comparator A Low Register (DBGCAL) .....	256
15.4.3.3	Debug Comparator B High Register (DBGCBH) .....	256
15.4.3.4	Debug Comparator B Low Register (DBG CBL) .....	256
15.4.3.5	Debug FIFO High Register (DBGFH) .....	257
15.4.3.6	Debug FIFO Low Register (DBGFL) .....	257
15.4.3.7	Debug Control Register (DBG C) .....	258
15.4.3.8	Debug Trigger Register (DBG T) .....	259
15.4.3.9	Debug Status Register (DBG S) .....	260

## Appendix A Electrical Characteristics

A.1	Introduction .....	261
A.2	Absolute Maximum Ratings .....	261
A.3	Thermal Characteristics .....	262
A.4	Electrostatic Discharge (ESD) Protection Characteristics .....	263
A.5	DC Characteristics .....	263

Section Number	Title	Page
A.6	Supply Current Characteristics .....	267
A.7	ATD Characteristics .....	271
A.8	Internal Clock Generation Module Characteristics .....	273
A.8.1	ICG Frequency Specifications .....	274
A.9	AC Characteristics .....	275
A.9.1	Control Timing .....	276
A.9.2	Timer/PWM (TPM) Module Timing .....	277
A.9.3	SPI Timing .....	278
A.10	Flash Specifications .....	281

## Appendix B

### EB652: Migrating from the GB60 Series to the GB60A Series

B.1	Overview .....	283
B.2	Flash Programming Voltage .....	283
B.3	Flash Block Protection: 60K Devices Only .....	283
B.4	Internal Clock Generator: High Gain Oscillator Option .....	283
B.5	Internal Clock Generator: Low-Power Oscillator Maximum Frequency .....	284
B.6	Internal Clock Generator: Loss-of-Clock Disable Option .....	284
B.7	System Device Identification Register .....	285

## Appendix C

### Ordering Information and Mechanical Drawings

C.1	Ordering Information .....	287
C.2	Mechanical Drawings .....	288

# Chapter 1

## Device Overview

### 1.1 Overview

The MC9S08GBxxA/GTxxA are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

### 1.2 Features

Features have been organized to reflect:

- Standard features of the HCS08 Family
- Features of the MC9S08GBxxA/GTxxA MCU

#### 1.2.1 Standard Features of the HCS08 Family

- 40-MHz HCS08 CPU (central processor unit)
- HC08 instruction set with added BGND instruction
- Background debugging system (see also [Chapter 15, “Development Support”](#))
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources
- Power-saving modes: wait plus three stops
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset (some devices don't have illegal addresses)

## 1.2.2 Features of MC9S08GBxxA/GTxxA Series of MCUs

- On-chip in-circuit programmable flash memory:
  - Fully read/write functional across voltage and temperature ranges
  - Block protection and security options
  - (see [Table 1-1](#) for device-specific information)
- On-chip random-access memory (RAM) (see [Table 1-1](#) for device specific information)
- 8-channel, 10-bit analog-to-digital converter (ATD)
- Two serial communications interface modules (SCI)
- Serial peripheral interface module (SPI)
- Multiple clock source options:
  - Internally generated clock with  $\pm 0.2\%$  trimming resolution and  $\pm 0.5\%$  deviation across voltage
  - Crystal
  - Resonator
  - External clock
- Inter-integrated circuit bus module to operate up to 100 kbps (IIC)
- One 3-channel and one 5-channel 16-bit timer/pulse width modulator (TPM) modules with selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels (TPM<sub>x</sub>).
- 8-pin keyboard interrupt module (KBI)
- 16 high-current pins (limited by package dissipation)
- Software selectable pullups on ports when used as input. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullup on  $\overline{\text{RESET}}$  and IRQ pin to reduce customer system cost
- Up to 56 general-purpose input/output (I/O) pins, depending on package selection
- 64-pin low-profile quad flat package (LQFP) — MC9S08GBxxA
- 48-pin quad flat package, no lead (QFN) — MC9S08GTxxA
- 44-pin quad flat package (QFP) — MC9S08GTxxA
- 42-pin skinny dual in-line package (SDIP) — MC9S08GTxxA

### 1.2.3 Devices in the MC9S08GBxxA/GTxxA Series

Table 1-1 lists the devices available in the MC9S08GBxxA/GTxxA series and summarizes the differences among them.

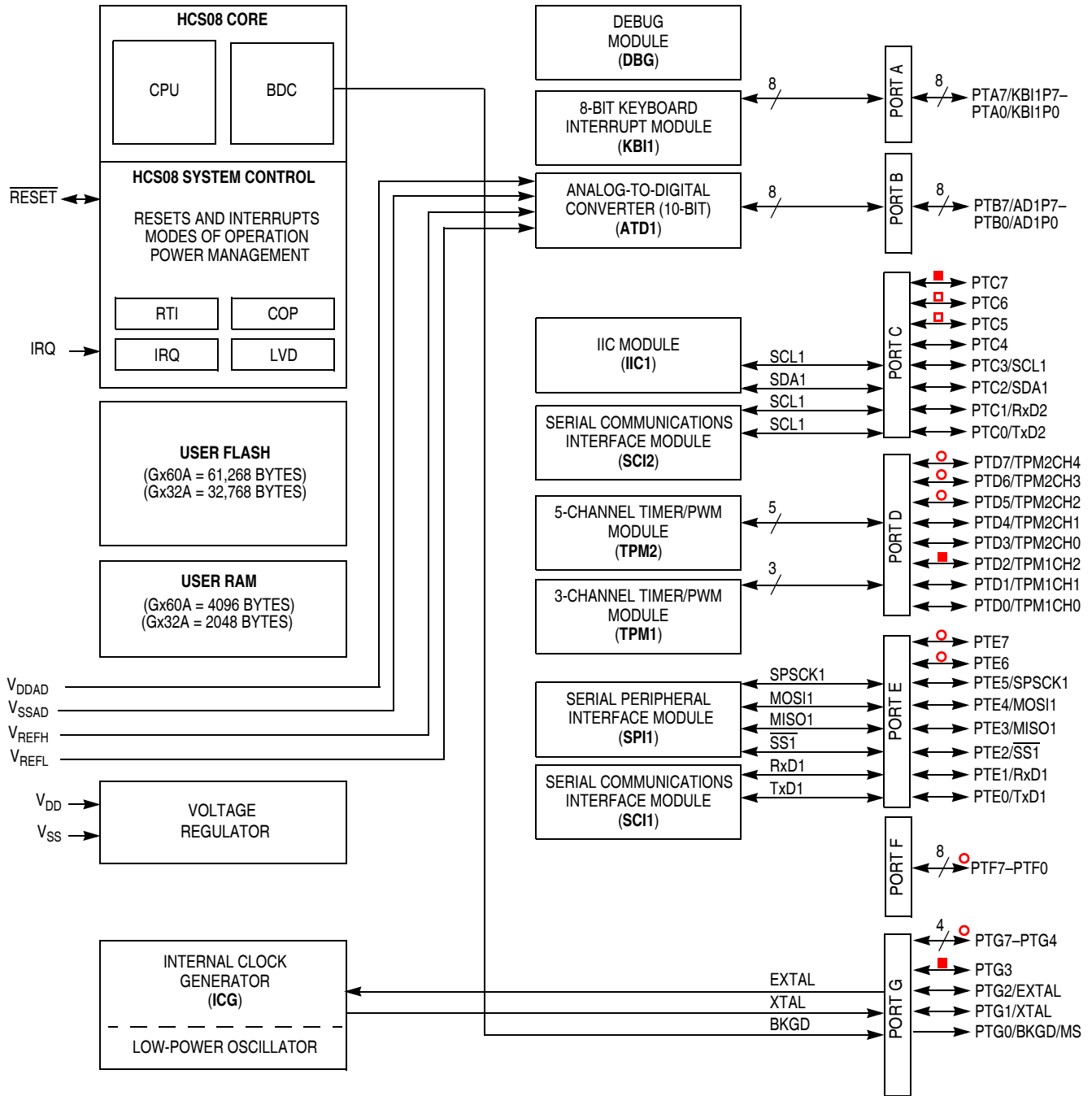
**Table 1-1. Devices in the MC9S08GBxxA/GTxxA Series**

Device	Flash	RAM	TPM	I/O	Packages
MC9S08GB60A	60K	4K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GB32A	32K	2K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GT60A	60K	4K	Two 2-channel, 16-bit timers	39 36 33	48 QFN <sup>1</sup> 44 QFP 42 SDIP
MC9S08GT32A	32K	2K	Two 2-channel, 16-bit timers	39 36 33	48 QFN <sup>(1)</sup> 44 QFP 42 SDIP

<sup>1</sup> The 48-pin QFN package has one 3-channel and one 2-channel 16-bit TPM.

## 1.3 MCU Block Diagrams

These block diagrams show the structure of the MC9S08GBxxA/GTxxA MCUs.



**Note:** Not all pins are bonded out in all packages. See Table 2-2 for complete details.

Block Diagram Symbol Key:	
○	= Not connected in 48-, 44-, and 42-pin packages
■	= Not connected in 44- and 42-pin packages
◻	= Not connected in 42-pin packages

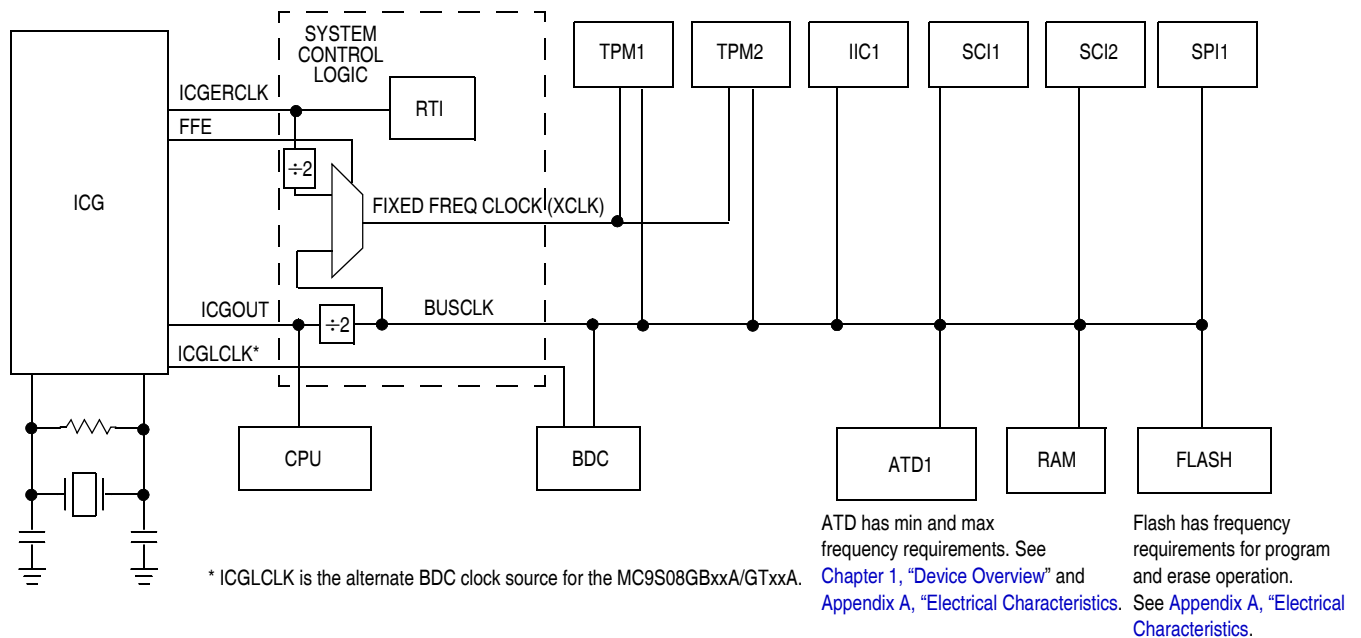
Figure 1-1. MC9S08GBxxA/GTxxA Block Diagram

Table 1-2 lists the functional versions of the on-chip modules.

**Table 1-2. Block Versions**

Module	Version
Analog-to-Digital Converter (ATD)	3
Internal Clock Generator (ICG)	2
Inter-Integrated Circuit (IIC)	1
Keyboard Interrupt (KBI)	1
Serial Communications Interface (SCI)	1
Serial Peripheral Interface (SPI)	3
Timer Pulse-Width Modulator (TPM)	1
Central Processing Unit (CPU)	2

## 1.4 System Clock Distribution



**Figure 1-2. System Clock Distribution Diagram**

Some of the modules inside the MCU have clock source choices. Figure 1-2 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
  - The external crystal oscillator
  - An external clock source
  - The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module

Control bits inside the ICG determine which source is connected.



- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT  $> 4 \times$  the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be the ICGERCLK. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source.

## **Chapter 2**

# **Pins and Connections**

### **2.1 Introduction**

This section describes signals that connect to package pins. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals.