Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MC9S08GB60
MC9S08GB32
MC9S08GT60
MC9S08GT32
MC9S08GT16

Data Sheet

HCS08
Microcontrollers

MC9S08GB60/D
Rev. 2.3
12/2004

freescale.com

freescale™
semiconductor

MC9S08GB/GT Data Sheet

Covers: MC9S08GB60
MC9S08GB32
MC9S08GT60
MC9S08GT32
MC9S08GT16

MC9S08GB60
Rev. 2.3
12/2004

freescale™
semiconductor

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1.0	4/25/2003	Initial release
1.1		Electricals change, appendix A only
1.2		Electricals change, appendix A only
1.3	10/2/2003	Added module version table; clarifications
1.4	10/29/2003	Fixed typos and made corrections and clarifications
1.5	11/12/2003	Added 1-MHz I_{DD} values to Electricals, appendix A
2	2/10/2004	Changed format of register names to enable reuse of code (from SCIBD to SCI1BD, even when only one instance of a module on a chip) Added new device: MC9S08GT16 to book. Added new 48-pin QFN package to book. BKGDPE description in Section 5 — changed PTD0 to PTG0. Changed typo in CPU section that listed MOV instruction as being 6 cycles instead of 5 (Table 8-2).
2.2	9/2/2004	Format to Freescale look-and-feel; Clarified RTI clock sources and other changes in Chapter 5; updated ICG initialization examples; expanded descriptions of LOLS and LOCS bits in ICGS1; updated ICG electricals Table A-9 and added a figure
2.3	12/01/2004	Minor changes to Table 7-4, Table 7-5, Table A-9; Clarifications in Section 11.10.6, “SCI x Control Register 3 (SCIxC3)”, Section 11.7, “Interrupts and Status Flags”, Section 11.8.1, “8- and 9-Bit Data Modes”, PTG availability in 48-pin package (see Table 2-2)

This product incorporates SuperFlash® technology licensed from SST.

List of Chapters

Contents

Section Number **Title** **Page**

Chapter 1
Introduction

Chapter 2
Pins and Connections

Chapter 3
Modes of Operation

Chapter 4
Memory

Chapter 5
Resets, Interrupts, and System Configuration

Chapter 6
Parallel Input/Output

Chapter 7
Internal Clock Generator (ICG) Module

Chapter 8
Central Processor Unit (CPU)

Chapter 9
Keyboard Interrupt (KBI) Module

Chapter 10
Timer/PWM (TPM) Module

Chapter 11
Serial Communications Interface (SCI) Module

Chapter 12
Serial Peripheral Interface (SPI) Module

Chapter 13
Inter-Integrated Circuit (IIC) Module

Chapter 14
Analog-to-Digital Converter (ATD) Module

Chapter 15
Development Support

Appendix A
Electrical Characteristics

Appendix B
Ordering Information and Mechanical Drawings

Chapter 1 Introduction

1.1 Overview

The MC9S08GB/GT are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.2 Features

Features have been organized to reflect:

- Standard features of the HCS08 Family
- Features of the MC9S08GB/GT MCU

1.2.1 Standard Features of the HCS08 Family

- 40-MHz HCS08 CPU (central processor unit)
- HC08 instruction set with added BGND instruction
- Background debugging system (see also Chapter 15, “Development Support”)
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources
- Power-saving modes: wait plus three stops
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset (some devices don’t have illegal addresses)

1.2.2 Features of MC9S08GB/GT Series of MCUs

- On-chip in-circuit programmable FLASH memory with block protection and security options (see Table 1-1 for device specific information)
- On-chip random-access memory (RAM) (see Table 1-1 for device specific information)
- 8-channel, 10-bit analog-to-digital converter (ATD)
- Two serial communications interface modules (SCI)
- Serial peripheral interface module (SPI)

- Multiple clock source options:
  - Internally generated clock with ±0.2% trimming resolution and ±0.5% deviation across voltage.
  - Crystal
  - Resonator, or
  - External clock
- Inter-integrated circuit bus module to operate up to 100 kbps (IIC)
- One 3-channel and one 5-channel 16-bit timer/pulse width modulator (TPM) modules with selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels (TPMx).
- 8-pin keyboard interrupt module (KBI)
- 16 high-current pins (limited by package dissipation)
- Software selectable pullups on ports when used as input. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullup on $\overline{\text{RESET}}$ and IRQ pin to reduce customer system cost
- Up to 56 general-purpose input/output (I/O) pins, depending on package selection
- 64-pin low-profile quad flat package (LQFP) — MC9S08GBxx
- 48-pin quad flat package, no lead (QFN) — MC9S08GTxx
- 44-pin quad flat package (QFP) — MC9S08GTxx
- 42-pin shrink dual in-line package (SDIP) — MC9S08GTxx

1.2.3 Devices in the MC9S08GB/GT Series

Table 1-1 lists the devices available in the MC9S08GB/GT series and summarizes the differences among them.

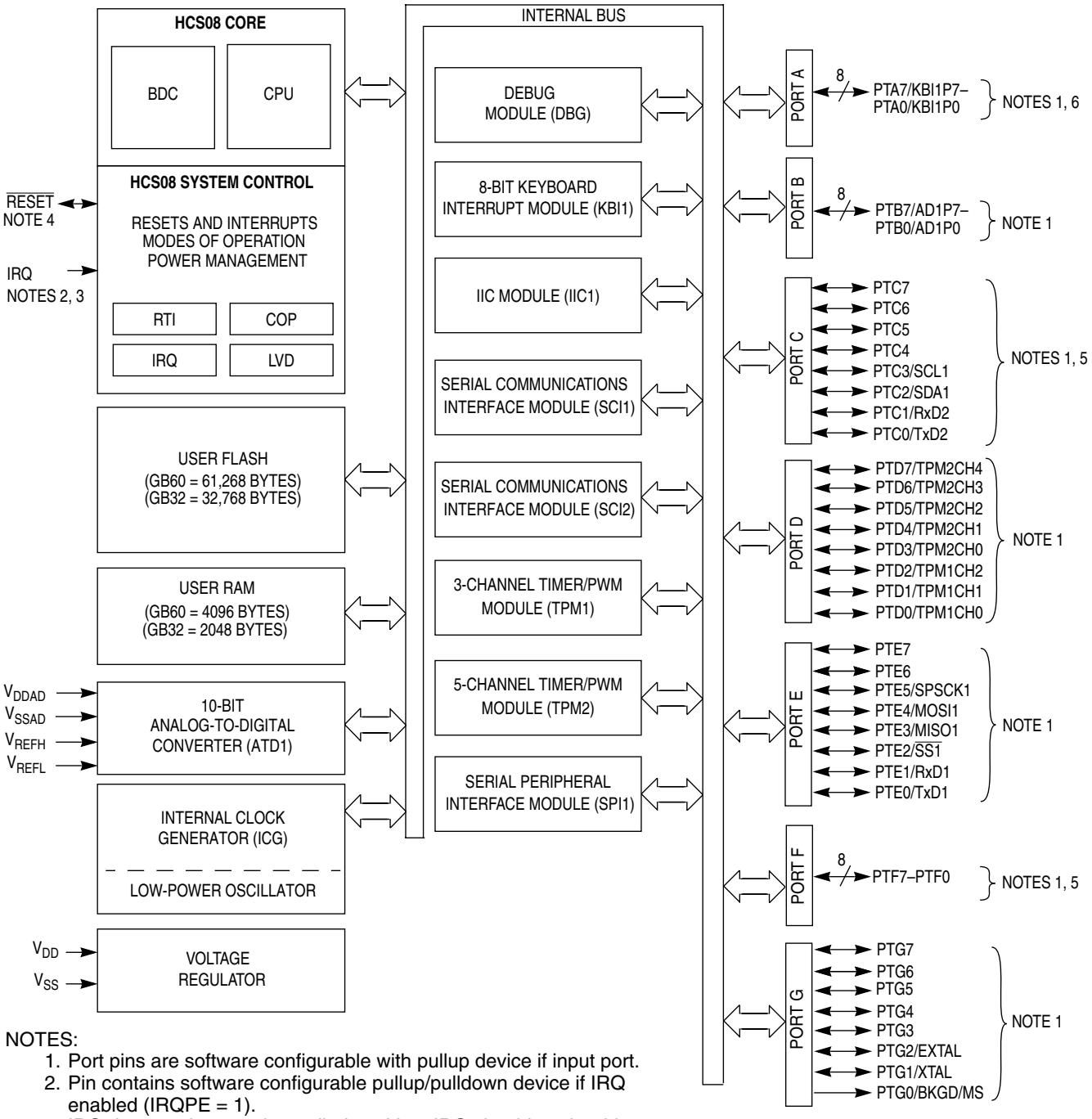
Table 1-1. Devices in the MC9S08GB/GT Series

Device	FLASH	RAM	TPM	I/O	Packages
MC9S08GB60	60K	4K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GB32	32K	2K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GT60	60K	4K	Two 2-channel, 16-bit timers	39 36 34	48 QFN[1] 44 QFP 42 SDIP
MC9S08GT32	32K	2K	Two 2-channel, 16-bit timers	39 36 34	48 QFN[(1)] 44 QFP 42 SDIP
MC9S08GT16	16K	1K	Two 2-channel, 16-bit timers	39 36 34	48 QFN[(1)] 44 QFP 42 SDIP

1 The 48-pin QFN package has one 3-channel and one 2-channel 16-bit TPM.

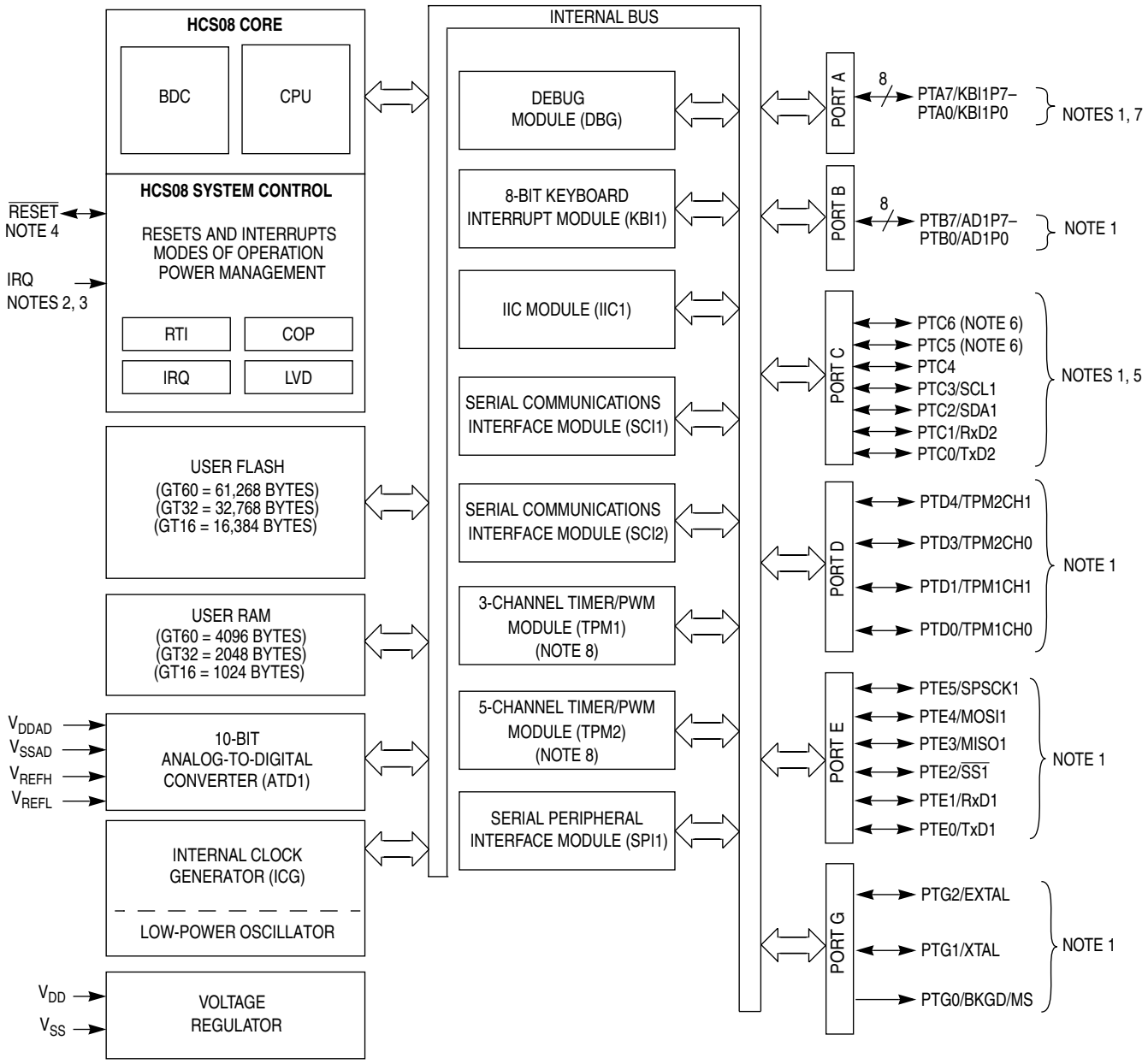
1.3 MCU Block Diagrams

These block diagrams show the structure of the MC9S08GB/GT MCUs.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1).
3. IRQ does not have a clamp diode to V_{DD}. IRQ should not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. High current drive
6. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown available when KBI enabled (KBIPn = 1).

Figure 1-1. MC9S08GBxx Block Diagram



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1).
3. IRQ does not have a clamp diode to V_{DD}. IRQ should not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. High current drive
6. PTC[6:5] are not available on the 42-pin SDIP package.
7. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown available when KBI enabled (KBIPn = 1).
8. Only two timer channels per TPM are bonded out. All channels are available for use as software compare.

Figure 1-2. MC9S08GTxx Block Diagram

Table 1-2 lists the functional versions of the on-chip modules.

Table 1-2. Block Versions

Module	Version
Analog-to-Digital Converter (ATD)	3
Internal Clock Generator (ICG)	2
Inter-Integrated Circuit (IIC)	1
Keyboard Interrupt (KBI)	1
Serial Communications Interface (SCI)	1
Serial Peripheral Interface (SPI)	3
Timer Pulse-Width Modulator (TPM)	1
Central Processing Unit (CPU)	2

1.4 System Clock Distribution

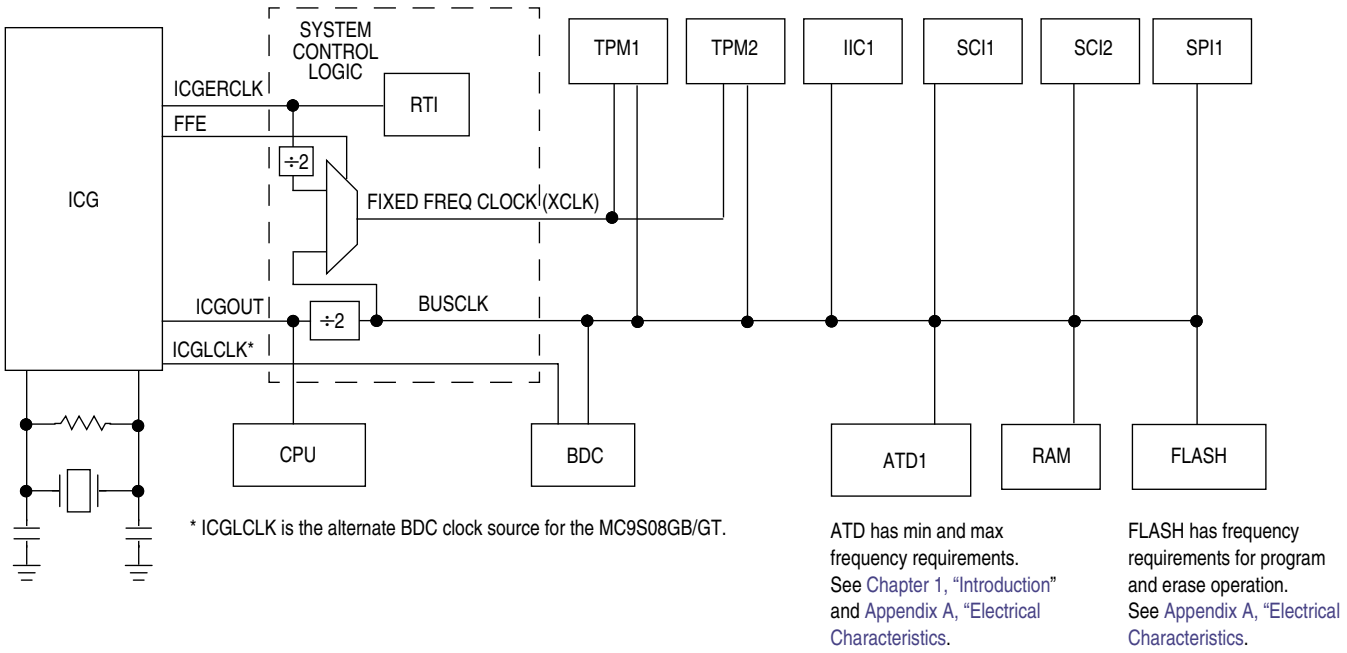


Figure 1-3. System Clock Distribution Diagram

Some of the modules inside the MCU have clock source choices. Figure 1-3 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
  - The external crystal oscillator
  - An external clock source
  - The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module

  Control bits inside the ICG determine which source is connected.

- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT > 4 × the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be the ICGERCLK. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source.

Chapter 2 Pins and Connections

2.1 Introduction

This section describes signals that connect to package pins. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals.

2.2 Device Pin Assignment

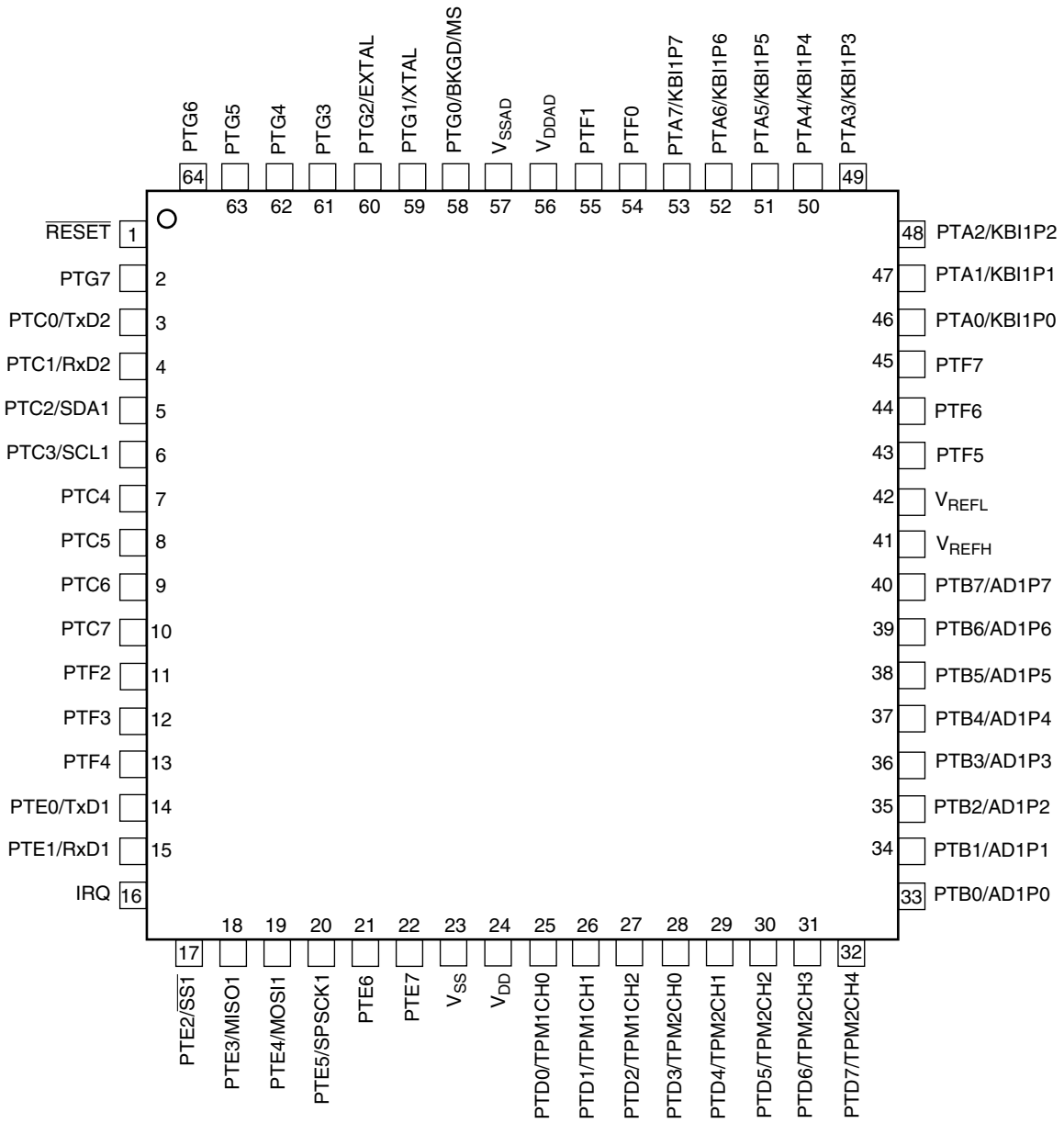


Figure 2-1. MC9S08GBxx in 64-Pin LQFP Package

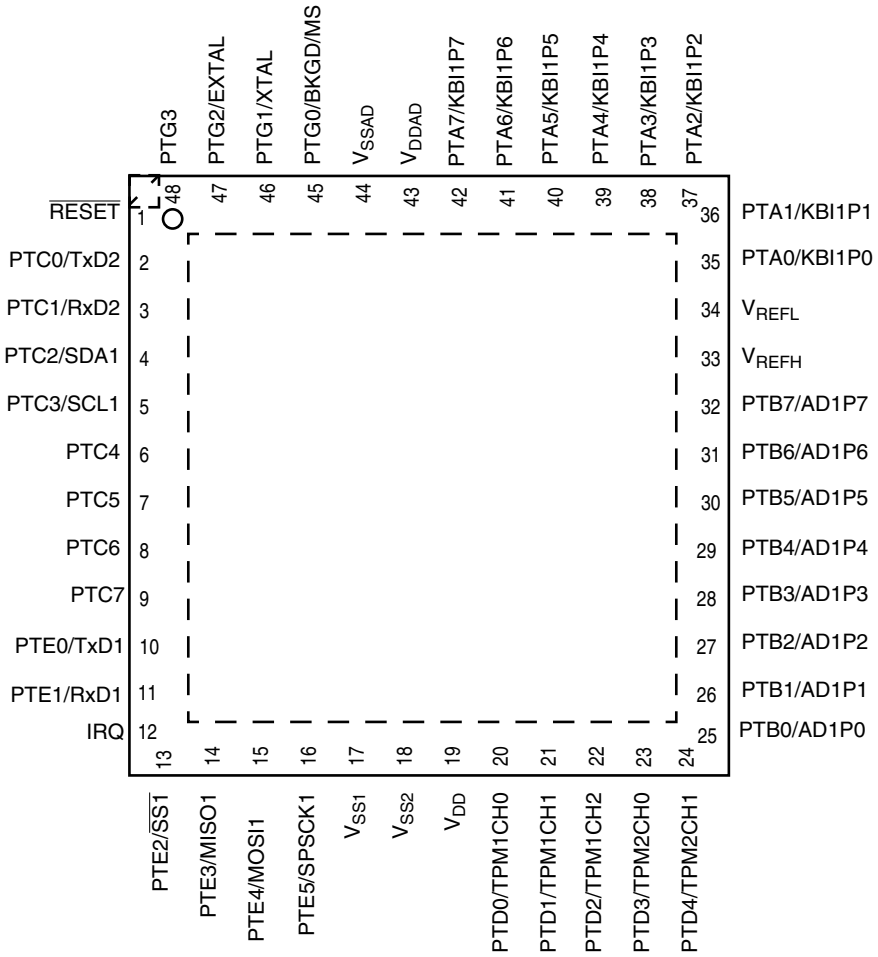


Figure 2-2. MC9S08GTxx in 48-Pin QFN Package

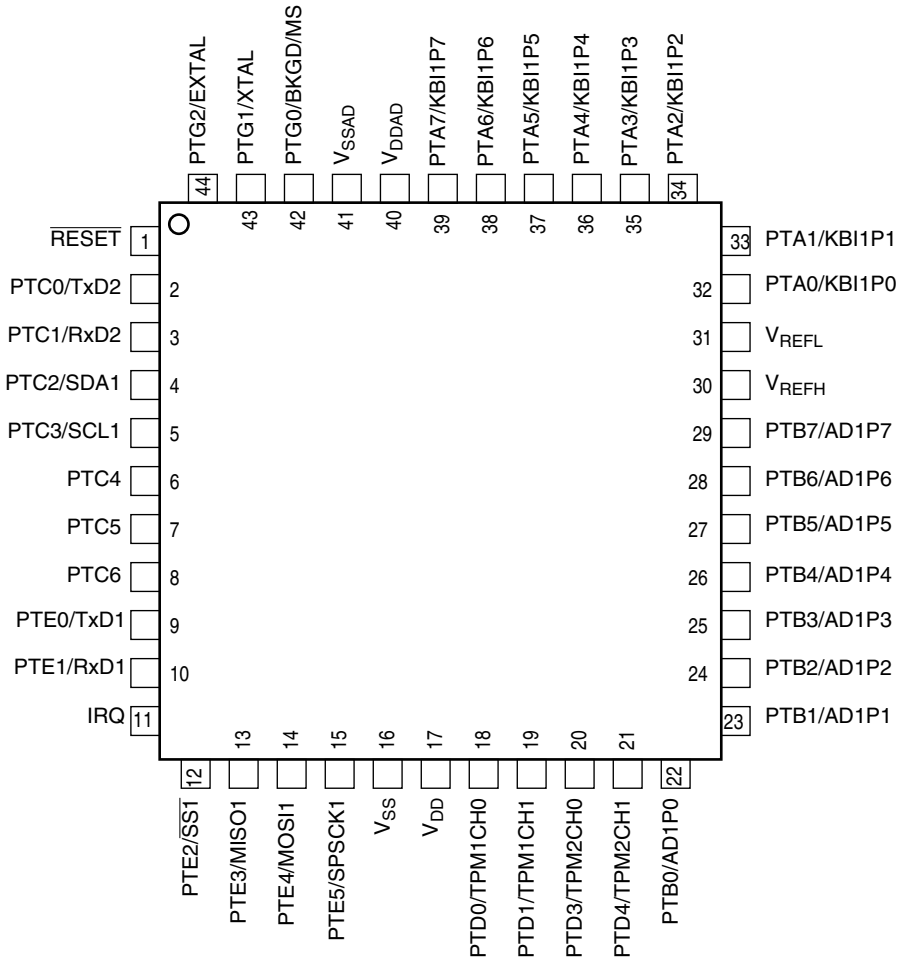


Figure 2-3. MC9S08GTxx in 44-Pin QFP Package