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**MC9S08GB60**

**MC9S08GB32**

**MC9S08GT60**

**MC9S08GT32**

**MC9S08GT16**

Data Sheet

***HCS08***  
***Microcontrollers***

MC9S08GB60/D  
Rev. 2.3  
12/2004

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# MC9S08GB/GT Data Sheet

Covers: MC9S08GB60  
MC9S08GB32  
MC9S08GT60  
MC9S08GT32  
MC9S08GT16

MC9S08GB60  
Rev. 2.3  
12/2004

# Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

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The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1.0	4/25/2003	Initial release
1.1		Electricals change, appendix A only
1.2		Electricals change, appendix A only
1.3	10/2/2003	Added module version table; clarifications
1.4	10/29/2003	Fixed typos and made corrections and clarifications
1.5	11/12/2003	Added 1-MHz I <sub>DD</sub> values to Electricals, appendix A
2	2/10/2004	Changed format of register names to enable reuse of code (from SCIBD to SCI1BD, even when only one instance of a module on a chip) Added new device: MC9S08GT16 to book. Added new 48-pin QFN package to book. BKGDPE description in Section 5 — changed PTD0 to PTG0. Changed typo in CPU section that listed MOV instruction as being 6 cycles instead of 5 (Table 8-2).
2.2	9/2/2004	Format to Freescale look-and-feel; Clarified RTI clock sources and other changes in Chapter 5; updated ICG initialization examples; expanded descriptions of LOLS and LOCS bits in ICGS1; updated ICG electricals Table A-9 and added a figure
2.3	12/01/2004	Minor changes to Table 7-4, Table 7-5, Table A-9; Clarifications in Section 11.10.6, “SCI x Control Register 3 (SCIxC3)”, Section 11.7, “Interrupts and Status Flags”, Section 11.8.1, “8- and 9-Bit Data Modes”, PTG availability in 48-pin package (see Table 2-2)

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# List of Chapters

Chapter 1	Introduction.....	17
Chapter 2	Pins and Connections .....	23
Chapter 3	Modes of Operation .....	33
Chapter 4	Memory .....	39
Chapter 5	Resets, Interrupts, and System Configuration .....	61
Chapter 6	Parallel Input/Output .....	77
Chapter 7	Internal Clock Generator (ICG) Module .....	97
Chapter 8	Central Processor Unit (CPU).....	125
Chapter 9	Keyboard Interrupt (KBI) Module .....	145
Chapter 10	Timer/PWM (TPM) Module.....	151
Chapter 11	Serial Communications Interface (SCI) Module.....	167
Chapter 12	Serial Peripheral Interface (SPI) Module.....	187
Chapter 13	Inter-Integrated Circuit (IIC) Module .....	203
Chapter 14	Analog-to-Digital Converter (ATD) Module .....	219
Chapter 15	Development Support .....	235
Appendix A	Electrical Characteristics.....	259
Appendix B	Ordering Information and Mechanical Drawings.....	281



# Contents

Section Number	Title	Page
<b>Chapter 1</b>		
<b>Introduction</b>		
1.1	Overview .....	17
1.2	Features .....	17
1.2.1	Standard Features of the HCS08 Family .....	17
1.2.2	Features of MC9S08GB/GT Series of MCUs .....	17
1.2.3	Devices in the MC9S08GB/GT Series .....	18
1.3	MCU Block Diagrams .....	19
1.4	System Clock Distribution .....	21
<b>Chapter 2</b>		
<b>Pins and Connections</b>		
2.1	Introduction .....	23
2.2	Device Pin Assignment .....	23
2.3	Recommended System Connections .....	26
2.3.1	Power .....	28
2.3.2	Oscillator .....	28
2.3.3	Reset .....	28
2.3.4	Background / Mode Select (PTG0/BKGD/MS) .....	29
2.3.5	General-Purpose I/O and Peripheral Ports .....	29
2.3.6	Signal Properties Summary .....	31
<b>Chapter 3</b>		
<b>Modes of Operation</b>		
3.1	Introduction .....	33
3.2	Features .....	33
3.3	Run Mode .....	33
3.4	Active Background Mode .....	33
3.5	Wait Mode .....	34
3.6	Stop Modes .....	34
3.6.1	Stop1 Mode .....	35
3.6.2	Stop2 Mode .....	35
3.6.3	Stop3 Mode .....	36
3.6.4	Active BDM Enabled in Stop Mode .....	36
3.6.5	LVD Enabled in Stop Mode .....	37
3.6.6	On-Chip Peripheral Modules in Stop Modes .....	37



Section Number	Title	Page
<b>Chapter 4</b>		
<b>Memory</b>		
4.1	MC9S08GB/GT Memory Map .....	39
4.1.1	Reset and Interrupt Vector Assignments .....	39
4.2	Register Addresses and Bit Assignments .....	41
4.3	RAM .....	46
4.4	FLASH .....	46
4.4.1	Features .....	47
4.4.2	Program and Erase Times .....	47
4.4.3	Program and Erase Command Execution .....	48
4.4.4	Burst Program Execution .....	49
4.4.5	Access Errors .....	50
4.4.6	FLASH Block Protection .....	51
4.4.7	Vector Redirection .....	52
4.5	Security .....	52
4.6	FLASH Registers and Control Bits .....	53
4.6.1	FLASH Clock Divider Register (FCDIV) .....	54
4.6.2	FLASH Options Register (FOPT and NVOPT) .....	55
4.6.3	FLASH Configuration Register (FCNFG) .....	56
4.6.4	FLASH Protection Register (FPROT and NVPROT) .....	56
4.6.5	FLASH Status Register (FSTAT) .....	58
4.6.6	FLASH Command Register (FCMD) .....	59
<b>Chapter 5</b>		
<b>Resets, Interrupts, and System Configuration</b>		
5.1	Introduction .....	61
5.2	Features .....	61
5.3	MCU Reset .....	61
5.4	Computer Operating Properly (COP) Watchdog .....	62
5.5	Interrupts .....	62
5.5.1	Interrupt Stack Frame .....	63
5.5.2	External Interrupt Request (IRQ) Pin .....	64
5.5.2.1	Pin Configuration Options .....	64
5.5.2.2	Edge and Level Sensitivity .....	65
5.5.3	Interrupt Vectors, Sources, and Local Masks .....	65
5.6	Low-Voltage Detect (LVD) System .....	67
5.6.1	Power-On Reset Operation .....	67
5.6.2	LVD Reset Operation .....	67
5.6.3	LVD Interrupt Operation .....	67
5.6.4	Low-Voltage Warning (LVW) .....	67
5.7	Real-Time Interrupt (RTI) .....	67

Section Number	Title	Page
5.8	Reset, Interrupt, and System Control Registers and Control Bits .....	68
5.8.1	Interrupt Pin Request Status and Control Register (IRQSC) .....	68
5.8.2	System Reset Status Register (SRS) .....	69
5.8.3	System Background Debug Force Reset Register (SBDFFR) .....	71
5.8.4	System Options Register (SOPT) .....	71
5.8.5	System Device Identification Register (SDIDH, SDIDL) .....	72
5.8.6	System Real-Time Interrupt Status and Control Register (SRTISC) .....	73
5.8.7	System Power Management Status and Control 1 Register (SPMSC1) .....	74
5.8.8	System Power Management Status and Control 2 Register (SPMSC2) .....	75

## Chapter 6 Parallel Input/Output

6.1	Introduction .....	77
6.2	Features .....	79
6.3	Pin Descriptions .....	79
6.3.1	Port A and Keyboard Interrupts .....	79
6.3.2	Port B and Analog to Digital Converter Inputs .....	80
6.3.3	Port C and SCI2, IIC, and High-Current Drivers .....	80
6.3.4	Port D, TPM1 and TPM2 .....	81
6.3.5	Port E, SCI1, and SPI .....	81
6.3.6	Port F and High-Current Drivers .....	82
6.3.7	Port G, BKGD/MS, and Oscillator .....	82
6.4	Parallel I/O Controls .....	82
6.4.1	Data Direction Control .....	83
6.4.2	Internal Pullup Control .....	83
6.4.3	Slew Rate Control .....	83
6.5	Stop Modes .....	84
6.6	Parallel I/O Registers and Control Bits .....	84
6.6.1	Port A Registers (PTAD, PTAPE, PTASE, and PTADD) .....	84
6.6.2	Port B Registers (PTBD, PTBPE, PTBSE, and PTBDD) .....	86
6.6.3	Port C Registers (PTCD, PTCPE, PTCSE, and PTCDD) .....	87
6.6.4	Port D Registers (PTDD, PTDPE, PTDSE, and PTDDD) .....	89
6.6.5	Port E Registers (PTED, PTEPE, PTESE, and PTEDD) .....	90
6.6.6	Port F Registers (PTFD, PTFPE, PTFSE, and PTFDD) .....	92
6.6.7	Port G Registers (PTGD, PTGPE, PTGSE, and PTGDD) .....	93

Section Number	Title	Page
<b>Chapter 7</b>		
<b>Internal Clock Generator (ICG) Module</b>		
7.1	Introduction .....	99
7.1.1	Features .....	100
7.1.2	Modes of Operation .....	101
7.2	External Signal Description .....	101
7.2.1	Overview .....	101
7.2.2	Detailed Signal Descriptions .....	102
7.2.2.1	EXTAL— External Reference Clock / Oscillator Input .....	102
7.2.2.2	XTAL— Oscillator Output .....	102
7.2.3	External Clock Connections .....	102
7.2.4	External Crystal/Resonator Connections .....	102
7.3	Functional Description .....	103
7.3.1	Off Mode (Off) .....	103
7.3.1.1	BDM Active .....	103
7.3.1.2	OS CSTEN Bit Set .....	103
7.3.1.3	Stop/Off Mode Recovery .....	104
7.3.2	Self-Clocked Mode (SCM) .....	104
7.3.3	FLL Engaged, Internal Clock (FEI) Mode .....	105
7.3.3.1	FLL Engaged Internal Unlocked .....	105
7.3.3.2	FLL Engaged Internal Locked .....	106
7.3.4	FLL Bypassed, External Clock (FBE) Mode .....	106
7.3.5	FLL Engaged, External Clock (FEE) Mode .....	106
7.3.5.1	FLL Engaged External Unlocked .....	106
7.3.5.2	FLL Engaged External Locked .....	107
7.3.6	FLL Lock and Loss-of-Lock Detection .....	107
7.3.7	FLL Loss-of-Clock Detection .....	107
7.3.8	Clock Mode Requirements .....	108
7.3.9	Fixed Frequency Clock .....	109
7.4	Initialization/Application Information .....	110
7.4.1	Introduction .....	110
7.4.2	Example #1: External Crystal = 32 kHz, Bus Frequency = 4.19 MHz .....	112
7.4.3	Example #2: External Crystal = 4 MHz, Bus Frequency = 20 MHz .....	113
7.4.4	Example #3: No External Crystal Connection, 5.4 MHz Bus Frequency .....	114
7.4.5	Example #4: Internal Clock Generator Trim .....	116
7.5	ICG Registers and Control Bits .....	117
7.5.1	ICG Control Register 1 (ICGC1) .....	118
7.5.2	ICG Control Register 2 (ICGC2) .....	119
7.5.3	ICG Status Register 1 (ICGS1) .....	120
7.5.4	ICG Status Register 2 (ICGS2) .....	122
7.5.5	ICG Filter Registers (ICGFLTU, ICGFLTL) .....	122
7.5.6	ICG Trim Register (ICGTRM) .....	123

Section Number	Title	Page
<b>Chapter 8</b>		
<b>Central Processor Unit (CPU)</b>		
8.1	Introduction .....	125
8.2	Features .....	126
8.3	Programmer's Model and CPU Registers .....	126
8.3.1	Accumulator (A) .....	127
8.3.2	Index Register (H:X) .....	127
8.3.3	Stack Pointer (SP) .....	128
8.3.4	Program Counter (PC) .....	128
8.3.5	Condition Code Register (CCR) .....	128
8.4	Addressing Modes .....	130
8.4.1	Inherent Addressing Mode (INH) .....	130
8.4.2	Relative Addressing Mode (REL) .....	130
8.4.3	Immediate Addressing Mode (IMM) .....	130
8.4.4	Direct Addressing Mode (DIR) .....	130
8.4.5	Extended Addressing Mode (EXT) .....	131
8.4.6	Indexed Addressing Mode .....	131
8.4.6.1	Indexed, No Offset (IX) .....	131
8.4.6.2	Indexed, No Offset with Post Increment (IX+) .....	131
8.4.6.3	Indexed, 8-Bit Offset (IX1) .....	131
8.4.6.4	Indexed, 8-Bit Offset with Post Increment (IX1+) .....	131
8.4.6.5	Indexed, 16-Bit Offset (IX2) .....	131
8.4.6.6	SP-Relative, 8-Bit Offset (SP1) .....	131
8.4.6.7	SP-Relative, 16-Bit Offset (SP2) .....	132
8.5	Special Operations .....	132
8.5.1	Reset Sequence .....	132
8.5.2	Interrupt Sequence .....	132
8.5.3	Wait Mode Operation .....	133
8.5.4	Stop Mode Operation .....	133
8.5.5	BGND Instruction .....	134
8.6	HCS08 Instruction Set Summary .....	134
<b>Chapter 9</b>		
<b>Keyboard Interrupt (KBI) Module</b>		
9.1	Introduction .....	145
9.1.1	Port A and Keyboard Interrupt Pins .....	145
9.2	Features .....	145
9.3	KBI Block Diagram .....	147
9.4	Keyboard Interrupt (KBI) Module .....	147
9.4.1	Pin Enables .....	147
9.4.2	Edge and Level Sensitivity .....	147
9.4.3	KBI Interrupt Controls .....	148
9.5	KBI Registers and Control Bits .....	148
9.5.1	KBI Status and Control Register (KBI1SC) .....	148
9.5.2	KBI Pin Enable Register (KBI1PE) .....	150

Section Number	Title	Page
<b>Chapter 10</b>		
<b>Timer/PWM (TPM) Module</b>		
10.1	Introduction .....	151
10.2	Features .....	151
10.3	TPM Block Diagram .....	153
10.4	Pin Descriptions .....	154
10.4.1	External TPM Clock Sources .....	154
10.4.2	TPM <sub>x</sub> CH <sub>n</sub> — TPM <sub>x</sub> Channel n I/O Pins .....	154
10.5	Functional Description .....	154
10.5.1	Counter .....	155
10.5.2	Channel Mode Selection .....	156
10.5.2.1	Input Capture Mode .....	156
10.5.2.2	Output Compare Mode .....	156
10.5.2.3	Edge-Aligned PWM Mode .....	156
10.5.3	Center-Aligned PWM Mode .....	157
10.6	TPM Interrupts .....	159
10.6.1	Clearing Timer Interrupt Flags .....	159
10.6.2	Timer Overflow Interrupt Description .....	159
10.6.3	Channel Event Interrupt Description .....	159
10.6.4	PWM End-of-Duty-Cycle Events .....	160
10.7	TPM Registers and Control Bits .....	160
10.7.1	Timer x Status and Control Register (TPM <sub>x</sub> SC) .....	160
10.7.2	Timer x Counter Registers (TPM <sub>x</sub> CNTH:TPM <sub>x</sub> CNTL) .....	162
10.7.3	Timer x Counter Modulo Registers (TPM <sub>x</sub> MODH:TPM <sub>x</sub> MODL) .....	163
10.7.4	Timer x Channel n Status and Control Register (TPM <sub>x</sub> CnSC) .....	163
10.7.5	Timer x Channel Value Registers (TPM <sub>x</sub> CnVH:TPM <sub>x</sub> CnVL) .....	165
<b>Chapter 11</b>		
<b>Serial Communications Interface (SCI) Module</b>		
11.1	Introduction .....	167
11.2	Features .....	169
11.3	SCI System Description .....	169
11.4	Baud Rate Generation .....	169
11.5	Transmitter Functional Description .....	170
11.5.1	Transmitter Block Diagram .....	170
11.5.2	Send Break and Queued Idle .....	172
11.6	Receiver Functional Description .....	172
11.6.1	Receiver Block Diagram .....	172
11.6.2	Data Sampling Technique .....	174
11.6.3	Receiver Wakeup Operation .....	174
11.6.3.1	Idle-Line Wakeup .....	175
11.6.3.2	Address-Mark Wakeup .....	175
11.7	Interrupts and Status Flags .....	175

Section Number	Title	Page
11.8	Additional SCI Functions .....	176
11.8.1	8- and 9-Bit Data Modes .....	176
11.9	Stop Mode Operation .....	176
11.9.1	Loop Mode .....	177
11.9.2	Single-Wire Operation .....	177
11.10	SCI Registers and Control Bits .....	177
11.10.1	SCI x Baud Rate Registers (SCIxBDH, SCIxBDL) .....	177
11.10.2	SCI x Control Register 1 (SCIxC1) .....	178
11.10.3	SCI x Control Register 2 (SCIxC2) .....	180
11.10.4	SCI x Status Register 1 (SCIxS1) .....	181
11.10.5	SCI x Status Register 2 (SCIxS2) .....	183
11.10.6	SCI x Control Register 3 (SCIxC3) .....	184
11.10.7	SCI x Data Register (SCIxD) .....	185

## Chapter 12

### Serial Peripheral Interface (SPI) Module

12.1	Features .....	189
12.2	Block Diagrams .....	189
12.2.1	SPI System Block Diagram .....	189
12.2.2	SPI Module Block Diagram .....	190
12.2.3	SPI Baud Rate Generation .....	192
12.3	Functional Description .....	192
12.3.1	SPI Clock Formats .....	193
12.3.2	SPI Pin Controls .....	195
12.3.2.1	SPSCK1 — SPI Serial Clock .....	195
12.3.2.2	MOSI1 — Master Data Out, Slave Data In .....	195
12.3.2.3	MISO1 — Master Data In, Slave Data Out .....	195
12.3.2.4	$\overline{SS1}$ — Slave Select .....	195
12.3.3	SPI Interrupts .....	196
12.3.4	Mode Fault Detection .....	196
12.4	SPI Registers and Control Bits .....	196
12.4.1	SPI Control Register 1 (SPI1C1) .....	197
12.4.2	SPI Control Register 2 (SPI1C2) .....	198
12.4.3	SPI Baud Rate Register (SPI1BR) .....	199
12.4.4	SPI Status Register (SPI1S) .....	201
12.4.5	SPI Data Register (SPI1D) .....	202

Section Number	Title	Page
<b>Chapter 13</b>		
<b>Inter-Integrated Circuit (IIC) Module</b>		
13.1	Introduction .....	205
13.1.1	Features .....	205
13.1.2	Modes of Operation .....	205
13.1.3	Block Diagram .....	206
13.1.4	Detailed Signal Descriptions .....	206
13.1.4.1	SCL1 — Serial Clock Line .....	206
13.1.4.2	SDA1 — Serial Data Line .....	206
13.2	Functional Description .....	207
13.2.1	IIC Protocol .....	207
13.2.1.1	START Signal .....	208
13.2.1.2	Slave Address Transmission .....	208
13.2.1.3	Data Transfer .....	208
13.2.1.4	STOP Signal .....	209
13.2.1.5	Repeated START Signal .....	209
13.2.1.6	Arbitration Procedure .....	209
13.2.1.7	Clock Synchronization .....	209
13.2.1.8	Handshaking .....	210
13.2.1.9	Clock Stretching .....	210
13.3	Resets .....	210
13.4	Interrupts .....	211
13.4.1	Byte Transfer Interrupt .....	211
13.4.2	Address Detect Interrupt .....	211
13.4.3	Arbitration Lost Interrupt .....	211
13.5	IIC Registers and Control Bits .....	212
13.5.1	IIC Address Register (IIC1A) .....	212
13.5.2	IIC Frequency Divider Register (IIC1F) .....	212
13.5.3	IIC Control Register (IIC1C) .....	215
13.5.4	IIC Status Register (IIC1S) .....	216
13.5.5	IIC Data I/O Register (IIC1D) .....	217
<b>Chapter 14</b>		
<b>Analog-to-Digital Converter (ATD) Module</b>		
14.1	Introduction .....	221
14.1.1	Features .....	221
14.1.2	Modes of Operation .....	221
14.1.2.1	Stop Mode .....	221
14.1.2.2	Power Down Mode .....	221
14.1.3	Block Diagram .....	221
14.2	Signal Description .....	222
14.2.1	Overview .....	222
14.2.1.1	Channel Input Pins — AD1P7–AD1P0 .....	223

Section Number	Title	Page
14.2.1.2	ATD Reference Pins — $V_{REFH}$ , $V_{REFL}$ .....	223
14.2.1.3	ATD Supply Pins — $V_{DDAD}$ , $V_{SSAD}$ .....	223
14.3	Functional Description .....	223
14.3.1	Mode Control .....	223
14.3.2	Sample and Hold .....	224
14.3.3	Analog Input Multiplexer .....	226
14.3.4	ATD Module Accuracy Definitions .....	226
14.4	Resets .....	229
14.5	Interrupts .....	229
14.6	ATD Registers and Control Bits .....	229
14.6.1	ATD Control (ATDC) .....	230
14.6.2	ATD Status and Control (ATD1SC) .....	232
14.6.3	ATD Result Data (ATD1RH, ATD1RL) .....	234
14.6.4	ATD Pin Enable (ATD1PE) .....	234

## Chapter 15 Development Support

15.1	Introduction .....	235
15.2	Features .....	236
15.3	Background Debug Controller (BDC) .....	237
15.3.1	BKGD Pin Description .....	237
15.3.2	Communication Details .....	238
15.3.3	BDC Commands .....	242
15.3.4	BDC Hardware Breakpoint .....	244
15.4	On-Chip Debug System (DBG) .....	245
15.4.1	Comparators A and B .....	245
15.4.2	Bus Capture Information and FIFO Operation .....	245
15.4.3	Change-of-Flow Information .....	246
15.4.4	Tag vs. Force Breakpoints and Triggers .....	246
15.4.5	Trigger Modes .....	247
15.4.6	Hardware Breakpoints .....	249
15.5	Registers and Control Bits .....	249
15.5.1	BDC Registers and Control Bits .....	249
15.5.1.1	BDC Status and Control Register (BDCSCR) .....	250
15.5.1.2	BDC Breakpoint Match Register (BDCBKPT) .....	251
15.5.2	System Background Debug Force Reset Register (SBDFR) .....	251
15.5.3	DBG Registers and Control Bits .....	252
15.5.3.1	Debug Comparator A High Register (DBGCAH) .....	252
15.5.3.2	Debug Comparator A Low Register (DBGCAL) .....	252
15.5.3.3	Debug Comparator B High Register (DBGCBH) .....	252
15.5.3.4	Debug Comparator B Low Register (DBGCBL) .....	252



Section Number	Title	Page
15.5.3.5	Debug FIFO High Register (DBGFH) .....	253
15.5.3.6	Debug FIFO Low Register (DBGFL) .....	253
15.5.3.7	Debug Control Register (DBGC) .....	254
15.5.3.8	Debug Trigger Register (DBGT) .....	255
15.5.3.9	Debug Status Register (DBGS) .....	256

## Appendix A Electrical Characteristics

A.1	Introduction .....	259
A.2	Absolute Maximum Ratings .....	259
A.3	Thermal Characteristics .....	260
A.4	Electrostatic Discharge (ESD) Protection Characteristics .....	261
A.5	DC Characteristics .....	261
A.6	Supply Current Characteristics .....	265
A.7	ATD Characteristics .....	269
A.8	Internal Clock Generation Module Characteristics .....	271
A.8.1	ICG Frequency Specifications .....	271
A.9	AC Characteristics .....	273
A.9.1	Control Timing .....	273
A.9.2	Timer/PWM (TPM) Module Timing .....	274
A.9.3	SPI Timing .....	275
A.10	FLASH Specifications .....	279

## Appendix B Ordering Information and Mechanical Drawings

B.1	Ordering Information .....	281
B.2	Mechanical Drawings .....	281
B.3	64-Pin LQFP Package Drawing .....	282
B.4	48-Pin QFN Package Drawing .....	283
B.5	44-Pin QFP Package Drawing .....	284
B.6	42-Pin SDIP Package Drawing .....	285

# Chapter 1 Introduction

## 1.1 Overview

The MC9S08GB/GT are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

## 1.2 Features

Features have been organized to reflect:

- Standard features of the HCS08 Family
- Features of the MC9S08GB/GT MCU

### 1.2.1 Standard Features of the HCS08 Family

- 40-MHz HCS08 CPU (central processor unit)
- HC08 instruction set with added BGND instruction
- Background debugging system (see also [Chapter 15, “Development Support”](#))
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources
- Power-saving modes: wait plus three stops
- System protection features:
  - Optional computer operating properly (COP) reset
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset (some devices don't have illegal addresses)

### 1.2.2 Features of MC9S08GB/GT Series of MCUs

- On-chip in-circuit programmable FLASH memory with block protection and security options (see [Table 1-1](#) for device specific information)
- On-chip random-access memory (RAM) (see [Table 1-1](#) for device specific information)
- 8-channel, 10-bit analog-to-digital converter (ATD)
- Two serial communications interface modules (SCI)
- Serial peripheral interface module (SPI)

- Multiple clock source options:
  - Internally generated clock with  $\pm 0.2\%$  trimming resolution and  $\pm 0.5\%$  deviation across voltage.
  - Crystal
  - Resonator, or
  - External clock
- Inter-integrated circuit bus module to operate up to 100 kbps (IIC)
- One 3-channel and one 5-channel 16-bit timer/pulse width modulator (TPM) modules with selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels (TPMx).
- 8-pin keyboard interrupt module (KBI)
- 16 high-current pins (limited by package dissipation)
- Software selectable pullups on ports when used as input. Selection is on an individual port bit basis. During output mode, pullups are disengaged.
- Internal pullup on  $\overline{\text{RESET}}$  and IRQ pin to reduce customer system cost
- Up to 56 general-purpose input/output (I/O) pins, depending on package selection
- 64-pin low-profile quad flat package (LQFP) — MC9S08GBxx
- 48-pin quad flat package, no lead (QFN) — MC9S08GTxx
- 44-pin quad flat package (QFP) — MC9S08GTxx
- 42-pin shrink dual in-line package (SDIP) — MC9S08GTxx

### 1.2.3 Devices in the MC9S08GB/GT Series

Table 1-1 lists the devices available in the MC9S08GB/GT series and summarizes the differences among them.

**Table 1-1. Devices in the MC9S08GB/GT Series**

Device	FLASH	RAM	TPM	I/O	Packages
MC9S08GB60	60K	4K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GB32	32K	2K	One 3-channel and one 5-channel, 16-bit timer	56	64 LQFP
MC9S08GT60	60K	4K	Two 2-channel, 16-bit timers	39 36 34	48 QFN <sup>1</sup> 44 QFP 42 SDIP
MC9S08GT32	32K	2K	Two 2-channel, 16-bit timers	39 36 34	48 QFN <sup>(1)</sup> 44 QFP 42 SDIP
MC9S08GT16	16K	1K	Two 2-channel, 16-bit timers	39 36 34	48 QFN <sup>(1)</sup> 44 QFP 42 SDIP

<sup>1</sup> The 48-pin QFN package has one 3-channel and one 2-channel 16-bit TPM.

## 1.3 MCU Block Diagrams

These block diagrams show the structure of the MC9S08GB/GT MCUs.

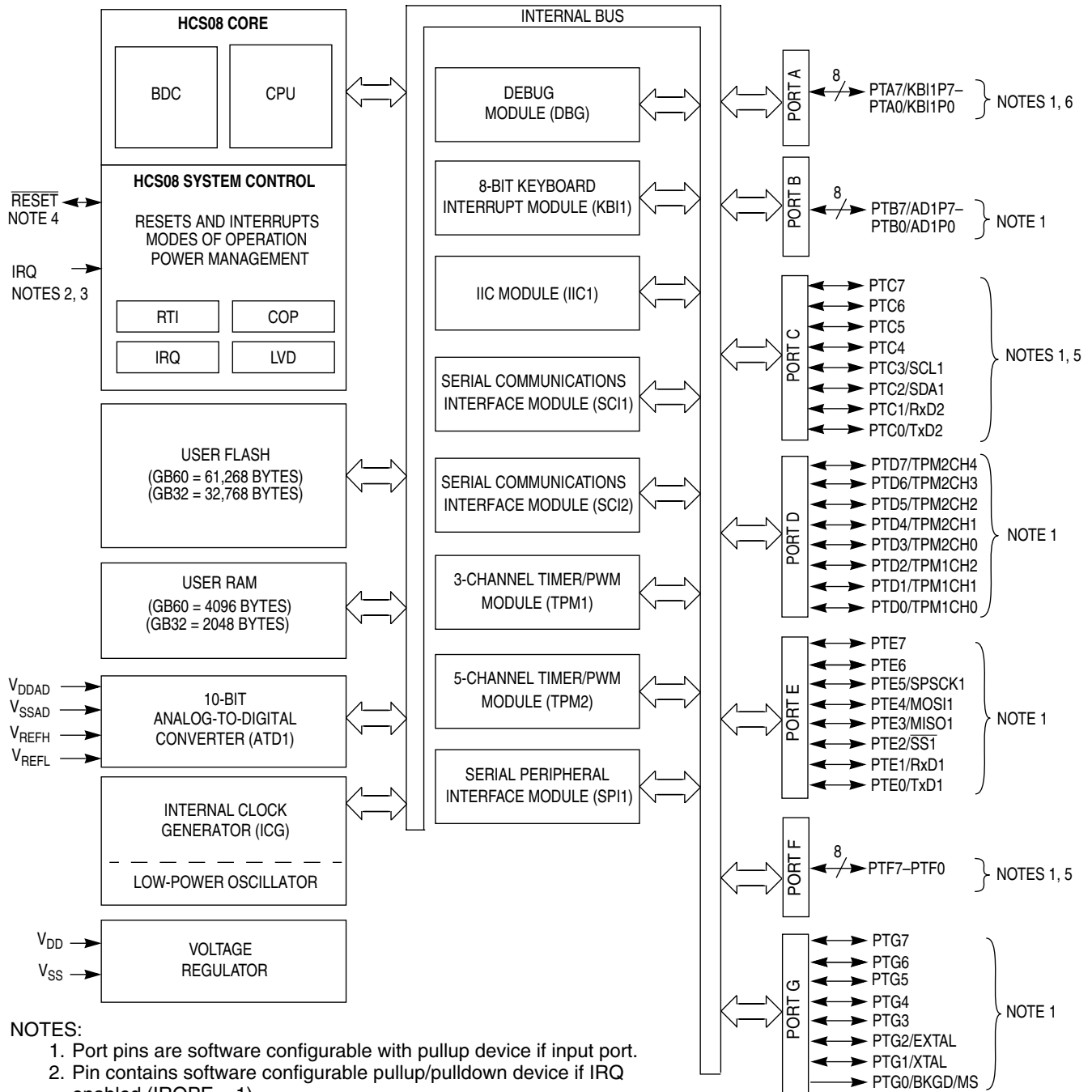
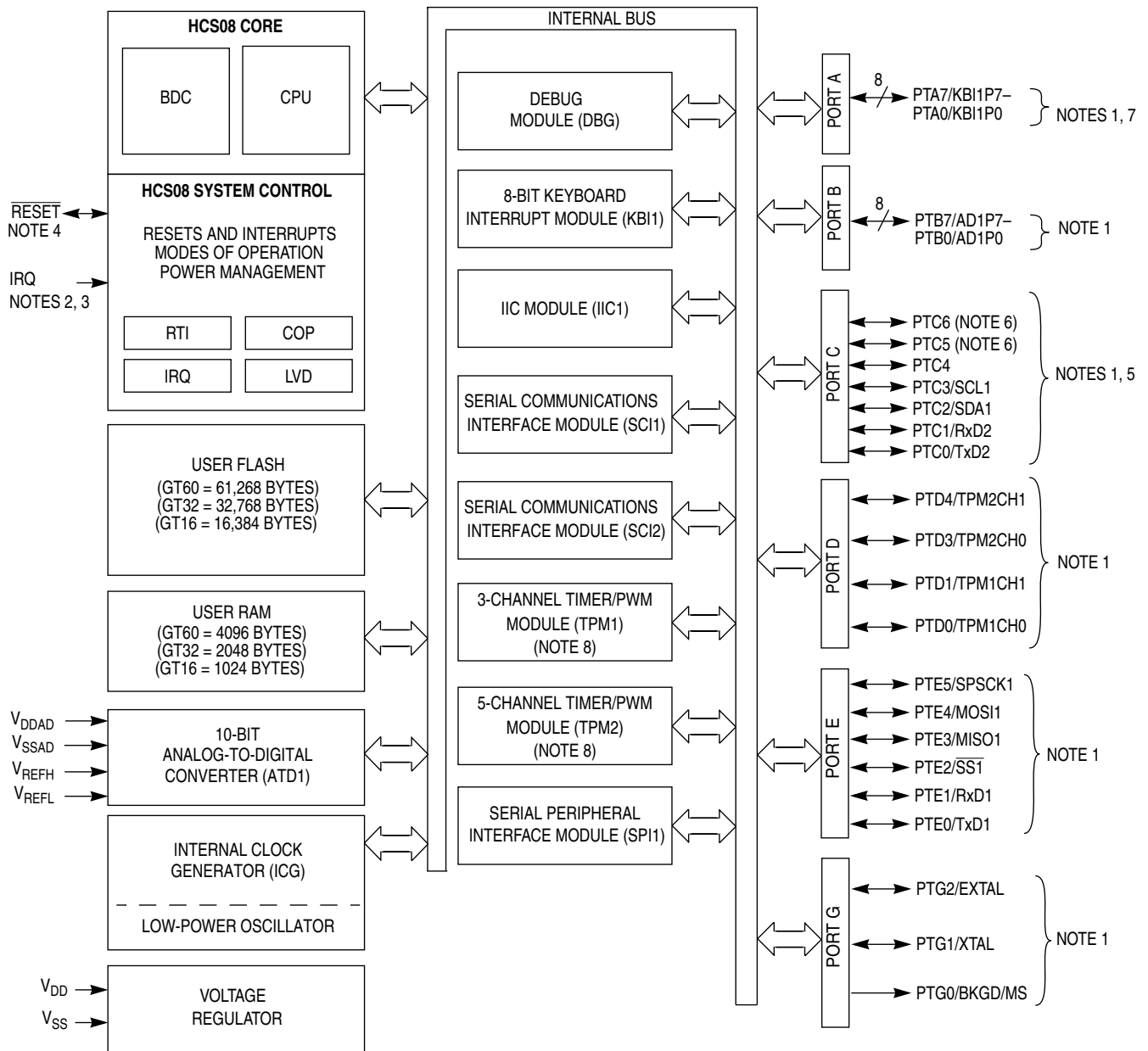


Figure 1-1. MC9S08GBxx Block Diagram



NOTES:

1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1).
3. IRQ does not have a clamp diode to V<sub>DD</sub>. IRQ should not be driven above V<sub>DD</sub>.
4. Pin contains integrated pullup device.
5. High current drive
6. PTC[6:5] are not available on the 42-pin SDIP package.
7. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown available when KBI enabled (KBIPn = 1).
8. Only two timer channels per TPM are bonded out. All channels are available for use as software compare.

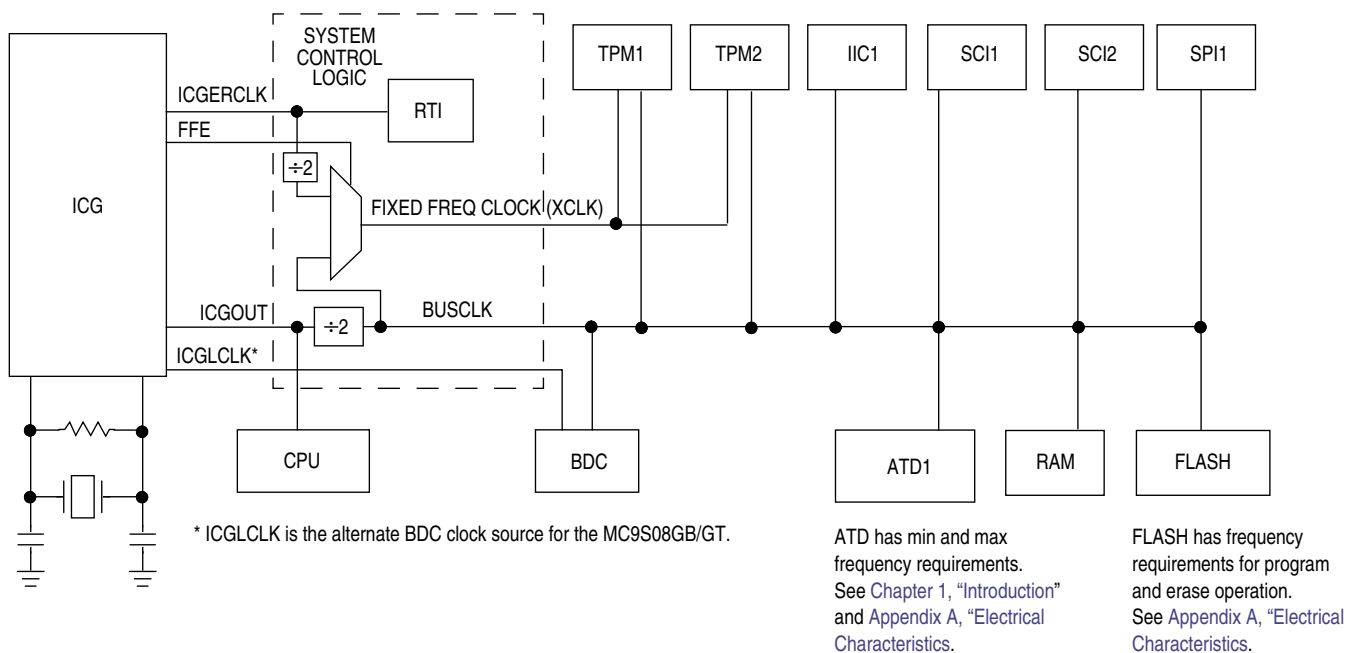
Figure 1-2. MC9S08GTxx Block Diagram

Table 1-2 lists the functional versions of the on-chip modules.

**Table 1-2. Block Versions**

Module	Version
Analog-to-Digital Converter (ATD)	3
Internal Clock Generator (ICG)	2
Inter-Integrated Circuit (IIC)	1
Keyboard Interrupt (KBI)	1
Serial Communications Interface (SCI)	1
Serial Peripheral Interface (SPI)	3
Timer Pulse-Width Modulator (TPM)	1
Central Processing Unit (CPU)	2

## 1.4 System Clock Distribution



**Figure 1-3. System Clock Distribution Diagram**

Some of the modules inside the MCU have clock source choices. Figure 1-3 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
  - The external crystal oscillator
  - An external clock source
  - The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module

Control bits inside the ICG determine which source is connected.

- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT  $> 4 \times$  the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be the ICGERCLK. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source.

# Chapter 2 Pins and Connections

## 2.1 Introduction

This section describes signals that connect to package pins. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals.

## 2.2 Device Pin Assignment

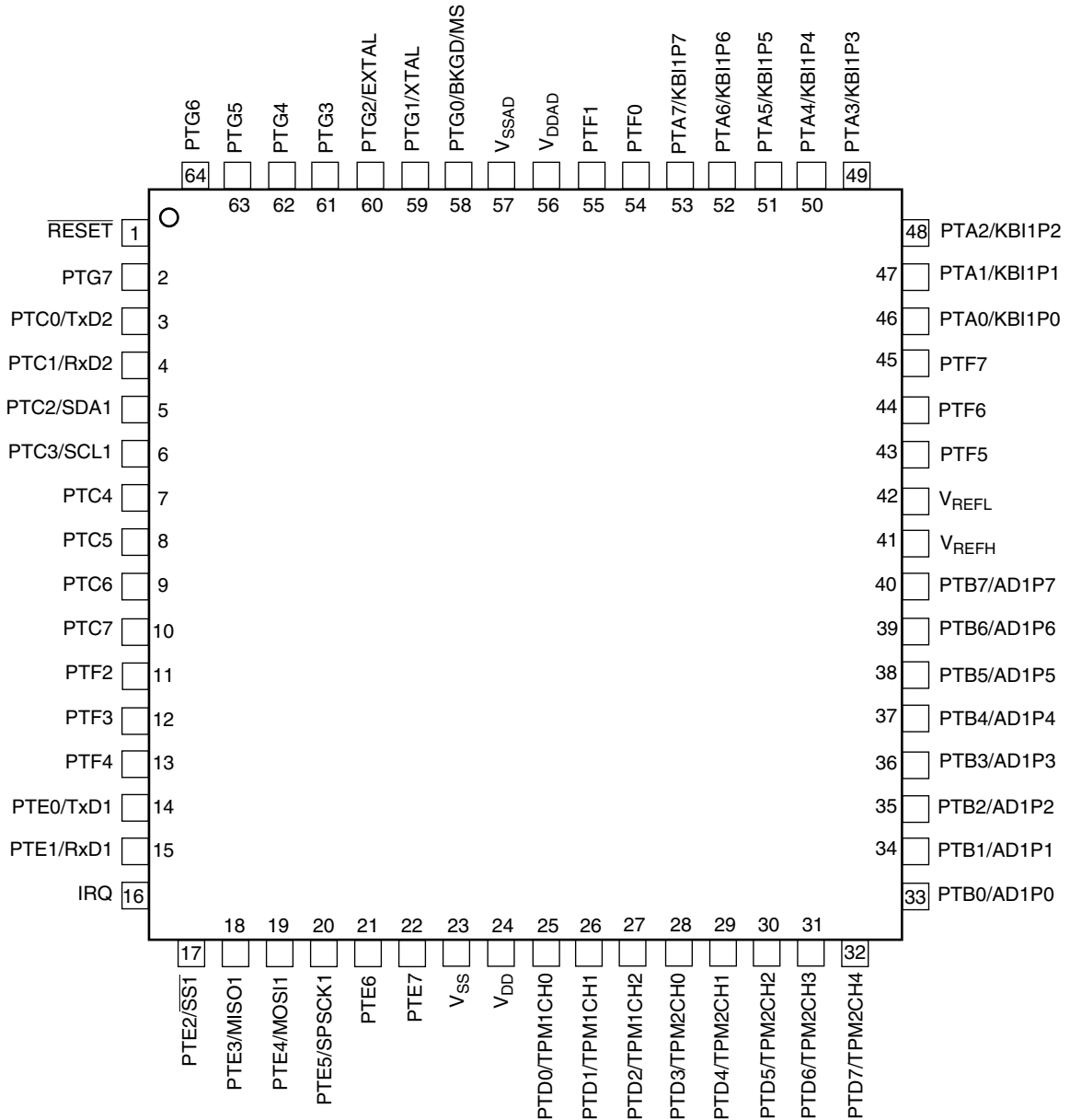


Figure 2-1. MC9S08GBxx in 64-Pin LQFP Package



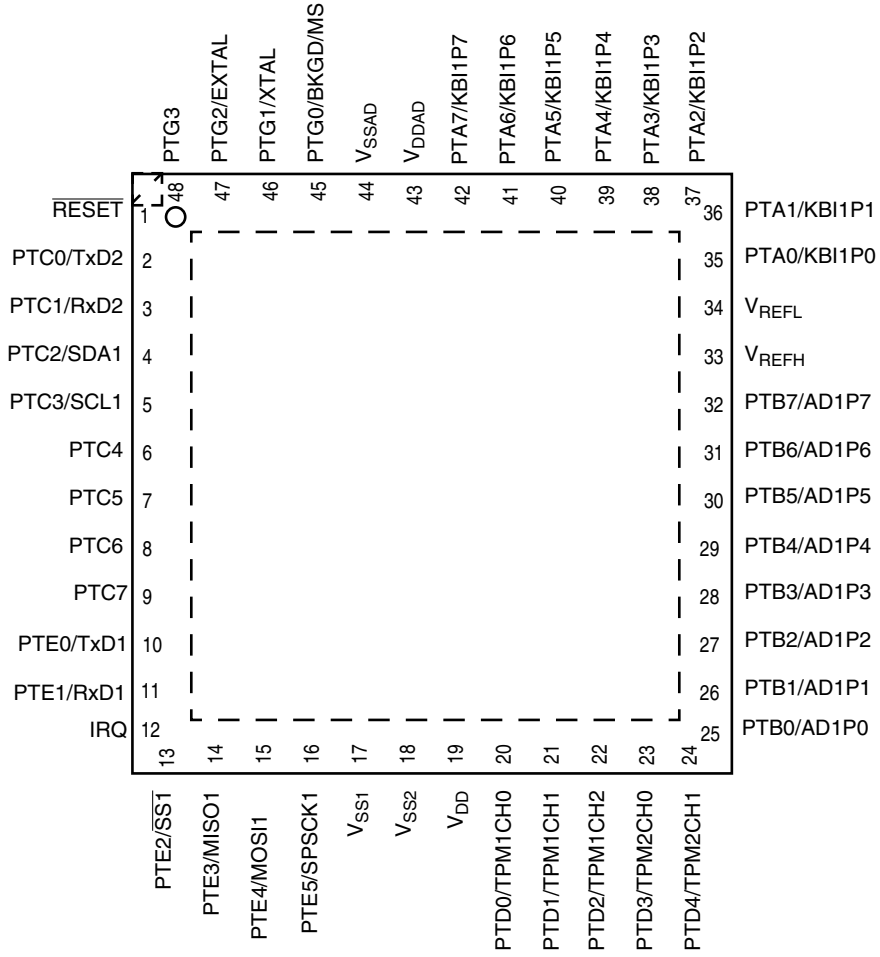


Figure 2-2. MC9S08GTxx in 48-Pin QFN Package

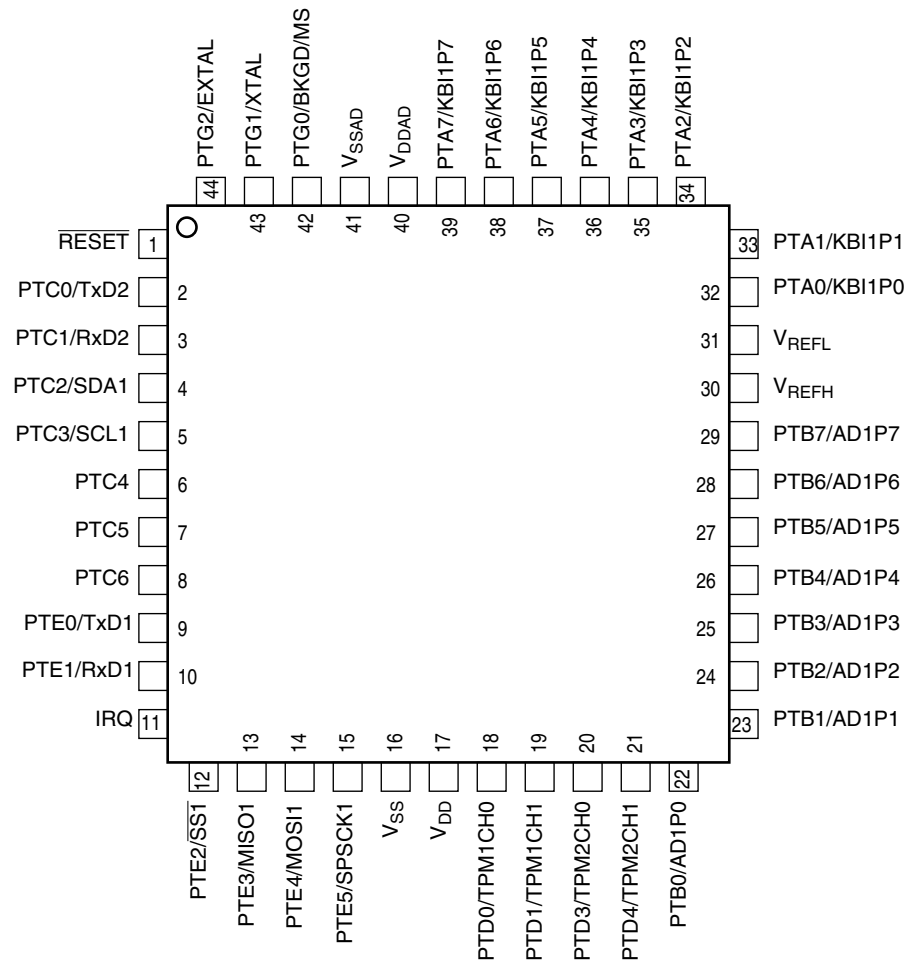


Figure 2-3. MC9S08GTxx in 44-Pin QFP Package