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Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC9S08GT16A
MC9S08GT8A

Data Sheet

HCS08
Microcontrollers

MC9S08GT16A
Rev. 1
7/2006

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MC9S08GT16A/GT8A Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

Memory Options

- FLASH read/program/erase down to 1.8 V
- Up to 16K FLASH; up to 2K RAM

Power-Saving Modes

- Three very low power stop modes
- Reduced power wait mode
- Very low power real time interrupt for use in run, wait, and stop

Clock Source Options

- Clock sources to internal hardware frequency locked-loop (FLL): internal, external, crystal, or resonator
- Internal clock with ±0.2% trimming resolution and ±0.5% deviation across voltage or across temperature

System Protection

- Optional watchdog computer operating properly (COP) reset
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect and security

Peripherals

- ATD — 8-channel, 10-bit analog-to-digital converter
- SCI — Two serial communications interface modules
- SPI — Serial peripheral interface module
- IIC — Inter-integrated circuit bus module
- Timer —One 3-channel timer PWM module (TPM) plus one 2-channel TPM
- KBI — 8-pin keyboard interrupt module

Input/Output

- 8 high-current pins (20 mA each)
- Software selectable pullups on ports when used as input
- Internal pullup on $\overline{\text{RESET}}$ and IRQ pin to reduce customer system cost
- Up to 38 general-purpose input/output (I/O) pins, plus one output-only pin, depending on package selection

Development Support

- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip, in-circuit emulation (ICE) debug module with real-time bus capture. On-chip ICE debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data.
- Single-wire background debug interface

Package Options

- 48-pin QFN
- 44-pin QFP
- 42-pin PSDIP
- 32-pin QFN

MC9S08GT16A/GT8A Data Sheet

Covers: MC9S08GT16A
MC9S08GT8A

MC9S08GT16A
Rev. 1
7/2006

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	07/17/2006	Initial public release

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Chapter 1
Device Overview

1.1 Introduction

The MC9S08GT16A/GT8A are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types (see Table 1-1).

1.1.1 Devices in the MC9S08GT16A/GT8A Series

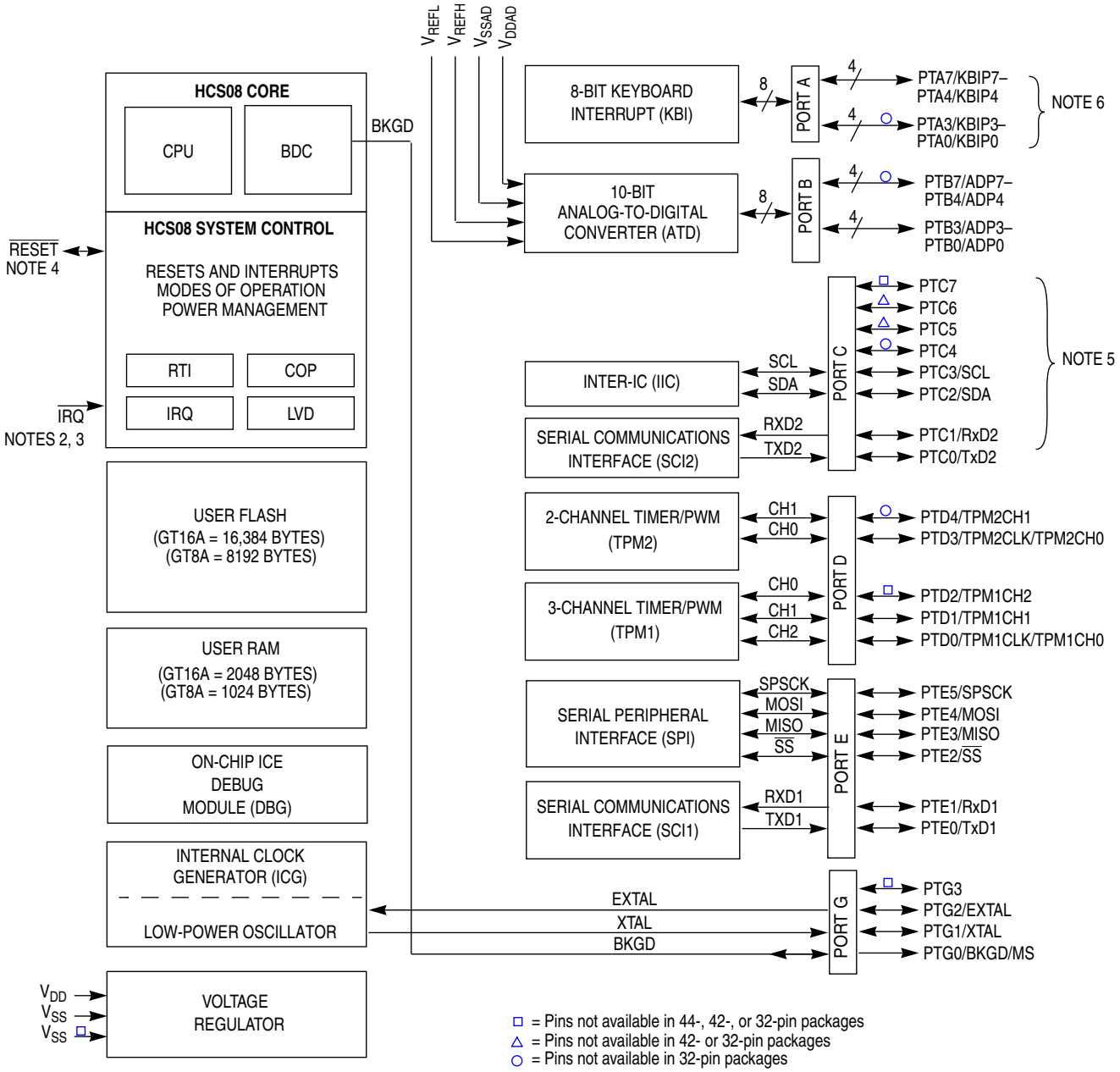
Table 1-1 lists the devices available in the MC9S08GT16A/GT8A series and summarizes the differences among them.

Table 1-1. Devices in the MC9S08GT16A/GT8A Series

Device	FLASH	RAM	TPM	ATD	KBI	I/O	Packages
MC9S08GT16A	16K	2K	(1) 3-ch, (1) 2-ch, 16-bit	8	8	39	48 QFN
			(2) 2-ch, 16-bit	8	8	36	44 QFP
			(2) 2-ch, 16-bit	8	8	34	42 SDIP
			(1) 2-ch, (1) 1-ch, 16-bit	4	4	24	32 QFN
MC9S08GT8A	8K	1K	(1) 3-ch, (1) 2-ch, 16-bit	8	8	39	48 QFN
			(2) 2-ch, 16-bit	8	8	36	44 QFP
			(2) 2-ch, 16-bit	8	8	34	42 SDIP
			(1) 2-ch, (1) 1-ch, 16-bit	4	4	24	32 QFN

1.1.2 MCU Block Diagram

This block diagrams show the structure of the MC9S08GT16A/GT8A MCUs.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains pullup/pulldown device if IRQ enabled (IRQPE = 1).
3. IRQ does not have a clamp diode to V_{DD}. IRQ should not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. High current drive
6. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown available when KBI enabled (KBIPn = 1).

Figure 1-1. MC9S08GT16A/GT8A Block Diagram

Table 1-2 lists the functional versions of the on-chip modules.

Table 1-2. Block Versions

Module	Version
Analog-to-Digital Converter (ATD)	3
Internal Clock Generator (ICG)	4
Inter-Integrated Circuit (IIC)	1
Keyboard Interrupt (KBI)	1
Serial Communications Interface (SCI)	1
Serial Peripheral Interface (SPI)	3
Timer Pulse-Width Modulator (TPM)	2
Central Processing Unit (CPU)	2

1.2 System Clock Distribution

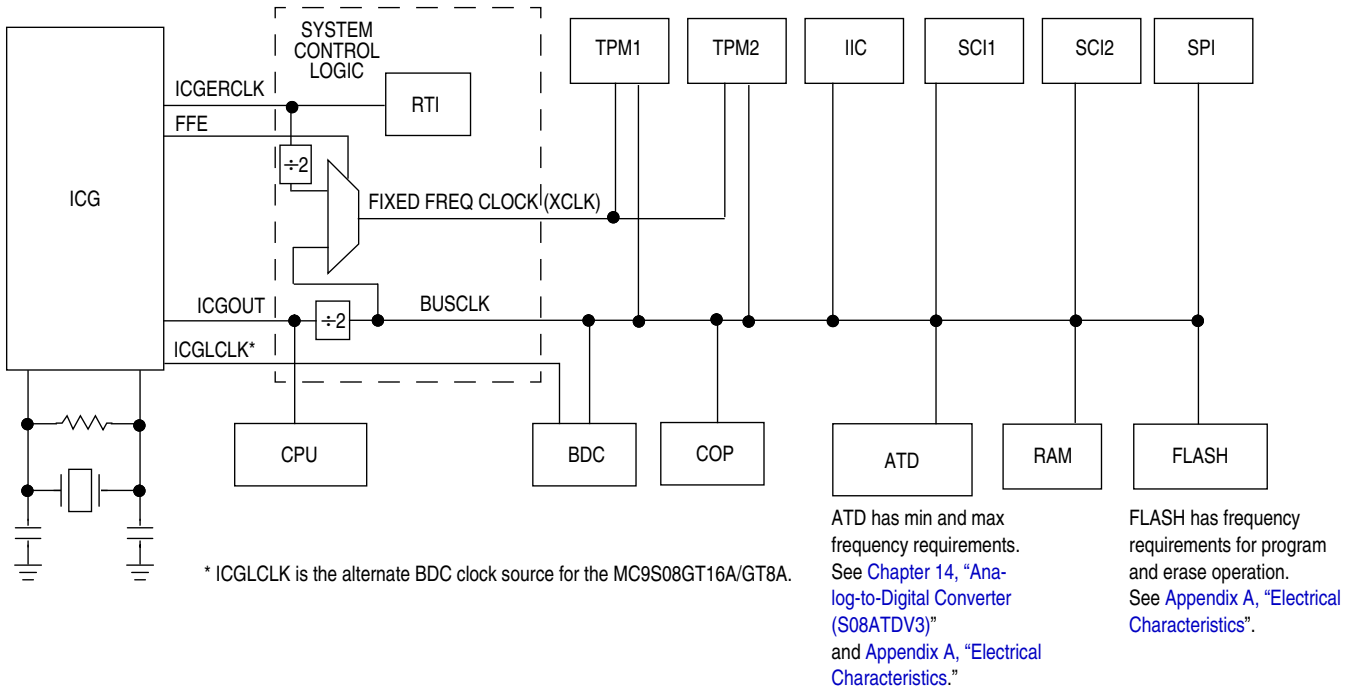


Figure 1-2. System Clock Distribution Diagram

Some of the modules inside the MCU have clock source choices. Figure 1-2 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
  - The external crystal oscillator
  - An external clock source
  - The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module

Control bits inside the ICG determine which source is connected.

- FFE is a control signal generated inside the ICG. If the frequency of ICGOUT > 4 × the frequency of ICGERCLK, this signal is a logic 1 and the fixed-frequency clock will be the ICGERCLK. Otherwise the fixed-frequency clock will be BUSCLK.
- ICGLCLK — Development tools can select this internal self-clocked source (~ 8 MHz) to speed up BDC communications in systems where the bus clock is slow.
- ICGERCLK — External reference clock can be selected as the real-time interrupt clock source.

Chapter 2
Pins and Connections

2.1 Introduction

This section describes signals that connect to package pins. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals.

2.2 Device Pin Assignment

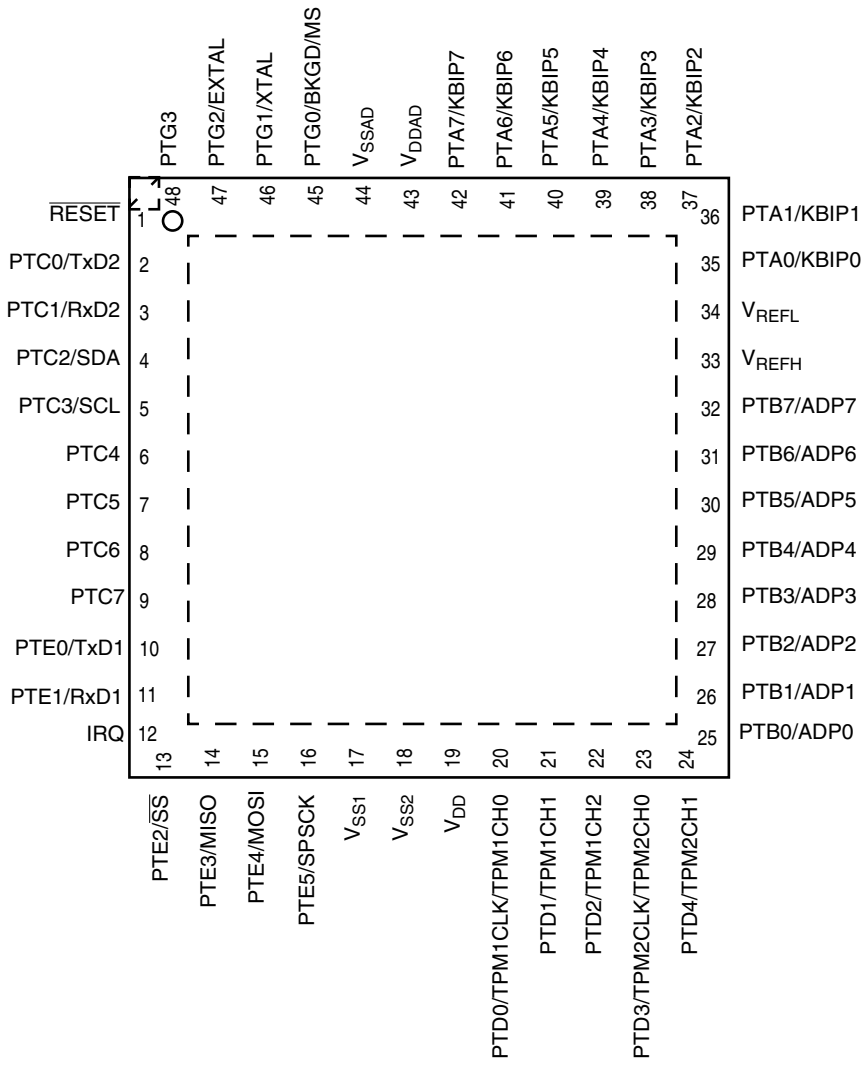


Figure 2-1. MC9S08GT16A/GT8A in 48-Pin QFN Package