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# Freescale Semiconductor

## Data Sheet: Advanced Information

An Energy-Efficient Solution from Freescale

### MC9S08JE128 series

Covers: MC9S08JE128 and MC9S08JE64

Document Number: MC9S08JE128

Rev. 3, 04/2010



#### 8-Bit HCS08 Central Processor Unit (CPU)

- Up to 48-MHz CPU above 2.4 V, 40 MHz CPU above 2.1 V, and 20 MHz CPU above 1.8 V across temperature of -40°C to 105°C
- HCS08 instruction set with added BGRND instruction
- Support for up to 32 interrupt/reset sources

#### On-Chip Memory

- 128 K Dual Array Flash read/program/erase over full operating voltage and temperature
- 12 KB Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and Flash

#### Power-Saving Modes

- Two ultra-low power stop modes. Peripheral clock enable register can disable clocks to unused modules to reduce currents
- Time of Day (TOD) — Ultra-low power 1/4 sec counter with up to 64s timeout.
- Ultra-low power external oscillator that can be used in stop modes to provide accurate clock source to the TOD. 6 usec typical wake up time from stop3 mode

#### Clock Source Options

- Oscillator (XOSC1) — Loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator dedicated for TOD operation.
- Oscillator (XOSC2) — for high frequency crystal input for MCG reference to be used for system clock and USB operations.
- Multipurpose Clock Generator (MCG) — PLL and FLL; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports CPU frequencies from 4 kHz to 48 MHz.

#### System Protection

- Watchdog computer operating properly (COP) reset Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points; separate low-voltage warning with optional interrupt; selectable trip points
- Illegal opcode and illegal address detection with reset
- Flash block protection for each array to prevent accidental write/erasure
- Hardware CRC to support fast cyclic redundancy checks

#### Development Support

- Single-wire background debug interface
- Real-time debug with 6 hardware breakpoints (4 PC, 1 address and 1 data) Breakpoint capability to allow single breakpoint setting during in-circuit debugging
- On-chip in-circuit emulator (ICE) debug module containing 3 comparators and 9 trigger modes

#### Peripherals

- **CMT**— Carrier Modulator timer for remote control communications. Carrier generator, modulator and driver for dedicated infrared out. Can be used as an output compare timer.
- **IIC**— Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven

- byte-by-byte data transfer; supports broadcast mode and 11-bit addressing
- **PRACMP** — Analog comparator with selectable interrupt; compare option to programmable internal reference voltage; operation in stop3
- **SCI** — Two serial communications interfaces with optional 13-bit break; option to connect Rx input to PRACMP output on SCI1 and SCI2; High current drive on Tx on SCI1 and SCI2; wake-up from stop3 on Rx edge
- **SPI1**— Serial peripheral interface (SPI) with 64-bit FIFO buffer; 16-bit or 8-bit data transfers; full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **SPI2**— Serial peripheral interface with full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **TPM** — Two 4-channel Timer/PWM Module; Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel; external clock input/pulse accumulator
- **USB** — Supports USB in full-speed device configuration. On-chip transceiver and 3.3V regulator help save system cost, fully compliant with USB Specification 2.0. Allows control, bulk, interrupt and isochronous transfers.
- **ADC12** — 12-bit Successive approximation ADC with up to 4 dedicated differential channels and 8 single-ended channels; range compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V, Configurable hardware trigger for 8 Channel select and result registers
- **PDB** — Programmable delay block with 16-bit counter and modulus and prescale to set reference clock to bus divided by 1 to bus divided by 2048; 8 trigger outputs for ADC12 module provides periodic coordination of ADC sampling sequence with sequence completion interrupt; Back-to-Back mode and Timed mode
- **DAC** — 12-bit resolution; 16-word data buffers with configurable watermark.

#### Input/Output

- Up to 47 GPIOs and 2 output-only pin and 1 input-only pin.
- Voltage Reference output (VREF0).
- Dedicated infrared output pin (IRO) with high current sink capability.
- Up to 16 KBI pins with selectable polarity.

#### Package Options

- 81-MBGA 10x10 mm
- 80-LQFP 12x12 mm
- 64-LQFP 10x10 mm



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Preliminary — Subject to Change

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## Related Documentation

Find the most current versions of all documents at: <http://www.freescale.com>.

### Reference Manual —MC9S08JE128RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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# 1 Devices in the MC9S08JE128 series

The following table summarizes the feature set available in the MC9S08JE128 series of MCUs.

**Table 1. MC9S08JE128 series Features by MCU and Package**

Feature	MC9S08JE128			MC9S08JE64
Pin quantity	81	80	64	64
FLASH size (bytes)	131072			65535
RAM size (bytes)	12K			12K
Programmable Analog Comparator (PRACMP)	yes			yes
Debug Module (DBG)	yes			yes
Multipurpose Clock Generator (MCG)	yes			yes
Inter-Integrated Communication (IIC)	yes			yes
Interrupt Request Pin (IRQ)	yes			yes
Keyboard Interrupt (KBI)	16	16	7	7
Port I/O <sup>1</sup>	47	46	33	33
Dedicated Analog Input Pins	12			12
Power and Ground Pins	8			8
Time Of Day (TOD)	yes			yes
Serial Communications (SCI1)	yes			yes
Serial Communications (SCI2)	yes			yes
Serial Peripheral Interface 1 (SPI1 (FIFO))	yes			yes
Serial Peripheral Interface 2 (SPI2)	yes			yes
Carrier Modulator Timer pin (IRO)	yes			yes
TPM input clock pin (TPMCLK)	yes			yes
TPM1 channels	4			4
TPM2 channels	4	4	2	2
XOSC1	yes			yes
XOSC2	yes			yes
USB	yes			yes
Programmable Delay Block (PDB)	yes			yes
SAR ADC differential channels <sup>2</sup>	4	4	3	3
SAR ADC single-ended channels	8	8	6	6
Voltage reference output pin (VREFO)	yes			yes

<sup>1</sup> Port I/O count does not include two (2) output-only and one (1) input-only pins.

<sup>2</sup> Each differential channel is comprised of 2 pin inputs.

## Devices in the MC9S08JE128 series

A complete description of the modules included on each device is provided in the following table.

**Table 2. Versions of On-Chip Modules**

Module	Version
Analog-to-Digital Converter (ADC12)	1
Digital to Analog Converter (DAC)	1
Programmable Delay Block	1
Inter-Integrated Circuit (IIC)	3
Central Processing Unit (CPU)	5
On-Chip In-Circuit Debug/Emulator (DBG)	3
Multi-Purpose Clock Generator (MCG)	3
Low Power Oscillator (XOSCVLP)	1
Carrier Modulator Timer (CMT)	1
Programable Analog Comparator (PRACMP)	1
Serial Communications Interface (SCI)	4
Serial Peripheral Interface (SPI)	5
Time of Day (TOD)	1
Universal Serial Bus (USB)	1
Timer Pulse-Width Modulator (TPM)	3
System Integration Module (SIM)	1
Cyclic Redundancy Check (CRC)	3
Keyboard Interrupt (KBI)	2
Voltage Reference (VREF)	1
Voltage Regulator (VREG)	1
Interrupt Request (IRQ)	3
Flash Wrapper	1
GPIO	2
Port Control	1

The block diagram in [Figure 1](#) shows the structure of the MC9S08JE128 series MCU.

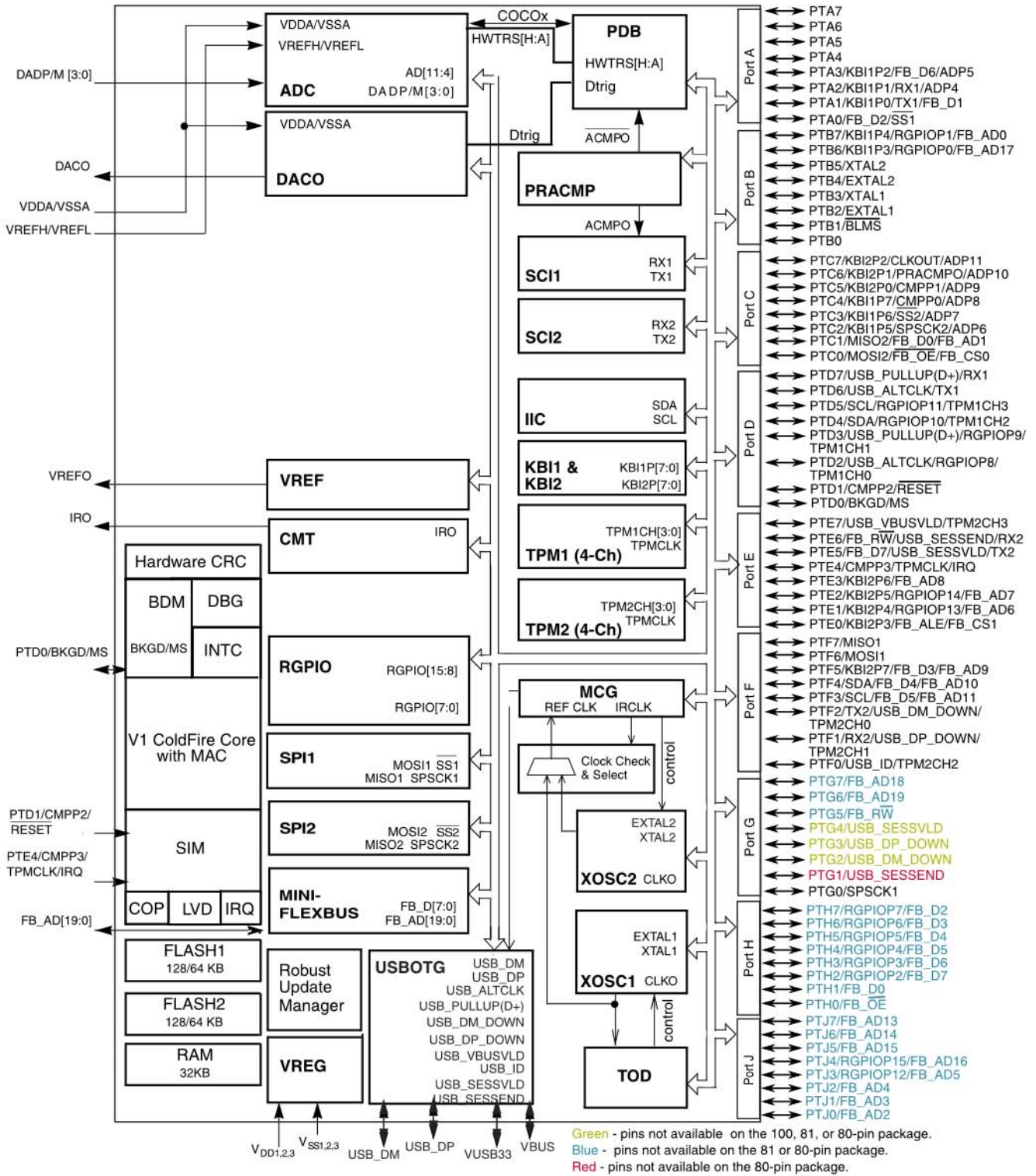


Figure 1. MC9S08JE128 series Block Diagram

# 1.1 Pin Assignments

This section shows the pin assignments for the MC9S08JE128 series devices.

## 1.1.1 64-Pin LQFP

The following two figures show the 64-pin LQFP pinout configuration.

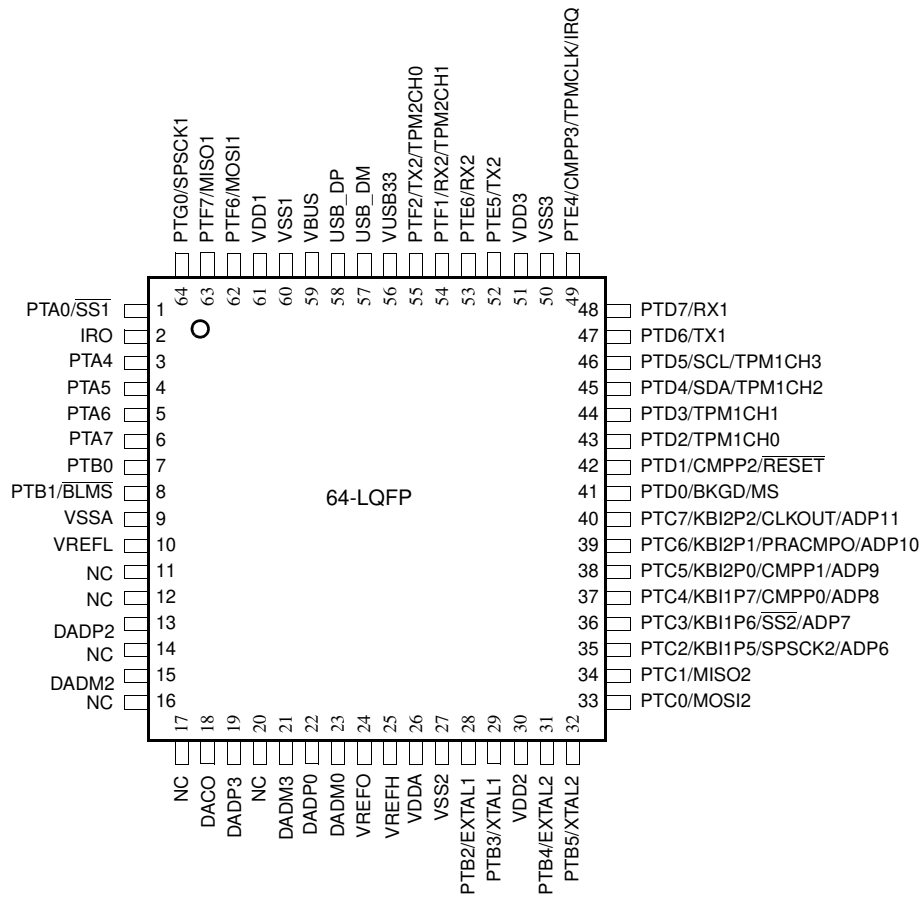


Figure 2. 64-Pin LQFP

### 1.1.2 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

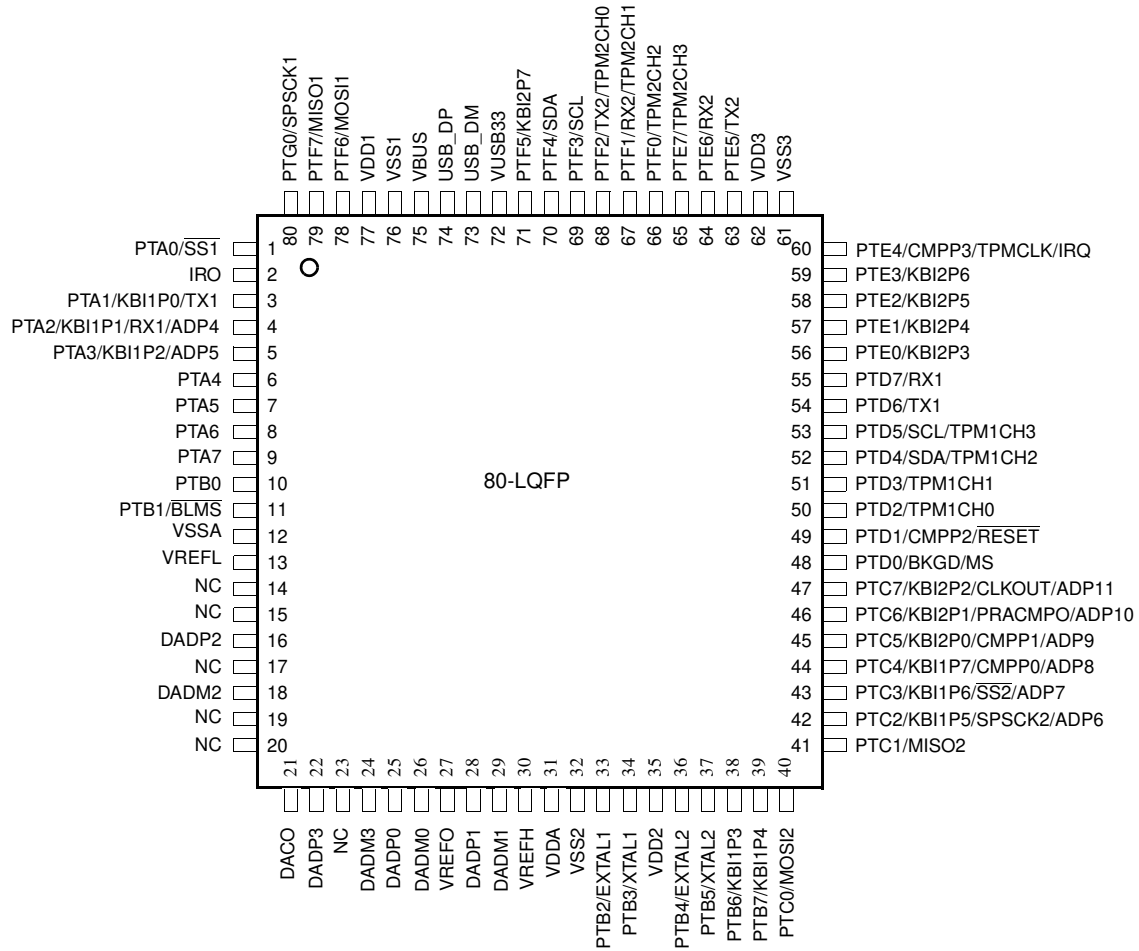


Figure 3. 80-Pin LQFP



### 1.1.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1
D		PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0
E		DADM2		VDD2	VDD3	VDD1	PTD2	PTD3	PTD6
F		DADP2		VSS2	VSS3	VSS1	PTB7	PTC7	PTD4
G	DADP0	DACO	DADP3	DADM3	VREFO	PTB6	PTC0	PTC1	PTC2
H	DADM0	DADM1	DADP1		PTC3	PTC4	PTD0	PTC5	PTC6
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5

**Figure 4. 81-Pin MAPBGA**

## 1.2 Pin Assignments by Packages

Table 3. Package Pin Assignments

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
B2	1	1	PTA0	$\overline{SS1}$	—	—	PTA0/ $\overline{SS1}$
A1	2	2	IRO	—	—	—	IRO
C4	3	—	PTA1	KBI1P0	TX1	—	PTA1/KBI1P0/TX1
D5	4	—	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
D6	5	—	PTA3	KBI1P2	ADP5	—	PTA3/KBI1P2/ADP5
C1	6	3	PTA4	—	—	—	PTA4
C2	7	4	PTA5	—	—	—	PTA5
C3	8	5	PTA6	—	—	—	PTA6
D2	9	6	PTA7	—	—	—	PTA7
D3	10	7	PTB0	—	—	—	PTB0
D4	11	8	PTB1	$\overline{BLMS}$	—	—	PTB1/ $\overline{BLMS}$
J1	12	9	VSSA	—	—	—	VSSA
J2	13	10	VREFL	—	—	—	VREFL
D1	14	11	NC	—	—	—	NC
E1	15	12	NC	—	—	—	NC
F2	16	13	DADP2	—	—	—	DADP2
F1	17	14	NC	—	—	—	NC
E2	18	15	DADM2	—	—	—	DADM2
F3	19	16	NC	—	—	—	NC
E3	20	17	NC	—	—	—	NC
G2	21	18	DACO	—	—	—	DACO
G3	22	19	DADP3	—	—	—	DADP3
H4	23	20	NC	—	—	—	NC
G4	24	21	DADM3	—	—	—	DADM3
G1	25	22	DADP0	—	—	—	DADP0
H1	26	23	DADM0	—	—	—	DADM0
G5	27	24	VREFO	—	—	—	VREFO
H3	28	—	DADP1	—	—	—	DADP1
H2	29	—	DADM1	—	—	—	DADM1

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
J3	30	25	VREFH	—	—	—	VREFH
J4	31	26	VDDA	—	—	—	VDDA
F4	32	27	VSS2	—	—	—	VSS2
J5	33	28	PTB2	EXTAL1	—	—	PTB2/EXTAL1
J6	34	29	PTB3	XTAL1	—	—	PTB3/XTAL1
E4	35	30	VDD2	—	—	—	VDD2
J8	36	31	PTB4	EXTAL2	—	—	PTB4/EXTAL2
J9	37	32	PTB5	XTAL2	—	—	PTB5/XTAL2
G6	38	—	PTB6	KBI1P3	—	—	PTB6/KBI1P3
F7	39	—	PTB7	KBI1P4	—	—	PTB7/KBI1P4
G7	40	33	PTC0	MOSI2	—	—	PTC0/MOSI2
G8	41	34	PTC1	MISO2	—	—	PTC1/MISO2
G9	42	35	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ADP6
H5	43	36	PTC3	KBI1P6	$\overline{SS2}$	ADP7	PTC3/KBI1P6/ $\overline{SS2}$ /ADP7
H6	44	37	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ADP8
H8	45	38	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ADP9
H9	46	39	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ADP10
F8	47	40	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ADP11
H7	48	41	PTD0	BKGD	MS	—	PTD0/BKGD/MS
J7	49	42	PTD1	CMPP2	$\overline{RESET}$	—	PTD1/CMPP2/ $\overline{RESET}$
E7	50	43	PTD2	TPM1CH0	—	—	PTD2/TPM1CH0
E8	51	44	PTD3	TPM1CH1	—	—	PTD3/TPM1CH1
F9	52	45	PTD4	SDA	TPM1CH2	—	PTD4/SDA/TPM1CH2
D7	53	46	PTD5	SCL	TPM1CH3	—	PTD5/SCL/TPM1CH3
E9	54	47	PTD6	TX1	—	—	PTD6/TX1
D8	55	48	PTD7	RX1	—	—	PTD7/RX1
D9	56	—	PTE0	KBI2P3	—	—	PTE0/KBI2P3
C9	57	—	PTE1	KBI2P4	—	—	PTE1/KBI2P4
C8	58	—	PTE2	KBI2P5	—	—	PTE2/KBI2P5
B9	59	—	PTE3	KBI2P6	—	—	PTE3/KBI2P6
A9	60	49	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/IRQ

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
F5	61	50	VSS3	—	—	—	VSS3
E5	62	51	VDD3	—	—	—	VDD3
C7	63	52	PTE5	TX2	—	—	PTE5/TX2
C6	64	53	PTE6	RX2	—	—	PTE6/RX2
B6	65	—	PTE7	TPM2CH3	—	—	PTE7/TPM2CH3
B8	66	—	PTF0	TPM2CH2	—	—	PTF0/TPM2CH2
B7	67	54	PTF1	RX2	TPM2CH1	—	PTF1/RX2/TPM2CH1
C5	68	55	PTF2	TX2	TPM2CH0	—	PTF2/TX2/TPM2CH0
A8	69	—	PTF3	SCL	—	—	PTF3/SCL
A7	70	—	PTF4	SDA	—	—	PTF4/SDA
B5	71	—	PTF5	KBI2P7	—	—	PTF5/KBI2P7
A6	72	56	VUSB33	—	—	—	VUSB33
B4	73	57	USB_DM	—	—	—	USB_DM
A4	74	58	USB_DP	—	—	—	USB_DP
A5	75	59	VBUS	—	—	—	VBUS
F6	76	60	VSS1	—	—	—	VSS1
E6	77	61	VDD1	—	—	—	VDD1
A3	78	62	PTF6	MOSI1	—	—	PTF6/MOSI1
B1	79	63	PTF7	MISO1	—	—	PTF7/MISO1
A2	80	64	PTG0	SPSCK1	—	—	PTG0/SPSCK1
B3	—	—	PTG1	—	—	—	PTG1

## 2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MC9S08JE128/64 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

### NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

### 2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 4. Parameter Classifications**

<b>P</b>	Those parameters are guaranteed during production testing on each individual device.
<b>C</b>	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
<b>T</b>	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
<b>D</b>	Those parameters are derived mainly from simulations.

### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## 2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

**Table 5. Absolute Maximum Ratings**

#	Rating	Symbol	Value	Unit
1	Supply voltage	$V_{DD}$	-0.3 to +3.8	V
2	Maximum current into $V_{DD}$	$I_{DD}$	120	mA
3	Digital input voltage	$V_{In}$	-0.3 to $V_{DD} + 0.3$	V
4	Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	$\pm 25$	mA
5	Storage temperature range	$T_{stg}$	-55 to 150	°C

<sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.

<sup>2</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ).

## 2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 6. Thermal Characteristics**

#	Symbol	Rating	Value	Unit
1	$T_A$	Operating temperature range (packaged):		°C
		MC9S08JE128	-40 to 105	
		MC9S08JE64	-40 to 105	
2	$T_{JMAX}$	Maximum junction temperature	135	°C
3	$\theta_{JA}$	Thermal resistance <sup>1,2,3,4</sup> Single-layer board — 1s		°C/W
		81-pin MBGA	77	
		80-pin LQFP	55	
		64-pin LQFP	68	
4	$\theta_{JA}$	Thermal resistance <sup>1, 2, 3, 4</sup> Four-layer board — 2s2p		°C/W
		81-pin MBGA	47	
		80-pin LQFP	40	
		64-pin LQFP	49	

<sup>1</sup> Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

<sup>2</sup> Junction to Ambient Natural Convection

<sup>3</sup> 1s — Single layer board, one signal layer

<sup>4</sup> 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

$T_A$  = Ambient temperature, °C

$\theta_{JA}$  = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$ , Watts — chip internal power

$P_{I/O}$  = Power dissipation on input and output pins — user determined

For most applications,  $P_{I/O} \ll P_{int}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving Equation 1 and Equation 2 iteratively for any value of  $T_A$ .

## 2.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (<http://www.aecouncil.com/>) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 7. ESD and Latch-up Test Conditions**

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	$\Omega$
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	$\Omega$
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

**Table 8. ESD and Latch-Up Protection Characteristics**

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	$V_{HBM}$	$\pm 2000$	—	V	T
2	Machine Model (MM)	$V_{MM}$	$\pm 200$	—	V	T
3	Charge Device Model (CDM)	$V_{CDM}$	$\pm 500$	—	V	T
4	Latch-up Current at $T_A = 125^\circ\text{C}$	$I_{LAT}$	$\pm 100$	—	mA	T



## 2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

**Table 9. DC Characteristics**

Num	Symbol	Characteristic	Condition	Min	Typ <sup>1</sup>	Max	Unit	C	
1	V <sub>DD</sub>	Operating Voltage	—	1.8 <sup>2</sup>	—	3.6	V	—	
2	V <sub>OH</sub>	Output high voltage	All I/O pins, low-drive strength	1.8 V, I <sub>Load</sub> = -600 μA	V <sub>DD</sub> - 0.5	—	—	V	C
			All I/O pins, high-drive strength	2.7 V, I <sub>Load</sub> = -10 mA	V <sub>DD</sub> - 0.5	—	—	V	P
			1.8V, I <sub>Load</sub> = -3 mA	V <sub>DD</sub> - 0.5	—	—	V	C	
3	I <sub>OHT</sub>	Output high current	Max total I <sub>OH</sub> for all ports	—	—	100	mA	D	
4	V <sub>OL</sub>	Output low voltage	All I/O pins, low-drive strength	1.8 V, I <sub>Load</sub> = 600 μA	—	—	0.5	V	C
			All I/O pins, high-drive strength	2.7 V, I <sub>Load</sub> = 10 mA	—	—	0.5	V	P
			1.8 V, I <sub>Load</sub> = 3 mA	—	—	0.5	V	C	
5	I <sub>OLT</sub>	Output low current	Max total I <sub>OL</sub> for all ports	—	—	100	mA	D	
6	V <sub>IH</sub>	Input high voltage	all digital inputs, V <sub>DD</sub> > 2.7 V	0.70 x V <sub>DD</sub>	—	—	V	P	
			all digital inputs, 2.7 V > V <sub>DD</sub> ≥ 1.8 V	0.85 x V <sub>DD</sub>	—	—	V	P	

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ <sup>1</sup>	Max	Unit	C	
7	$V_{IL}$	Input low voltage all digital inputs	all digital inputs, $V_{DD} > 2.7\text{ V}$	—	—	$0.35 \times V_{DD}$	V	P	
			all digital inputs, $2.7 > V_{DD} \geq 1.8\text{ V}$	—	—	$0.30 \times V_{DD}$	V	P	
8	$V_{hys}$	Input hysteresis all digital inputs	—	$0.06 \times V_{DD}$	—	—	mV	C	
9	$ I_{In} $	Input leakage current all input only pins (Per pin)	$V_{In} = V_{DD}$ or $V_{SS}$	—	—	0.25 (TBD)	$\mu\text{A}$	P	
10	$ I_{OZ} $	Hi-Z (off-state) leakage current all input/output (per pin)	$V_{In} = V_{DD}$ or $V_{SS}$	—	—	1 (TBD)	$\mu\text{A}$	P	
11	$ I_{OZ} $	Leakage current for analog output pins (DACO, VREFO) all input/output (per pin)	$V_{In} = V_{DD}$ or $V_{SS}$	—	—	(TBD)	$\mu\text{A}$	P	
12	$ I_{InT} $	Total Leakage Current <sup>3</sup> For all pins	—	—	—	2	$\mu\text{A}$	D	
13	$R_{PU}$	Pull-up resistors	—	17.5	—	52.5	$\text{k}\Omega$	P	
14	$R_{PD}$	Internal pull-down resistors <sup>4</sup>	—	17.5	—	52.5	$\text{k}\Omega$	P	
15	$I_{IC}$	DC injection current <sup>5, 6, 7</sup> Single pin limit	$V_{SS} > V_{IN} > V_{DD}$	-0.2	—	0.2	mA	D	
			Total MCU limit, includes sum of all stressed pins						
			$V_{SS} > V_{IN} > V_{DD}$	-5	—	5	mA	D	
16	$C_{In}$	Input Capacitance, all pins	—	—	—	8	pF	C	
17	$V_{RAM}$	RAM retention voltage	—	—	0.6	1.0	V	C	
18	$V_{POR}$	POR re-arm voltage <sup>8</sup>	—	0.9	1.4	1.79	V	C	
19	$t_{POR}$	POR re-arm time	—	10	—	—	$\mu\text{s}$	D	

**Table 9. DC Characteristics (Continued)**

Num	Symbol	Characteristic	Condition	Min	Typ <sup>1</sup>	Max	Unit	C	
20	V <sub>LVDH</sub> <sup>9</sup>	Low-voltage detection threshold — high range	V <sub>DD</sub> falling	—	2.11	2.16	2.22	V	P
			V <sub>DD</sub> rising	—	2.16	2.23	2.27	V	P
		Low-voltage detection threshold — low range <sup>9</sup>	V <sub>DD</sub> falling	—	1.80	1.84	1.88	V	P
			V <sub>DD</sub> rising	—	1.88	1.93	1.96	V	P
22	V <sub>LVWH</sub>	Low-voltage warning threshold — high range <sup>9</sup>	V <sub>DD</sub> falling	—	2.36	2.46	2.56	V	P
			V <sub>DD</sub> rising	—	2.36	2.46	2.56	V	P
		Low-voltage warning threshold — low range <sup>9</sup>	V <sub>DD</sub> falling	—	2.11	2.16	2.22	V	P
			V <sub>DD</sub> rising	—	2.16	2.23	2.27	V	P
24	V <sub>hys</sub>	Low-voltage inhibit reset/recover hysteresis <sup>10</sup>	—	—	50	—	mV	C	
25	V <sub>BG</sub>	Bandgap Voltage Reference <sup>11</sup>	—	1.15	1.17	1.18	V	P	

<sup>1</sup> Typical values are measured at 25°C. Characterized, not tested

<sup>2</sup> As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V<sub>LVDL</sub>.

<sup>3</sup> Total Leakage current is the sum value for all GPIO pins; this leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

<sup>4</sup> Measured with V<sub>In</sub> = V<sub>DD</sub>.

<sup>5</sup> All functional non-supply pins are internally clamped to V<sub>SS</sub> and V<sub>DD</sub>.

<sup>6</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

- <sup>7</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{in} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).
- <sup>8</sup> Maximum is highest voltage that POR is guaranteed.
- <sup>9</sup> Run at 1 MHz bus frequency
- <sup>10</sup> Low voltage detection and warning limits measured at 1 MHz bus frequency.
- <sup>11</sup> Factory trimmed at  $V_{DD} = 3.0$  V, Temp = 25°C

## 2.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V <sub>DD</sub> (V)	Typ <sup>1</sup>	Max	Unit	Temp (°C)	C
1	R <sub>I</sub> DD	Run supply current FEI mode All modules ON	24 MHz	3	20	24	mA	-40 to 25	P
			24 MHz	3	20	TBD	mA	105	P
			20 MHz	3	18	—	mA	-40 to 105	T
			8 MHz	3	8	—	mA	-40 to 105	T
			1 MHz	3	1.8	—	mA	-40 to 105	T
2	R <sub>I</sub> DD	Run supply current FEI mode; All modules OFF	24 MHz	3	12.3	TBD	mA	-40 to 105	C
			20 MHz	3	10.5	—	mA	-40 to 105	T
			8 MHz	3	4.8	—	mA	-40 to 105	T
			1 MHz	3	1.3	—	mA	-40 to 105	T
3	R <sub>I</sub> DD	Run supply current LPS=0; All modules OFF	16 kHz FBILP	3	TBD	—	μA	-40 to 105	T
			16 kHz FBELP	3	TBD	—	μA	-40 to 105	T
4	R <sub>I</sub> DD	Run supply current LPS=1, all modules OFF	16 kHz FBELP	3	TBD	—	μA	0 to 70	T
			16 kHz FBELP	3	TBD	—	μA	-40 to 105	T

Table 10. Supply Current Characteristics (Continued)

#	Symbol	Parameter	Bus Freq	V <sub>DD</sub> (V)	Typ <sup>1</sup>	Max	Unit	Temp (°C)	C
5	W <sub>I</sub> DD	Wait mode supply current FEI mode, all modules OFF	24 MHz	3	TBD	6	mA	-40 to 105	C
			20 MHz	3	TBD	—	mA	-40 to 105	T
			8 MHz	3	TBD	—	mA	-40 to 105	T
			1 MHz	3	TBD	—	mA	-40 to 105	T
6	S2 <sub>I</sub> DD	Stop2 mode supply current	N/A	3	0.39	0.6	μA	-40 to 25	P
			N/A	3	TBD	TBD	μA	70	C
			N/A	3	7	TBD	μA	85	C
			N/A	3	16	TBD	μA	105	P
			N/A	2	TBD	TBD	μA	-40 to 25	C
			N/A	2	TBD	TBD	μA	70	C
			N/A	2	TBD	TBD	μA	85	C
			N/A	2	TBD	TBD	μA	105	C
7	S3 <sub>I</sub> DD	Stop3 mode supply current No clocks active	N/A	3	0.55	0.9	μA	-40 to 25	P
			N/A	3	TBD	TBD	μA	70	C
			N/A	3	14	TBD	μA	85	C
			N/A	3	37	TBD	μA	105	P
			N/A	2	TBD	TBD	μA	-40 to 25	C
			N/A	2	TBD	TBD	μA	70	C
			N/A	2	14	TBD	μA	85	C
			N/A	2	TBD	TBD	μA	105	C

<sup>1</sup> Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

**Table 11. Typical Stop Mode Adders**

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600 (TBD)	650 (TBD)	750 (TBD)	850 (TBD)	1000 (TBD)	nA	D
3	IREFSTEN <sup>1</sup>	—	68	70	77	86	120	μA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D
5	LVD <sup>1</sup>	LVDSE = 1	114	115	123	135	170	μA	T
6	ACMP <sup>1</sup>	Not using the bandgap (BGBE = 0)	18	20	23	33	65	μA	T
7	ADC <sup>1</sup>	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	75	85	100	115	165	μA	T
8	DAC <sup>1</sup>	High power mode; no load on DACO	500	500	500	500	500	μA	T

<sup>1</sup> Not available in stop2 mode.

## 2.7 PRACMP Electricals

**Table 12. PRACMP Electrical Specifications**

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V <sub>PWR</sub>	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I <sub>DDACT1</sub>	—	—	60	μA	C
3	Supply current (active) (PRG disabled)	I <sub>DDACT2</sub>	—	—	40	μA	C
4	Supply current (ACMP and PRG all disabled)	I <sub>DDDIS</sub>	—	—	2	nA	D
5	Analog input voltage	V <sub>AIN</sub>	V <sub>SS</sub> - 0.3	—	V <sub>DD</sub>	V	—
6	Analog input offset voltage	V <sub>AIO</sub>	—	5	40	mV	T
7	Analog comparator hysteresis	V <sub>H</sub>	3.0	—	20.0	mV	T
8	Analog input leakage current	I <sub>ALKG</sub>	—	—	1	nA	D
9	Analog comparator initialization delay	t <sub>AINIT</sub>	—	—	1.0	μs	T

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
10	Programmable reference generator inputs	$V_{In2}(V_{DD25})$	1.8	—	2.75	V	—
11	Programmable reference generator setup delay	$t_{PRGST}$	—	1	—	$\mu\text{s}$	D
12	Programmable reference generator step size	$V_{step}$	-0.25	1	0.25	LSB	D
13	Programmable reference generator voltage range	$V_{prgout}$	$V_{In}/32$	—	$V_{in}$	V	P

## 2.8 12-bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	$V_{DDA}$	1.8	3.6	V	P	
2	Reference voltage	$V_{DACR}$	1.15	3.6	V	C	
3	Temperature	$T_A$	-40	105	$^{\circ}\text{C}$	C	
4	Output load capacitance	$C_L$	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	$I_L$	—	1	mA	C	



Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Resolution	N	12	12	bit	C	
2	Supply current low-power mode	$I_{DDA\_DACLP}$	50	100	$\mu A$	C	
3	Supply current high-power mode	$I_{DDA\_DACHP}$	120	500 (TBD)	$\mu A$	C	
4	Full-scale Settling time ( $\pm 0.5$ LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$T_{SFSLP}$	—	200 (TBD)	$\mu s$	C	
5	Full-scale Settling time ( $\pm 0.5$ LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$T_{SFHP}$	—	30	$\mu s$	C	
6	Code-to-code Settling time ( $\pm 0.5$ LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$T_{SCCLP}$	—	5	$\mu s$	C	
7	Code-to-code Settling time ( $\pm 0.5$ LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode	$T_{SCCHP}$	—	1(TBD)	$\mu s$	C	
8	DAC output voltage range low (high-power mode, no load, DAC set to 0)	$V_{dacoutl}$	—	100 (TBD)	mV	C	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	$V_{DACR} - 100$	—	mV	C	
10	Integral non-linearity error	INL	—	$\pm 8$	LSB	C	
11	Differential non-linearity error VDACR is > 2.4 V	DNL	—	$\pm 1$	LSB	C	
12	Offset error	$E_O$	—	$\pm 0.5$	%FSR	C	
13	Gain error	$E_G$	—	$\pm 0.5$ (TBD)	%FSR	C	
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	dB	C	
15	Temperature drift of offset voltage (DAC set to 0x0800)	$T_{co}$	—	2 (TBD)	mV	C	See Typical Drift figure that follows.
16	Offset aging coefficient	$A_c$	—	TBD	$\mu V/yr$	C	

Figure 5. Offset at Half Scale vs Temperature

## 2.9 ADC Characteristics

Table 15. 12-bit ADC Operating Conditions

#	Symb	Characteristic	Conditions	Min	Typ <sup>1</sup>	Max	Unit	C	Comment
1	V <sub>DDAD</sub>	Supply voltage	Absolute	1.8	—	3.6	V	D	
2	ΔV <sub>DDAD</sub>		Delta to V <sub>DD</sub> (V <sub>DD</sub> -V <sub>DDAD</sub> ) <sup>2</sup>	-100	0	+100	mV	D	
3	ΔV <sub>SSAD</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> -V <sub>SSAD</sub> ) <sup>2</sup>	-100	0	+100	mV	D	
4	V <sub>REFH</sub>	Ref Voltage High		1.13	V <sub>DDAD</sub>	V <sub>DDAD</sub>	V	D	
5	V <sub>REFL</sub>	Ref Voltage Low		V <sub>SSAD</sub>	V <sub>SSAD</sub>	V <sub>SSAD</sub>	V	D	
6	V <sub>ADIN</sub>	Input Voltage		V <sub>REFL</sub>	—	V <sub>REFH</sub>	V	D	
7	C <sub>ADIN</sub>	Input Capacitance		—	4	5	pF	C	
8	R <sub>ADIN</sub>	Input Resistance		—	2	5	kΩ	C	
9	R <sub>AS</sub>	Analog Source Resistance							External to MCU Assumes ADLSMP=0
			12-bit mode f <sub>ADCK</sub> > 4 MHz	—	—	2	kΩ	C	
			f <sub>ADCK</sub> < 4 MHz	—	—	5	kΩ	C	
			11/10-bit mode f <sub>ADCK</sub> > 8 MHz	—	—	2	kΩ	C	
			4 MHz < f <sub>ADCK</sub> < 8 MHz	—	—	5	kΩ	C	
			f <sub>ADCK</sub> < 4 MHz	—	—	10	kΩ	C	
			9/8-bit mode f <sub>ADCK</sub> > 4 MHz	—	—	5	kΩ	C	
			f <sub>ADCK</sub> < 4 MHz	—	—	10	kΩ	C	
10	f <sub>ADCK</sub>	ADC Conversion Clock Freq.	High Speed (ADLPC=0, ADHSC=1)	1.0	—	8.0	MHz	D	
			High Speed (ADLPC=0, ADHSC=0)	1.0	—	5.0	MHz	D	
			Low Power (ADLPC=1, ADHSC=1)	1.0	—	2.5	MHz	D	

<sup>1</sup> Typical values assume V<sub>DDAD</sub> = 3.0 V, Temp = 25 °C, f<sub>ADCK</sub>=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> DC potential difference.