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MC9S08JM60
MC9S08JM32

Data Sheet

HCS08
Microcontrollers

MC9S08JM60
Rev. 5
10/2014

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MC9S08JM60 Series Features

8-Bit HCS08 Central Processor Unit (CPU)

- 48-MHz HCS08 CPU (central processor unit)
- 24-MHz internal bus frequency
- HC08 instruction set with added BGND instruction
- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- In-circuit emulator (ICE) debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources

Memory Options

- Up to 60 KB of on-chip in-circuit programmable flash memory with block protection and security options
- Up to 4 KB of on-chip RAM
- 256 bytes of USB RAM

Clock Source Options

- Clock source options include crystal, resonator, external clock
- MCG (multi-purpose clock generator) — PLL and FLL; internal reference clock with trim adjustment

System Protection

- Optional computer operating properly (COP) reset with option to run from independent 1-kHz internal clock source or the bus clock
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Illegal address detection with reset

Power-Saving Modes

- Wait plus two stops

Peripherals

- **USB —** USB 2.0 full-speed (12 Mbps) device controller with dedicated on-chip USB transceiver, 3.3-V regulator and USBDP pull-up resister; supports control, interrupt, isochronous, and bulk transfers; supports endpoint 0 and up to 6 additional endpoints; endpoints 5 and 6 can be combined to provide double buffering capability
- **ADC** — 12-channel, 12-bit analog-to-digital converter with automatic compare function; internal temperature sensor
- **ACMP** — Analog comparator with option to compare to internal reference; operation in stop3 mode
- **SCI** — Two serial communications interface modules with optional 13-bit break LIN extensions
- **SPI** — Two 8- or 16-bit selectable serial peripheral interface modules with a receive data buffer hardware match function
- **IIC** — Inter-integrated circuit bus module to operate at up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt-driven byte-by-byte data transfer; 10-bit addressing and broadcast modes support
- **Timers** — One 2-channel and one 6-channel 16-bit timer/pulse-width modulator (TPM) modules: Selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels
- **KBI** — 8-pin keyboard interrupt module
- **RTC** — Real-time counter with binary- or decimal-based prescaler

Input/Output

- Up to 51 general-purpose input/output pins
- Software selectable pullups on ports when used as inputs
- Software selectable slew rate control on ports when used as outputs
- Software selectable drive strength on ports when used as outputs
- Master reset pin and power-on reset (POR)
- Internal pullup on $\overline{\text{RESET}}$, IRQ, and BKGD/MS pins to reduce customer system cost

Package Options

- 64-pin quad flat package (QFP)
- 64-pin low-profile quad flat package (LQFP)
- 48-pin quad flat no-lead (QFN)
- 44-pin low-profile quad flat package (LQFP)

MC9S08JM60 Series Data Sheet

Covers MC9S08JM60
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10/2014

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

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The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	11/27/2007	Initial release
2	3/4/2008	Changed the location of R_S to connect to EXTAL in Figure 2-4. Changed port rise and fall time in Table A-13. Added DC injection current and RAM retention voltage in Table A-6. Deleted note on 625 ns of item 17 in Table A-12. Moved Bandgap Voltage Reference item from Table A-8 to Table A-6. Added one paragraph on how to improve accuracy to Section 10.1.1.5, "Temperature Sensor."
3	1/21/2009	Changed the V_{TEMP25} from 1.396 mV to 1.396 V in Table A-10. Complete the EMC data in Section A.15, "EMC Performance." Revised the Typo in Table 11-4.
4	2/21/2010	Changed the location of R_S to connect to XTAL in Figure 2-4.
5	10/2014	Updated t_{LPO} in Table A-13.

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Chapter 1
Device Overview

1.1 Introduction

MC9S08JM60 series MCUs are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

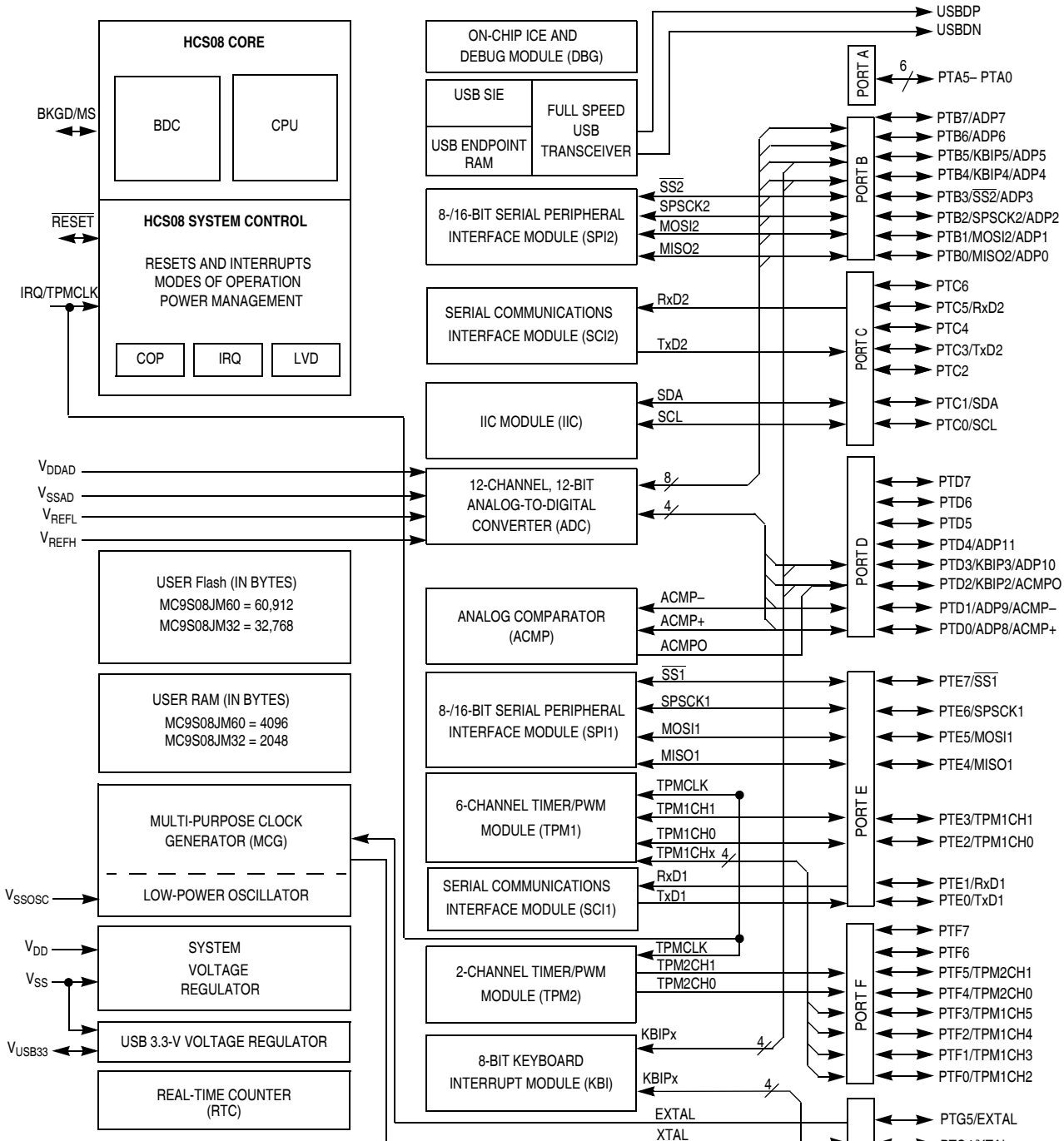
Table 1-1 summarizes the peripheral availability per package type for the devices available in the MC9S08JM60 series.

Table 1-1. Devices in the MC9S08JM60 Series

Feature	Device					
	MC9S08JM60			MC9S08JM32		
Package	64-pin	48-pin	44-pin	64-pin	48-pin	44-pin
Flash	60,912			32,768		
RAM	4096			2048		
USB RAM	256			256		
ACMP	yes			yes		
ADC	12-ch	8-ch	8-ch	12-ch	8-ch	8-ch
IIC	yes			yes		
IRQ	yes			yes		
KBI	8	7	7	8	7	7
SCI1	yes			yes		
SCI2	yes			yes		
SPI1	yes			yes		
SPI2	yes			yes		
TPM1	6-ch	4-ch	4-ch	6-ch	4-ch	4-ch
TPM2	2-ch			2-ch		
USB	yes			yes		
I/O pins	51	37	33	51	37	33
Package types	64 QFP 64 LQFP	48 QFN	44 LQFP	64 QFP 64 LQFP	48 QFN	44 LQFP

1.2 MCU Block Diagram

The block diagram in Figure 1-1 shows the structure of the MC9S08JM60 series MCU.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pull-down device if IRQ is enabled (IRQPE = 1). Pull-down is enabled if rising edge detect is selected (IRQEDG = 1)
3. IRQ does not have a clamp diode to V_{DD}. IRQ must not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pull-down device.

Figure 1-1. MC9S08JM60 Series Block Diagram

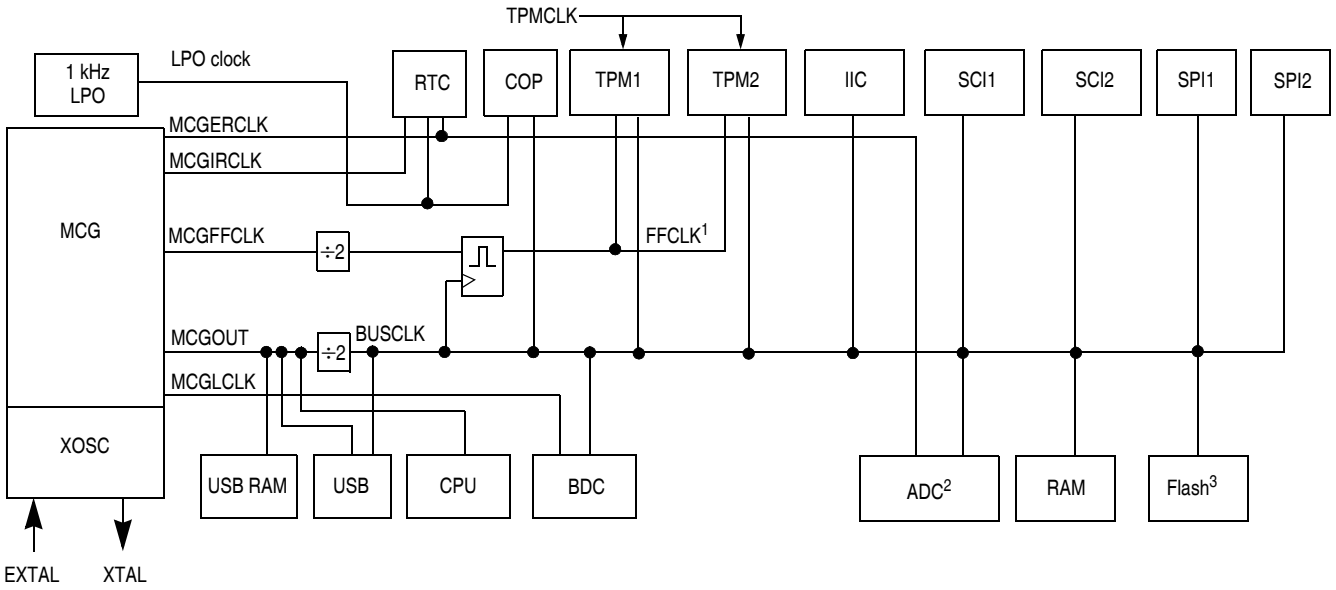
Table 1-2 lists the functional versions of the on-chip modules.

Table 1-2. Versions of On-Chip Modules

Module		Version
Analog Comparator	(ACMP)	2
Analog-to-Digital Converter	(ADC)	1
Central Processing Unit	(CPU)	2
IIC Module	(IIC)	2
Keyboard Interrupt	(KBI)	2
Multi-Purpose Clock Generator	(MCG)	1
Real-Time Counter	(RTC)	1
Serial Communications Interface	(SCI)	4
16-bit Serial Peripheral Interface	(SPI16)	1
Timer Pulse-Width Modulator	(TPM)	3
Universal Serial Bus	(USB)	1
Debug Module	(DBG)	2

1.3 System Clock Distribution

Figure 1-2 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function. All memory mapped registers associated with the modules are clocked with BUSCLK.



1. The FFCLK is internally synchronized to the bus clock and must not exceed one half of the bus clock frequency.

2. ADC has min. and max. frequency requirements. See Chapter 10, “Analog-to-Digital Converter (S08ADC12V1),” and Appendix A, “Electrical Characteristics,” for details.

3. Flash has the frequency requirements for program and erase operation. See the Appendix A, “Electrical Characteristics,” for details.

Figure 1-2. System Clock Distribution Diagram

The MCG supplies the following clock sources:

- MCGOUT — This clock source is used as the CPU, USB RAM and USB module clock, and is divided by two to generate the peripheral bus clock (BUSCLK). Control bits in the MCG control registers determine which of the three clock sources is connected:
  - Internal reference clock
  - External reference clock
  - Frequency-locked loop (FLL) or Phase-locked loop (PLL) output

  See Chapter 12, “Multi-Purpose Clock Generator (S08MCGV1),” for details on configuring the MCGOUT clock.
- MCGLCLK — This clock source is derived from the digitally controlled oscillator (DCO) of the MCG. Development tools can select this internal self-clocked source to speed up BDC communications in systems where the bus clock is slow.
- MCGIRCLK — This is the internal reference clock and can be selected as the real-time counter clock source. Chapter 12, “Multi-Purpose Clock Generator (S08MCGV1),” explains the MCGIRCLK in more detail. See Chapter 13, “Real-Time Counter (S08RTCV1),” for more information regarding the use of MCGIRCLK.
- MCGERCLK — This is the external reference clock and can be selected as the clock source of real-time counter and ADC module. Section 12.4.6, “External Reference Clock,” explains the MCGERCLK in more detail. See Chapter 13, “Real-Time Counter (S08RTCV1),” and Chapter 10,

"Analog-to-Digital Converter (S08ADC12V1)," for more information regarding the use of MCGERCLK with these modules.

- MCGFFCLK — This clock source is divided by 2 to generate FFCLK after being synchronized to the BUSCLK. It can be selected as clock source for the TPM modules. The frequency of the MCGFFCLK is determined by the settings of the MCG. See the Section 12.4.7, "Fixed Frequency Clock," for details.
- LPO clock— This clock is generated from an internal Low Power Oscillator that is completely independent of the MCG module. The LPO clock can be selected as the clock source to the RTC or COP modules. See Chapter 13, "Real-Time Counter (S08RTCV1)," and Section 5.4, "Computer Operating Properly (COP) Watchdog," for details on using the LPO clock with these modules.
- TPMCLK — TPMCLK is the optional external clock source for the TPM modules. The TPMCLK must be limited to 1/4th the frequency of the BUSCLK for synchronization. See Chapter 16, "Timer/Pulse-Width Modulator (S08TPMV3)," for more details.

Chapter 2
Pins and Connections

2.1 Introduction

This chapter describes signals that connect to package pins. It includes pinout diagrams, a table of signal properties, and detailed discussion of signals.