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Freescale Semiconductor
Data Sheet

Document Number: MC9S08LC60
Rev. 4.1 11/2014

MC9S08LC60 Data Sheet

Rev. 4.1 of the MC9S08LC60 data sheet has two parts:

- The addendum to revision 4 of the data sheet, immediately following this cover page.
- Revision 4 of the data sheet, following the addendum.

The addendum identifies errors and changes in revision 4 of the data sheet. It is intended to clearly identify changes so readers can find them easily.

Document Number: MC9S08LC60
Rev. 1 11/2014

Addendum for Rev. 4 of the MC9S08LC60 Data Sheet

1 Information removed from Figure 6-23, Pullup Enable for Port C (PTCPE)

Please remove the footnote 1 under Figure 6-23, Pullup Enable for Port C (PTCPE).

The note says, “PTCPE7 has no effect on the output-only PTC7 pin.”

The figure will now look like this:

	7	6	5	4	3	2	1	0
R W	PTCPE7	PTCPE6(1)	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
Reset	0	0	0	0	0	0	0	0

Figure 6-23. Pullup Enable for Port C (PTCPE)

1. PTCPE6 has no effect on the output-only PTC6 pin.

2 Information removed from Figure 6-24, Output Slew Rate Control Enable (PTCSE)

Please remove the footnote 2 under Figure 6-24, Output Slew Rate Control Enable (PTCSE).

The note says, “Reads of PTCD6 always return the contents of PTCD6, regardless of the value stored in the bit PTCDD6.”

The figure will now look like this:

	7	6	5	4	3	2	1	0
R W	PTCSE7(1)	PTCSE6	PTCSE5	PTCSE4	PTCSE3	PTCSE2	PTCSE1	PTCSE0
Reset	1	1	1	1	1	1	1	1

Figure 6-24. Slew Rate Control Enable for Port C (PTCSE)

1. PTCSE7 has no effect on the input-only PTC7 pin.

3 Information removed from Figure 6-25, Output Drive Strength Select (PTCDS)

Please remove the footnote 2 under Figure 6-25, Output Slew Rate Control Enable (PTCSE).

The note says, “PTCDD6 has no effect on the output-only PTC6 pin.”

The figure will now look like this:

	7	6	5	4	3	2	1	0
R W	PTCDS7(1)	PTCDS6	PTCDS5	PTCDS4	PTCDS3	PTCDS2	PTCDS1	PTCDS0
Reset	0	0	0	0	0	0	0	0

Figure 6-25. Drive Strength Selection for Port C (PTCDS)

1. PTCDS7 has no effect on the input-only PTC7 pin.

4 New information added to Table A-5

Please replace the I_{OZ} row of Table A-5 with this row of the table below.

Table A-5 DC Characteristics
(Temperature Range = -40 to 85°C Ambient)

Parameter	Symbol	Min	Typ(1)	Max	Unit
High impedance (off-state) leakage current (per pin) $V_{in} = V_{DD}$ or V_{SS}, all input/output (all except PTC7) $V_{in} = V_{DD}$ or V_{SS}, (PTC7 only)	$\|I_{OZ}\|$	—	0.025 0.025	1 3	µA

1. Typicals are measured at 25°C.

MC9S08LC60
MC9S08LC36

Data Sheet: Technical Data

HCS08
Microcontrollers

MC9S08LC60
Rev. 4
07/2007

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MC9S08LC60 Series Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU
- HC08 instruction set with added BGND instruction
- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- In-Circuit Emulator (ICE) debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. ICE debug module supports both tag and force breakpoints.
- Support for up to 32 interrupt/reset sources

Memory Options

- Dual on-chip in-circuit programmable FLASH memories with block protection and security options; 60K and 36K options available
- Program/erase of one FLASH array while executing from another
- On-chip random-access memory (RAM); 4K and 2.5K options available

Power-Saving Features

- Wait plus three stops
- Software disable of clock monitor and low-voltage interrupt (LVI) for lowest stop current
- Software-generated real-time clock (RTC) functions using real-time interrupt (RTI)

Configurable Clock Source

- Clock source options include crystal, resonator, external clock, or internally generated clock with precision nonvolatile memory (NVM) trimming
- Automatic clock monitor function

System Protection

- Optional computer operating properly (COP) reset
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset

Package Options

- 64-pin low-profile quad flat package (LQFP)
- 80-pin LQFP

Peripherals

- **LCD** (liquid crystal display driver) — Compatible with 5-V or 3-V LCD glass displays; functional in wait and stop3 low-power modes; selectable frontplane and backplane configurations:
  - 4 x 40 or 3 x 41 (80-pin package)
  - 4 x 32 or 3 x 33 (64-pin package)
- **ACMP** (analog comparator) — option to compare to internal reference voltage; output is software selectable to be driven to the input capture of TPM1 channel 0.
- **ADC** (analog-to-digital converter) — 8-channel, 12-bit with automatic compare function, asynchronous clock source, temperature sensor and internal bandgap reference channel. ADC is hardware triggerable using the RTI counter.
- **SCI** (serial communications interface) — available single-wire mode
- **SPI1** and **SPI2** — Two serial peripheral interface modules
- **KBI** — Two 8-pin keyboard interrupt modules with software selectable rising or falling edge detect
- **IIC** — Inter-integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; capable of higher baudrates with reduced loading
- **TPM1** and **TPM2** — Two timer/pulse-width modulators with selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels.

Input/Output

- Up to 24 general-purpose input/output (I/O) pins; includes two output-only pins and one input-only pin
- Software selectable pullups on ports when used as input. Selection is on an individual port bit basis.
- Software selectable slew rate control on ports when used as outputs (selection is on an individual port bit basis)
- Software selectable drive strength control on ports when used as outputs (selection is on an individual port bit basis)
- Internal pullup on $\overline{\text{RESET}}$ and IRQ pin to reduce customer system cost

MC9S08LC60 Series Data Sheet

Covers MC9S08LC60
MC9S08LC36

MC9S08LC60
Rev. 4
07/2007

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	02/2007	Initial advance information release.
2	05/2007	Incorporated changes to the LCDSupply Field Descriptions for the CPCADJ field, added a Run Idd chart, performed some minor formatting edits and fixed a couple of typos.
3	06/2007	Updated the Appendix with ESD tables, package info, and mechanical drawings.
4	07/2007	Updated the Appendix with ESD tables, package info, and mechanical drawings for the 80-pin LQFP package.

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Chapter 1
Device Overview

1.1 Introduction

MC9S08LC60 Series MCUs are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.2 Devices in the MC9S08LC60 Series

Table 1-1 lists the devices available in the MC9S08LC60 Series and summarizes the differences among them.

Table 1-1. Devices in the MC9S08LC60 Series

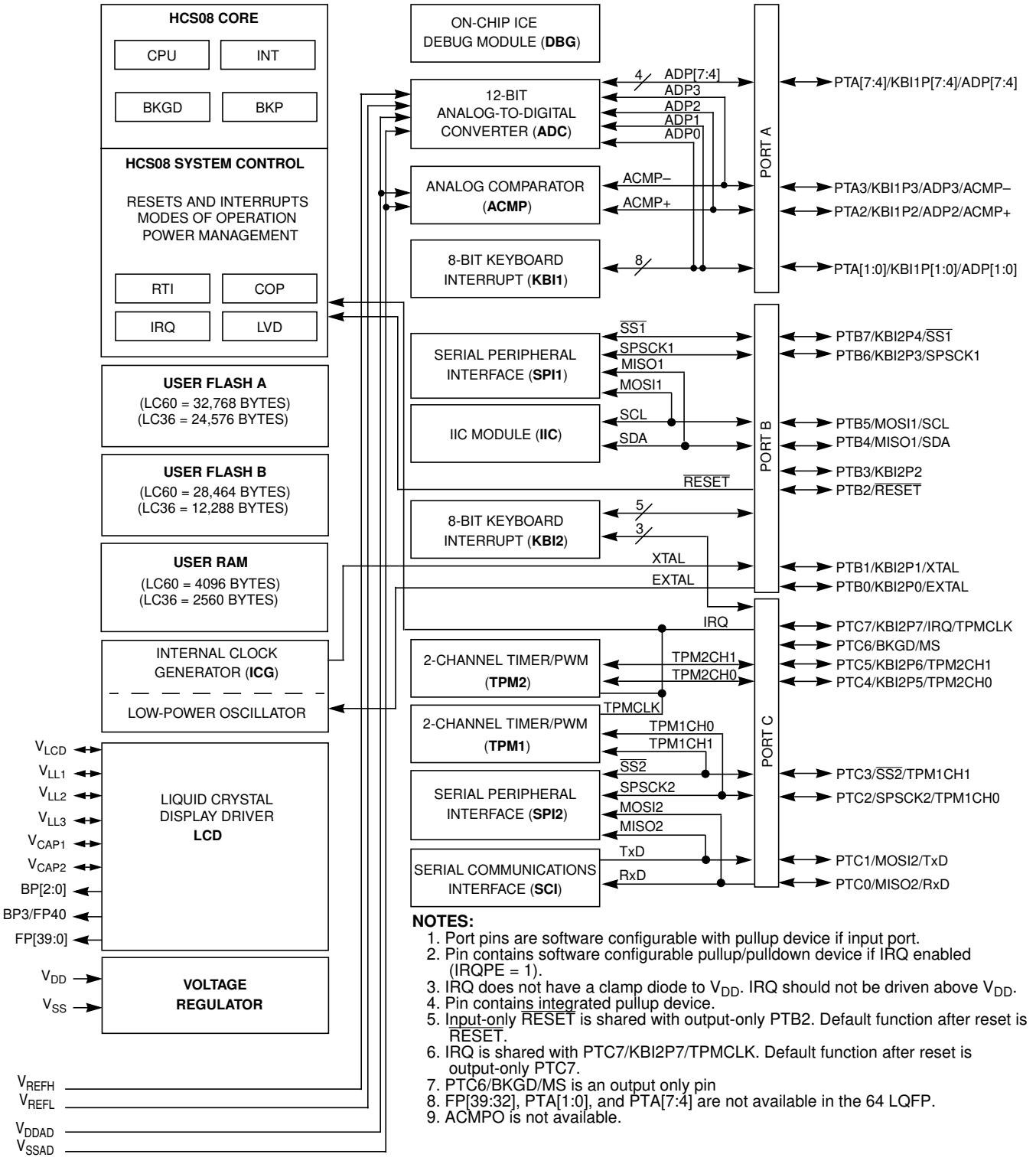
Device	FLASH A	FLASH B	RAM	Package
MC9S08LC60	32K	28K	4K	80 LQFP 64 LQFP
MC9S08LC36	24K	12K	2.5K	

Table 1-2. Package Options by Feature

Feature	Package	
	80-Pin	64-Pin
ACMP	yes	yes
ADC	8-ch	2-ch
IIC	yes	yes
IRQ	yes	yes
KBI1 KBI2	8 8	2 8
SCI	yes	yes
SPI1 SPI2	yes yes	yes yes
TPM1 TPM2	2-ch 2-ch	2-ch 2-ch
Shared I/O pins (max)	24 - I/O 2 - Output only 1- Input only	18 - I/O 2 - Output only 1- Input only
LCD	4x40 3x41	4x32 3x33

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC9S08LC60 Series MCUs.



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1).
3. IRQ does not have a clamp diode to V_{DD}. IRQ should not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. Input-only RESET is shared with output-only PTB2. Default function after reset is RESET.
6. IRQ is shared with PTC7/KBI2P7/TPMCLK. Default function after reset is output-only PTC7.
7. PTC6/BKGD/MS is an output only pin
8. FP[39:32], PTA[1:0], and PTA[7:4] are not available in the 64 LQFP.
9. ACMPO is not available.

Figure 1-1. MC9S08LC60 Series Block Diagram

Table 1-3 lists the functional versions of the on-chip modules.

Table 1-3. Module Versions

Module	Version
Analog Comparator (ACMP)	2
Analog-to-Digital Converter (ADC)	1
Internal Clock Generator (ICG)	4
Inter-Integrated Circuit (IIC)	1
Keyboard Interrupt (KBI)	2
Serial Communications Interface (SCI)	3
Serial Peripheral Interface (SPI)	3
Timer Pulse-Width Modulator (TPM)	2
Liquid Crystal Display Module (LCD)	1
Central Processing Unit (CPU)	2

1.4 System Clock Distribution

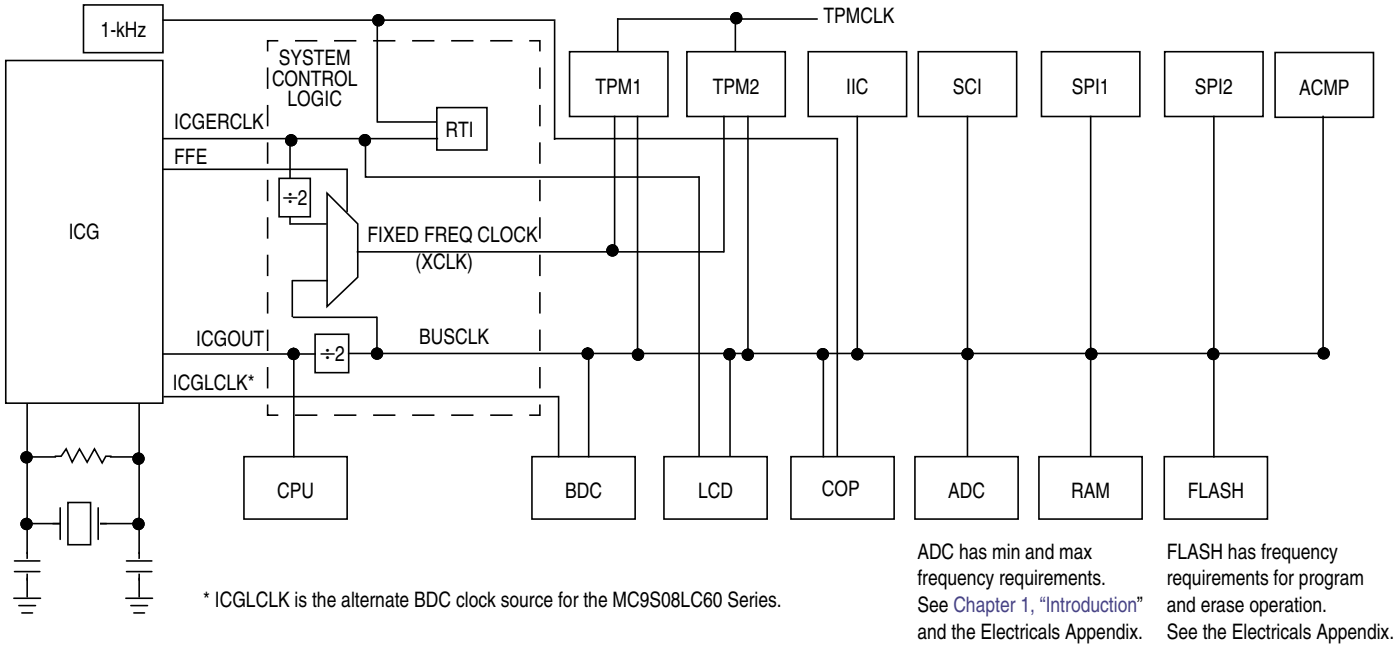


Figure 1-2. System Clock Distribution Diagram

Some of the modules inside the MCU have clock source choices. Figure 1-2 shows a simplified clock connection diagram. The ICG supplies the clock sources:

- ICGOUT is an output of the ICG module. It is one of the following:
  - The external crystal oscillator
  - An external clock source
  - The output of the digitally-controlled oscillator (DCO) in the frequency-locked loop sub-module