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Freescale Semiconductor, Inc.
Data Sheet: Technical Data

Document Number: MC9S08LG32
Rev. 10, 04/2015

MC9S08LG32 Series with Addendum Covers: MC9S08LG32 and MC9S08LG16

Rev. 10 of the MC9S08LG32 Series data sheet (covering MC9S08LG32 and MC9S08LG16) has two parts:

- The addendum to revision 9 of the data sheet, immediately following this cover page.
- Revision 9 of the data sheet, following the addendum. The changes described in the addendum have not been implemented in the specified pages.

Document Number: MC9S08LG32AD
Rev. 0, 04/2015

Addendum to Rev. 9 of the MC9S08LG32 Series Covers: MC9S08LG32 and MC9S08LG16

This addendum identifies changes to Rev. 9 of the MC9S08LG32 Series data sheet (covering MC9S08LG32 and MC9S08LG16). The changes described in this addendum have not been implemented in the specified pages.

1 Add min values for I_{IC} (DC injection current)

Location:	Table 8. DC Characteristics, Page 14

In Table 8, "DC Characteristics," add min values for I_{IC} (row number 14) as follows:

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
14	D	DC injection current [5, 6, 7] $V_{IN} < V_{SS}$ (min) $V_{IN} > V_{DD}$ (max)	Single pin limit	I_{IC}	**-0.2**	—	2	mA
			Total MCU limit, includes sum of all stressed pins		**-5**	—	25	mA

2 Change the max value of t_{LPO} (low power oscillator period)

Location:	Table 14. Control Timing, Page 29

In Table 14, "Control Timing," change the max value of t_{LPO} (row number 2) from 1300 to 1500 µs.

Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08LG32
Rev. 9 , 09/2011

MC9S08LG32 Series

Covers: MC9S08LG32 and MC9S08LG16

MC9S08LG32

80-LQFP
Case 917A
14 mm × 14 mm

64-LQFP
Case 840F
10 mm × 10 mm

48-LQFP
Case 932
7 mm × 7mm

Features

- 8-bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 5.5 V to 2.7 V across temperature range of –40 °C to 85 °C and –40 °C to 105 °C
  - HCS08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - 32 KB or 18 KB dual array flash; read/program/erase over full operating voltage and temperature
  - 1984 byte random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low-power stop modes (stop2 and stop3)
  - Reduced-power wait mode
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Low power On-Chip crystal oscillator (XOSC) that can be used in low-power modes to provide accurate clock source to real time counter and LCD controller
  - 100 µs typical wakeup time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 20 MHz.
- System Protection
  - COP reset with option to run from dedicated 1 kHz internal clock or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash and RAM protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging and plus two more breakpoints in On-Chip debug module
  - On-Chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — Up to 4 × 41 or 8 × 37 LCD driver with internal charge pump.
  - **ADC** — Up to 16-channel, 12-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel, runs in stop3 and can wake up the system, fully functional from 5.5 V to 2.7 V
  - **SCI** — Full duplex non-return to zero (NRZ), LIN master extended break generation, LIN slave extended break detection, wakeup on active edge
  - **SPI** — Full-duplex or single-wire bidirectional, double-buffered transmit and receive, master or slave mode, MSB-first or LSB-first shifting
  - **IIC** — With up to 100 kbps with maximum bus loading, multi-master operation, programmable slave address, interrupt driven byte-by-byte data transfer, supports broadcast mode and 10-bit addressing
  - **TPMx** — One 6 channel and one 2 channel, selectable input capture, output compare, or buffered edge or center-aligned PWM on each channel
  - **MTIM** — 8-bit counter with match register,, four clock sources with prescaler dividers, can be used for periodic wakeup
  - **RTC** — 8-bit modulus counter with binary or decimal based prescaler, three clock sources including one external source, can be used for time base, calendar, or task scheduling functions
  - **KBI** — One keyboard control module capable of supporting 8 × 8 keyboard matrix
  - **IRQ** — External pin for wakeup from low-power modes
- Input/Output
  - 39, 53, or 69 GPIOs
  - 8 KBI and 1 IRQ interrupt with selectable polarity
  - Hysteresis and configurable pullup device on all input pins, configurable slew rate and drive strength on all output pins.
- Package Options
  - 48-pin LQFP, 64-pin LQFP, and 80-pin LQFP

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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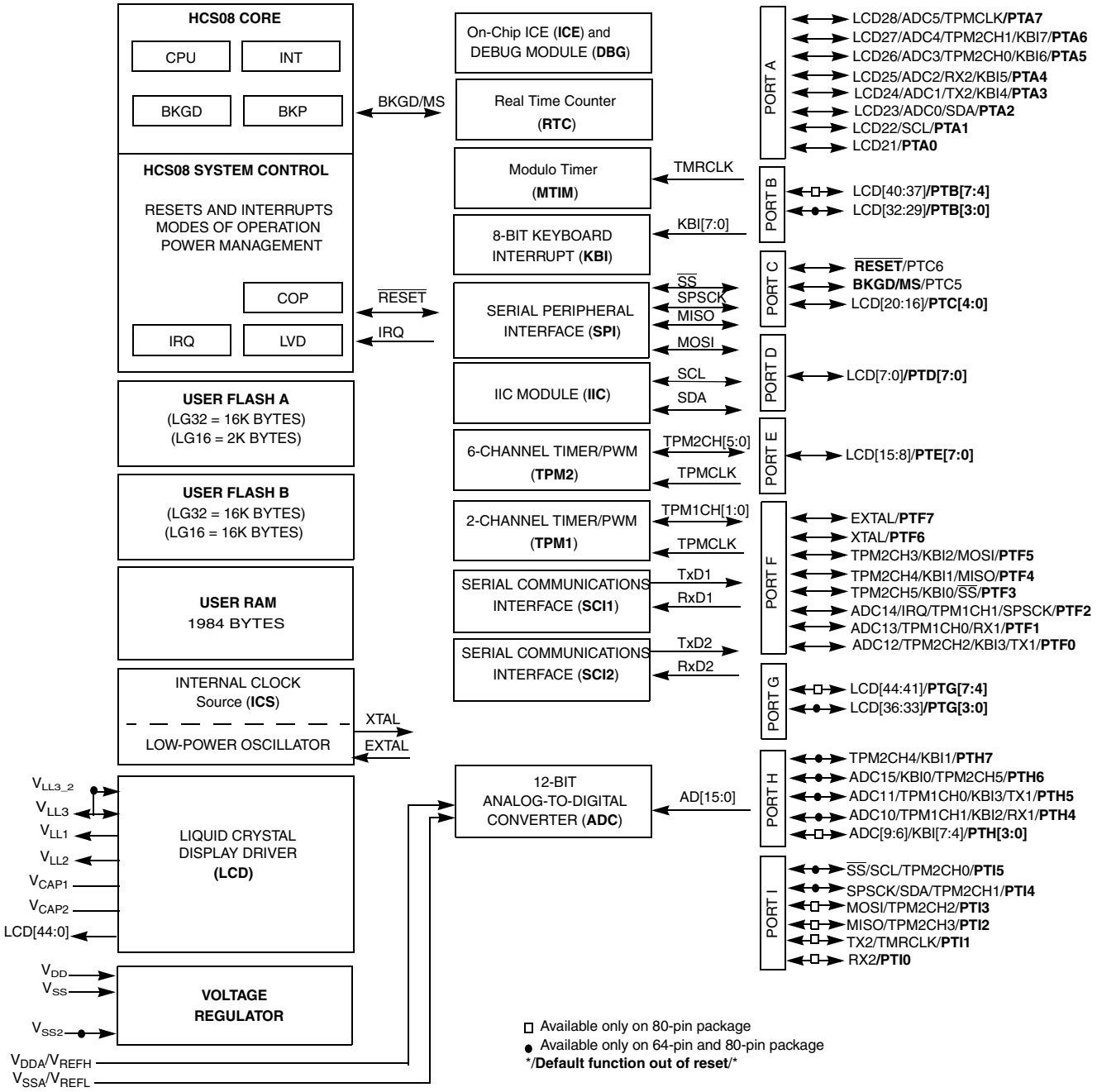

Figure 1. MC9S08LG32 Series Block Diagram

Table 1. MC9S08LG32 Series Features by MCU and Package

Feature	MC9S08LG32			MC9S08LG16	
Flash size (bytes)	32,768			18,432	
RAM size (bytes)	1984				
Pin quantity	80	64	48	64	48
ADC	16 ch	12 ch	9 ch	12 ch	9 ch
LCD	8 x 37 4 x 41	8 x 29 4 x 33	8 x 21 4 x 25	8 x 29 4 x 33	8 x 21 4 x 25
ICE + DBG	yes				
ICS	yes				
IIC	yes				
IRQ	yes				
KBI	8 pin				
GPIOs	69	53	39	53	39
RTC	yes				
MTIM	yes				
SCI1	yes				
SCI2	yes				
SPI	yes				
TPM1 channels	2				
TPM2 channels	6				
XOSC	yes				

1 Pin Assignments

This section shows the pin assignments for the MC9S08LG32 series devices. The priority of functions on a pin is in ascending order from left to right and bottom to top. Another view of pinouts and function priority is given in Table 2.

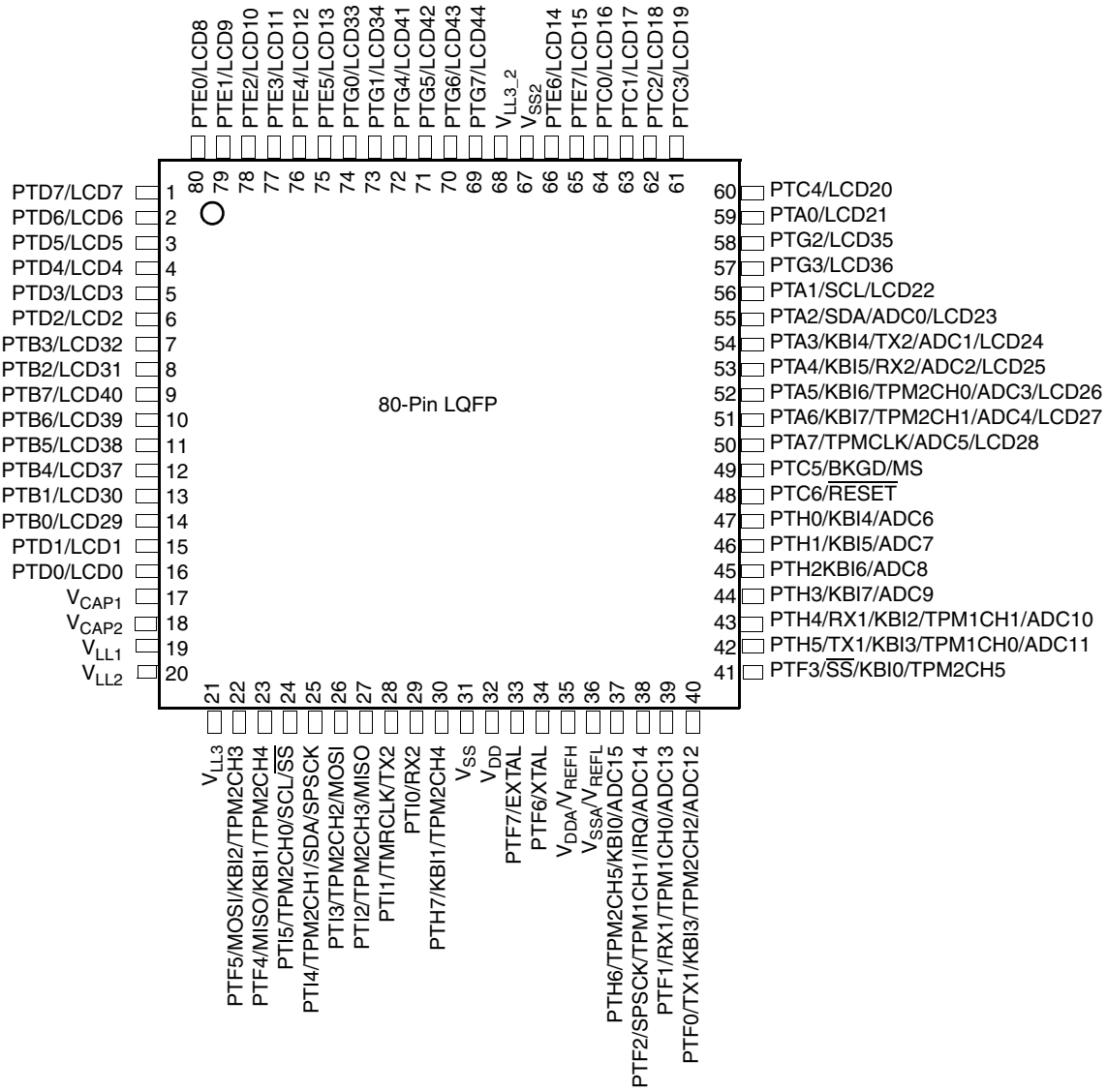

Figure 2. 80-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

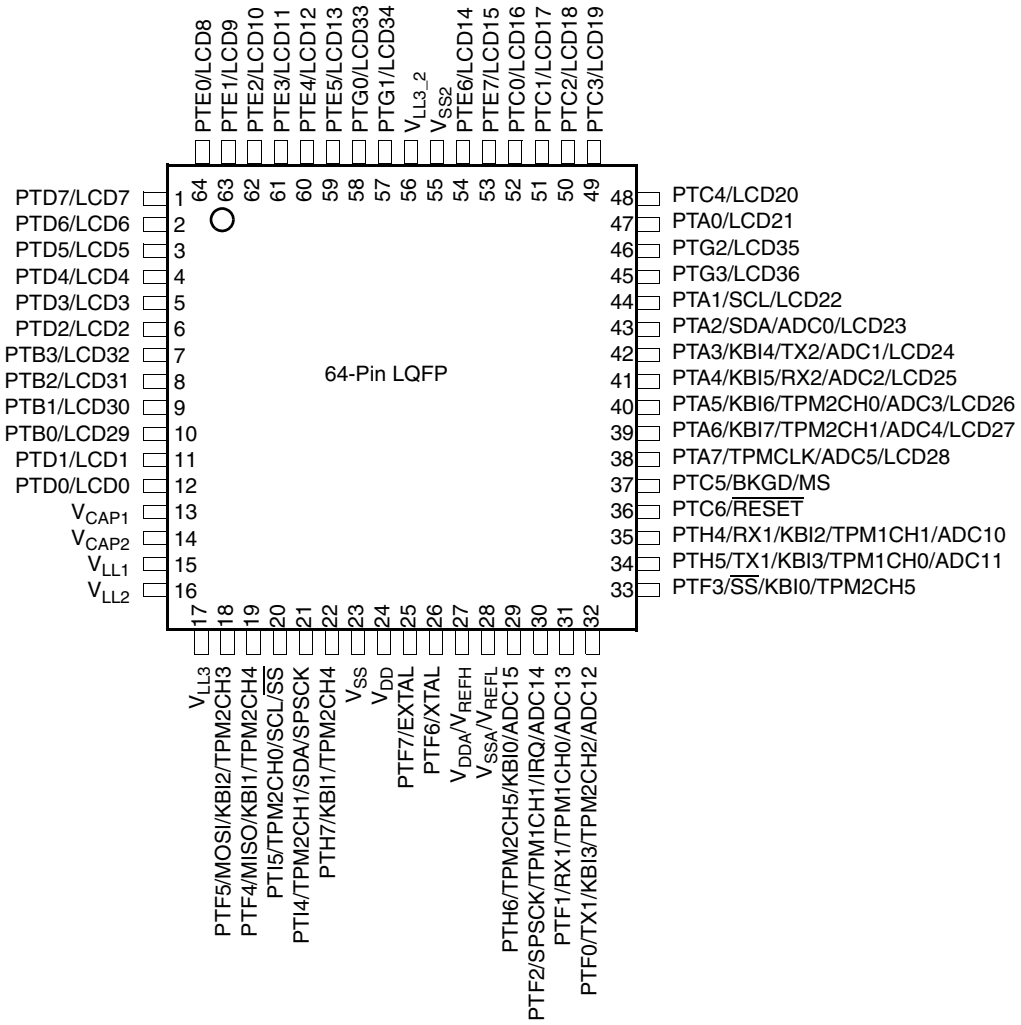

Figure 3. 64-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

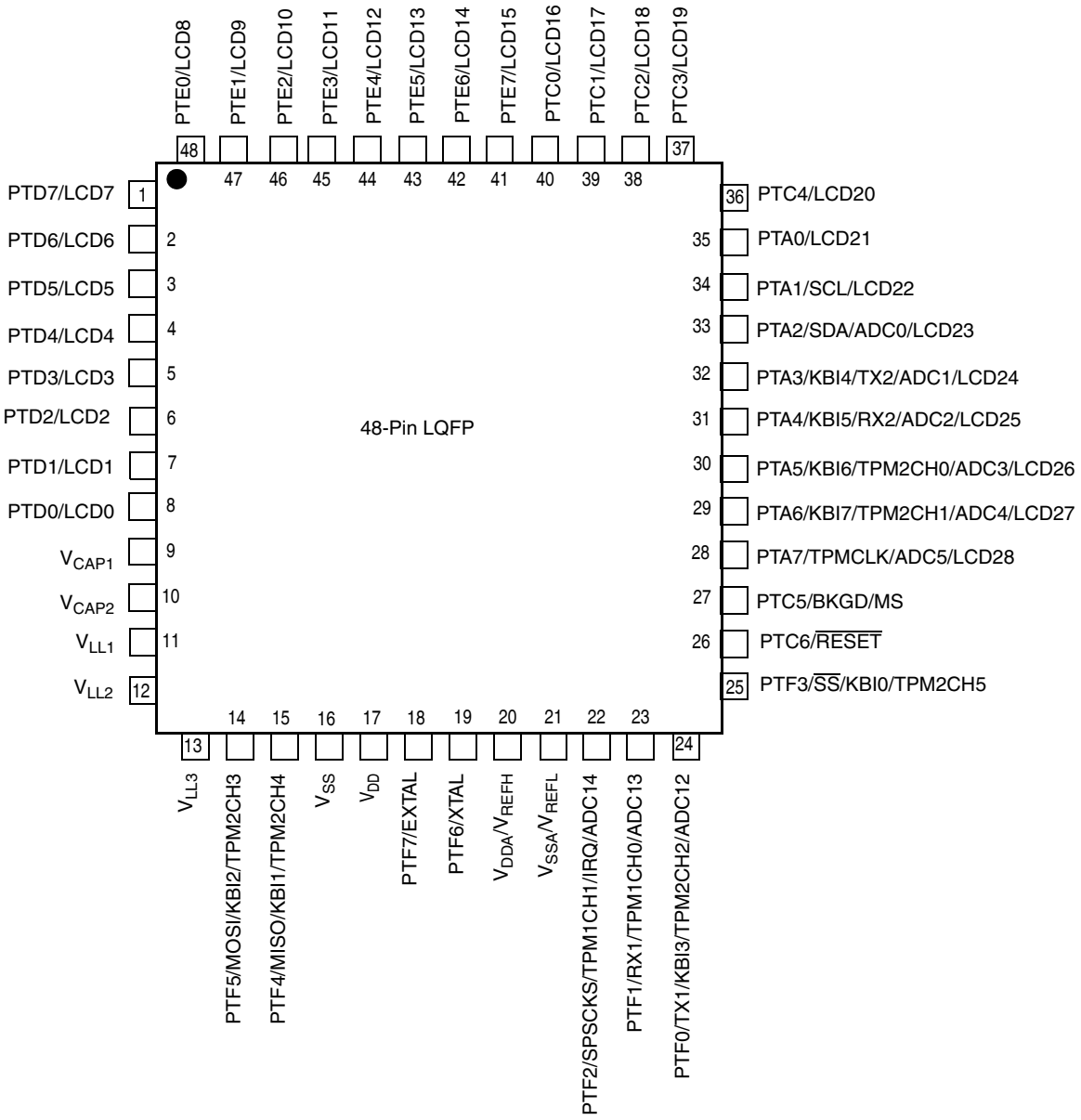

Figure 4. 48-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Table 2. Pin Availability by Package Pin-Count

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	PTD7	LCD7	—	—	—
2	2	2	PTD6	LCD6	—	—	—
3	3	3	PTD5	LCD5	—	—	—
4	4	4	PTD4	LCD4	—	—	—
5	5	5	PTD3	LCD3	—	—	—
6	6	6	PTD2	LCD2	—	—	—
7	7	—	PTB3	LCD32	—	—	—
8	8	—	PTB2	LCD31	—	—	—
9	—	—	PTB7	LCD40	—	—	—
10	—	—	PTB6	LCD39	—	—	—
11	—	—	PTB5	LCD38	—	—	—
12	—	—	PTB4	LCD37	—	—	—
13	9	—	PTB1	LCD30	—	—	—
14	10	—	PTB0	LCD29	—	—	—
15	11	7	PTD1	LCD1	—	—	—
16	12	8	PTD0	LCD0	—	—	—
17	13	9	V_{CAP1}	—	—	—	—
18	14	10	V_{CAP2}	—	—	—	—
19	15	11	V_{LL1}	—	—	—	—
20	16	12	V_{LL2}	—	—	—	—
21	17	13	V_{LL3}	—	—	—	—
22	18	14	PTF5	MOSI	KBI2	TPM2CH3	—
23	19	15	PTF4	MISO	KBI1	TPM2CH4	—
24	20	—	PTI5	TPM2CH0	SCL	$\overline{SS}$	—
25	21	—	PTI4	TPM2CH1	SDA	SPSCK	—
26	—	—	PTI3	TPM2CH2	MOSI	—	—
27	—	—	PTI2	TPM2CH3	MISO	—	—
28	—	—	PTI1	TMRCLK	TX2	—	—
29	—	—	PTI0	RX2	—	—	—
30	22	—	PTH7	KBI1	TPM2CH4	—	—
31	23	16	V_{SS}	—	—	—	—
32	24	17	V_{DD}	—	—	—	—
33	25	18	PTF7	EXTAL	—	—	—
34	26	19	PTF6	XTAL	—	—	—
35	27	20	V_{DDA}	V_{REFH}	—	—	—
36	28	21	V_{SSA}	V_{REFL}	—	—	—
37	29	—	PTH6	TPM2CH5	KBI0	ADC15	—
38	30	22	PTF2	SPSCK	TPM1CH1	IRQ	ADC14

Table 2. Pin Availability by Package Pin-Count (continued)

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
39	31	23	PTF1	RX1	TPM1CH0	ADC13	—
40	32	24	PTF0	TX1	KBI3	TPM2CH2	ADC12
41	33	25	PTF3	$\overline{SS}$	KBI0	TPM2CH5	—
42	34	—	PTH5	TX1	KBI3	TPM1CH0	ADC11
43	35	—	PTH4	RX1	KBI2	TPM1CH1	ADC10
44	—	—	PTH3	KBI7	ADC9	—	—
45	—	—	PTH2	KBI6	ADC8	—	—
46	—	—	PTH1	KBI5	ADC7	—	—
47	—	—	PTH0	KBI4	ADC6	—	—
48	36	26	PTC6	$\overline{RESET}$	—	—	—
49	37	27	PTC5	BKGD/MS	—	—	—
50	38	28	PTA7	TPMCLK	ADC5	LCD28	—
51	39	29	PTA6	KBI7	TPM2CH1	ADC4	LCD27
52	40	30	PTA5	KBI6	TPM2CH0	ADC3	LCD26
53	41	31	PTA4	KBI5	RX2	ADC2	LCD25
54	42	32	PTA3	KBI4	TX2	ADC1	LCD24
55	43	33	PTA2	SDA	ADC0	LCD23	—
56	44	34	PTA1	SCL	LCD22	—	—
57	45	—	PTG3	LCD36	—	—	—
58	46	—	PTG2	LCD35	—	—	—
59	47	35	PTA0	LCD21	—	—	—
60	48	36	PTC4	LCD20	—	—	—
61	49	37	PTC3	LCD19	—	—	—
62	50	38	PTC2	LCD18	—	—	—
63	51	39	PTC1	LCD17	—	—	—
64	52	40	PTC0	LCD16	—	—	—
65	53	41	PTE7	LCD15	—	—	—
66	54	42	PTE6	LCD14	—	—	—
67	55	—	V_{SS2}	—	—	—	—
68	56	—	V_{LL3_2}	—	—	—	—
69	—	—	PTG7	LCD44	—	—	—
70	—	—	PTG6	LCD43	—	—	—
71	—	—	PTG5	LCD42	—	—	—
72	—	—	PTG4	LCD41	—	—	—
73	57	—	PTG1	LCD34	—	—	—
74	58	—	PTG0	LCD33	—	—	—
75	59	43	PTE5	LCD13	—	—	—
76	60	44	PTE4	LCD12	—	—	—

Table 2. Pin Availability by Package Pin-Count (continued)

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
77	61	45	PTE3	LCD11	—	—	—
78	62	46	PTE2	LCD10	—	—	—
79	63	47	PTE1	LCD9	—	—	—
80	64	48	PTE0	LCD8	—	—	—

2 Electrical Characteristics

2.1 Introduction

This section contains electrical and timing specifications for the MC9S08LG32 series of microcontrollers available at the time of publication.

2.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry that protects against damage due to high static voltage or electrical fields. However, it is advised that normal precautions should be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25 ±2	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages and use the largest of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in an external power supply going out of regulation. Ensure that the external V_{DD} load will shunt current greater than maximum injection current, this will be of greater risk when the MCU is not consuming power. For instance, if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

2.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in On-Chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to +105	°C
Maximum junction temperature	T_J	125	°C
Thermal resistance Single-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	 61 71 80	°C/W
Thermal resistance Four-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	 48 52 56	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for automotive grade integrated circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 6. ESD and Latch-Up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body Model	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	2500	—	V
2	Charge device model (CDM)	V_{CDM}	750	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	—	Operating Voltage	—	2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA	V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8	 — —	 — —	V
		Output high voltage — High Drive (PTxDSn = 1) V 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA		 V_{DD} – 0.8 V_{DD} – 0.8	 — —	 — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA	V_{OL}	—	 — —	 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA			 — —	 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5 V 3 V	I_{OHT}	—	—	 100 60	mA
5	C	Output high current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	—	—	 100 60	mA
6	P	Bandgap voltage reference	V_{BG}	—	1.225	—	V
7	P	Input high voltage; all digital inputs	V_{IH}	0.65 x V_{DD}	—	—	V
8	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 x V_{DD}	V
9	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}	—	—	mV
10	P	Input leakage current; input only pins[2] V_{In} = V_{DD} or V_{SS}	$\lvert I_{In} \rvert$	—	0.1	1	μA
11	P	High impedence (off-state) leakage current V_{In} = V_{DD} or V_{SS}	$\lvert I_{OZ} \rvert$	—	0.1	1	μA
12	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
13	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
14	D	DC injection current [5, 6, 7] $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	Single pin limit	I_{IC}	—	—	2	mA
			Total MCU limit, includes sum of all stressed pins		—	—	25	mA
15	C	Input Capacitance, all non-supply pins		C_{In}	—	—	8	pF
16	C	RAM retention voltage		V_{RAM}	2	—	—	V
17	P	POR rearm voltage		V_{POR}	0.9	1.4	2.0	V
18	D	POR rearm time		t_{POR}	10	—	—	µs
19	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising		V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
20	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising		V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
21	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising		V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
22	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising		V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
23	P	Low-voltage warning threshold — low range 1 V_{DD} falling V_{DD} rising		V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
24	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising		V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
25	P	Low-voltage inhibit reset/recover hysteresis 5 V 3 V		V_{hys}	—	 100 60	—	mV

1 Typical values are measured at 25 °C. Characterized, not tested

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins, except for PTC6 are internally clamped to V_{SS} and V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. For instance, if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

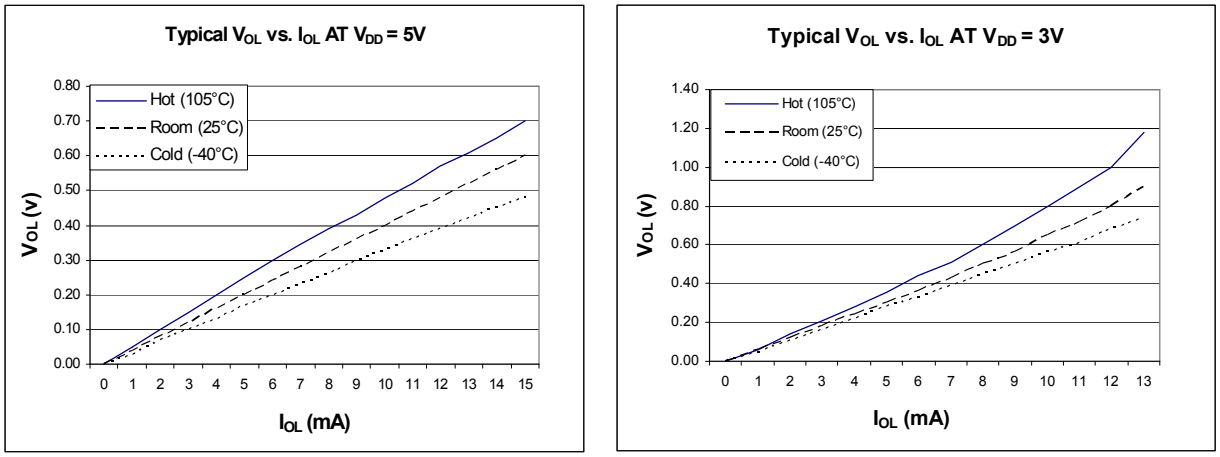

Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)

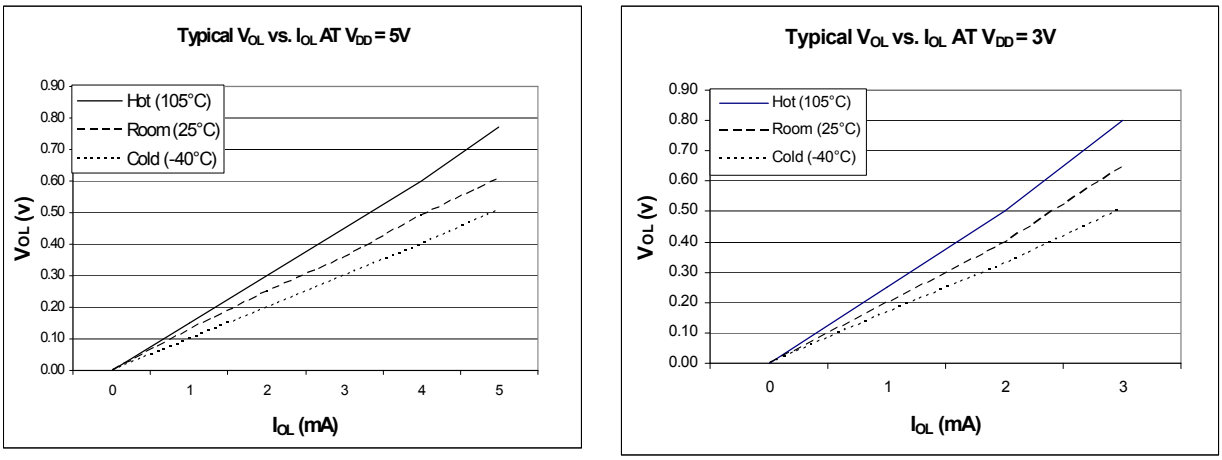

Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)

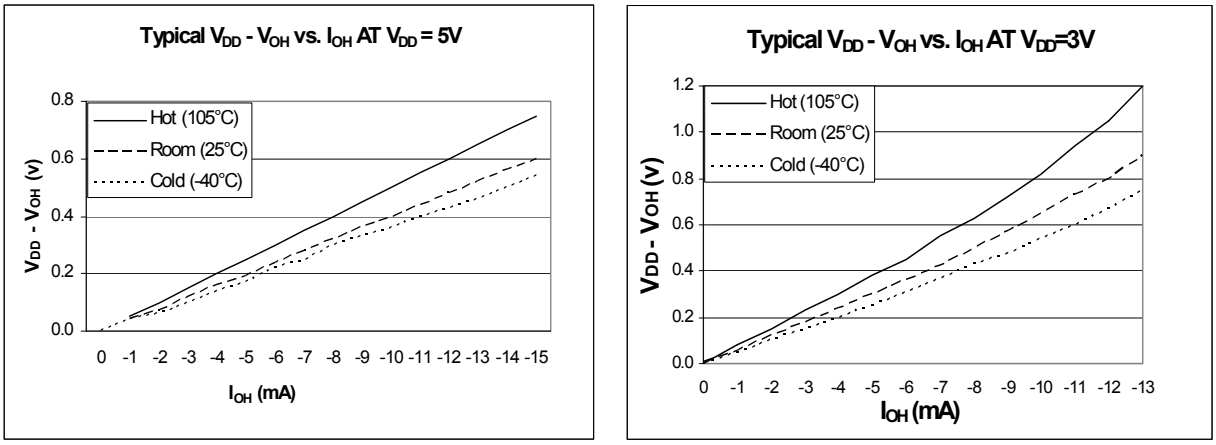

Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)

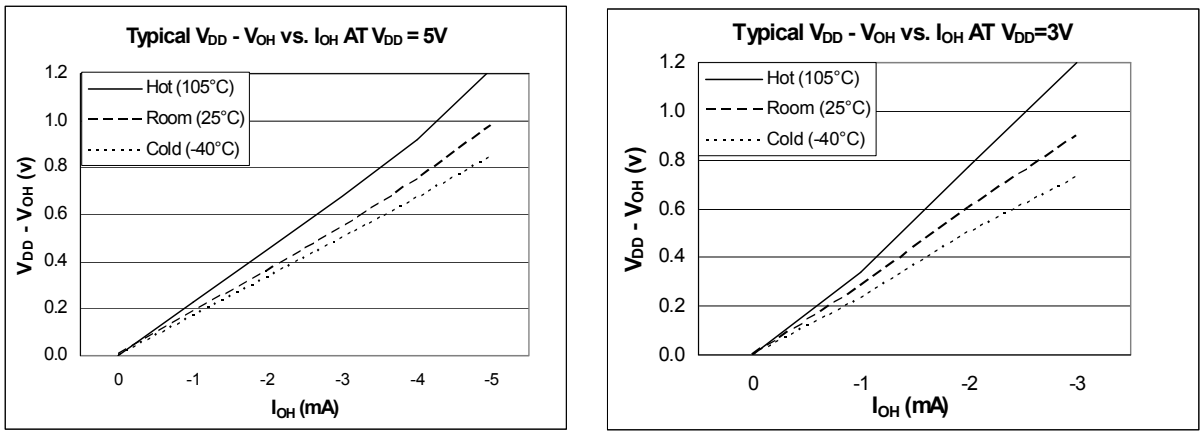

Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)

2.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	16.38	27.85	mA	–40 °C to 85 °C
	C						28.05		–40 °C to105 °C
	C			1 MHz		1.67	2.84		–40 °C to 85 °C
	C						2.87		–40 °C to105 °C
	P			20 MHz	5	16.55	28.14	mA	–40 °C to 85 °C
	P						28.35		–40 °C to105 °C
	C			1 MHz		1.77	3.01		–40 °C to 85 °C
	C						3.05		–40 °C to105 °C
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	11.9	20.25	mA	–40 °C to 85 °C
	T						21.72		–40 °C to105 °C
	T			1 MHz		1.16	1.95		–40 °C to 85 °C
	T						1.98		–40 °C to105 °C
	T			20 MHz	5	12.68	21.56	mA	–40 °C to 85 °C
	T						23.12		–40 °C to105 °C
	T			1 MHz		1.4	2.39		–40 °C to 85 °C
	T						2.41		–40 °C to105 °C
3	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	7.9	13.42	mA	–40 °C to 85 °C
	T						13.59		–40 °C to105 °C
	T			1 MHz		0.88	1.49		–40 °C to 85 °C
	T						1.51		–40 °C to105 °C
	P			20 MHz	5	8.13	13.81	mA	–40 °C to 85 °C
	P						13.98		–40 °C to105 °C
	T			1 MHz		1.12	1.91		–40 °C to 85 °C
	T						1.94		–40 °C to105 °C
4	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3	1.1	16.0	µA	–40 °C to 85 °C
	C						39.0		–40 °C to105 °C
	P				5	1.2	18.7	µA	–40 °C to 85 °C
	P						46.1		–40 °C to105 °C
5	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	1.2	22.4	µA	–40 °C to 85 °C
	C						56.2		–40 °C to105 °C
	P				5	1.32	25.5	µA	–40 °C to 85 °C
	P						63.9		–40 °C to105 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
6	T	Stop2 adders:	RTC using LPO	—	n/a	3	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.25	—	µA	
			LCD[2] with rbias (Low Gain)				1.2[3]	—		
			LCD[2] with rbias (High Gain)				18[4]	—		
			LCD[2] with Cpump				4.05[3]	—		–40 °C to 85 °C
			RTC using LPO			5	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.22	—	µA	
			LCD[2] with rbias (Low Gain)				1.5[3]	—		
			LCD[2] with rbias (High Gain)				32[4]	—		
			LCD[2] with Cpump				7.12[3]	—		–40 °C to 85 °C
7	T	Stop3 adders:	RTC using LPO	—	n/a	3	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.75	—	µA	
			LCD[2] with rbias (Low Gain)				1.2[3]	—		
			LCD[2] with rbias (High Gain)				18[4]	—		
			LCD[2] with Cpump				4.35[3]	—		–40 °C to 85 °C
			RTC using LPO			5	230	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.74	—	µA	
			LCD[2] with rbias (Low Gain)				1.5[3]	—		
			LCD[2] with rbias (High Gain)				32[4]	—		
			LCD[2] with Cpump				7.49[3]	—		–40 °C to 85 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
8	T	Stop3 adders:	EREFSTEN = 1	—	n/a	3	4.58	—	µA	–40 °C to 105 °C
			IREFSTEN = 1				71.7	—		
			LVD				94.35	—		
			EREFSTEN = 1			5	4.61	—	µA	
			IREFSTEN = 1				71.69	—		
			LVD				107.34	—		

1 Typical values are measured at 25 °C. Characterized, not tested.

2 LCD configured for Charge Pump Enabled V_{LL3} connected to V_{DD}.

3 This does not include current required for 32 kHz oscillator.

4 This is the maximum current when all LCD inputs/outputs are used.

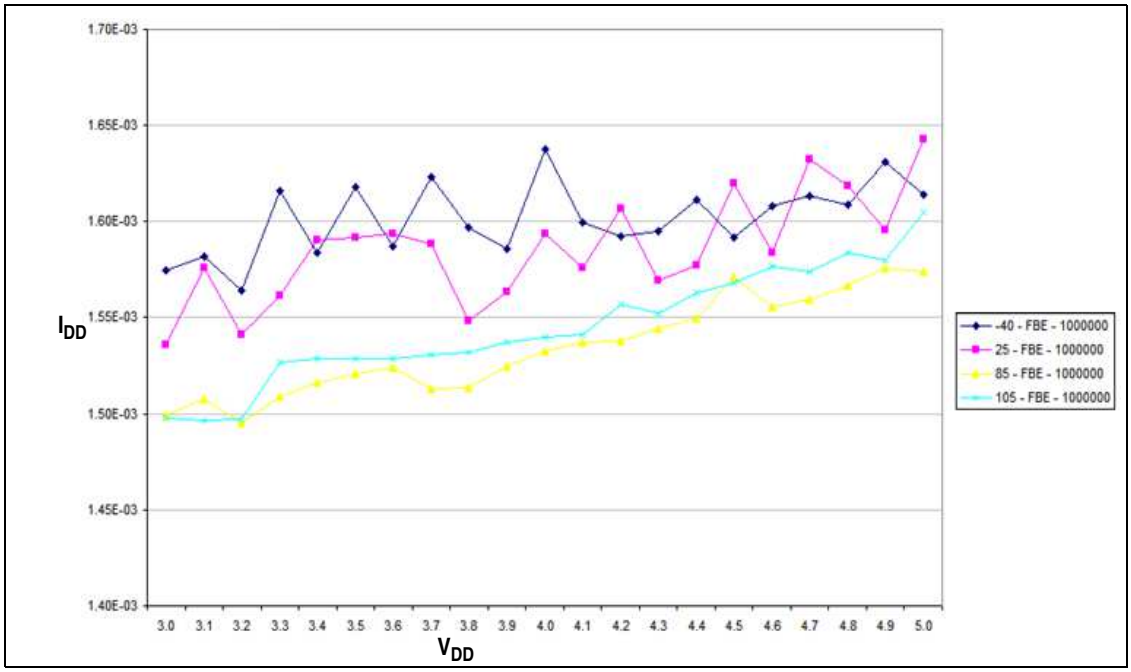

Figure 9. Typical Run I_{DD} for FBE Mode at 1 MHz

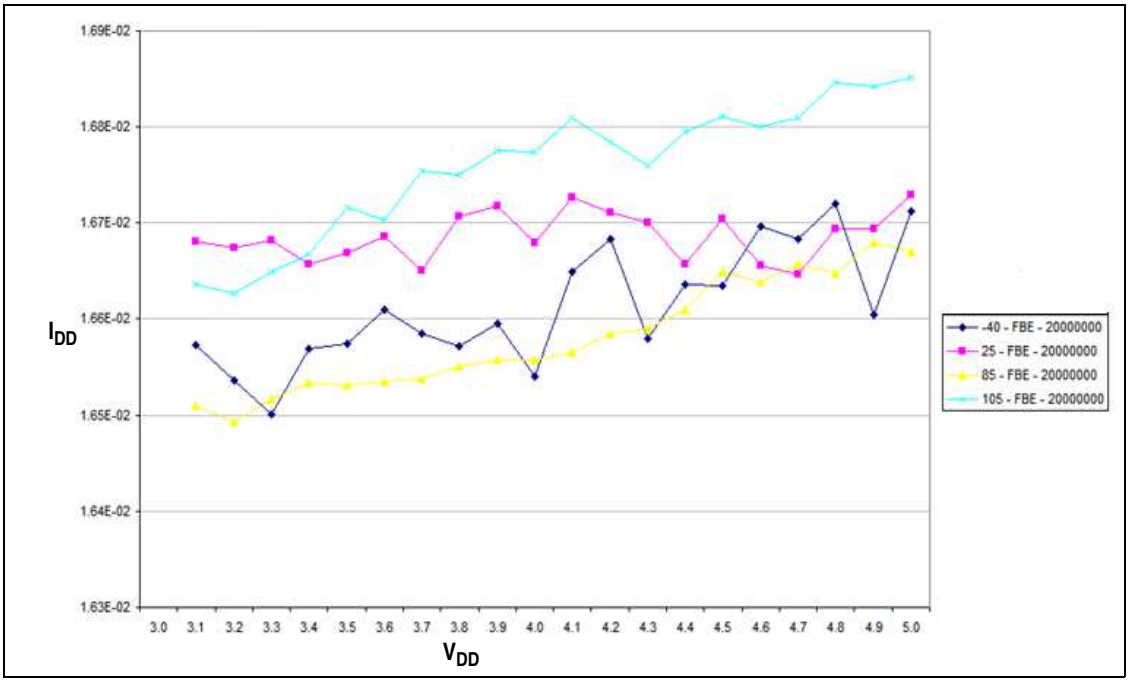

Figure 10. Typical Run I_{DD} for FBE Mode at 20 MHz

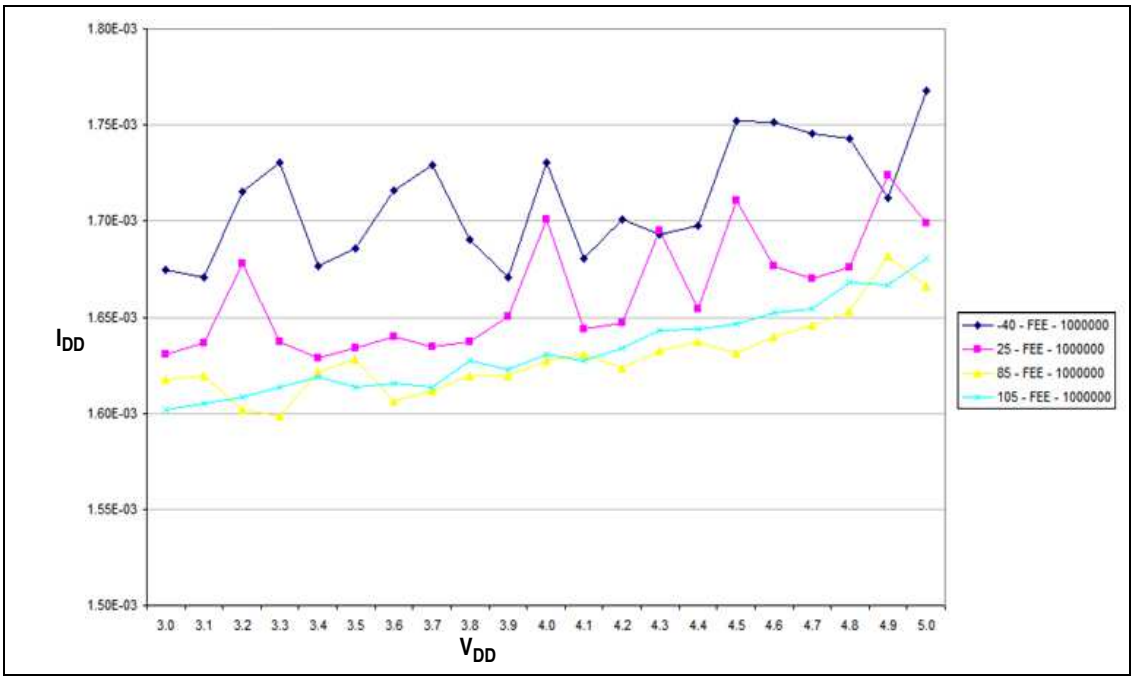

Figure 11. Typical Run I_{DD} for FEE Mode at 1 MHz

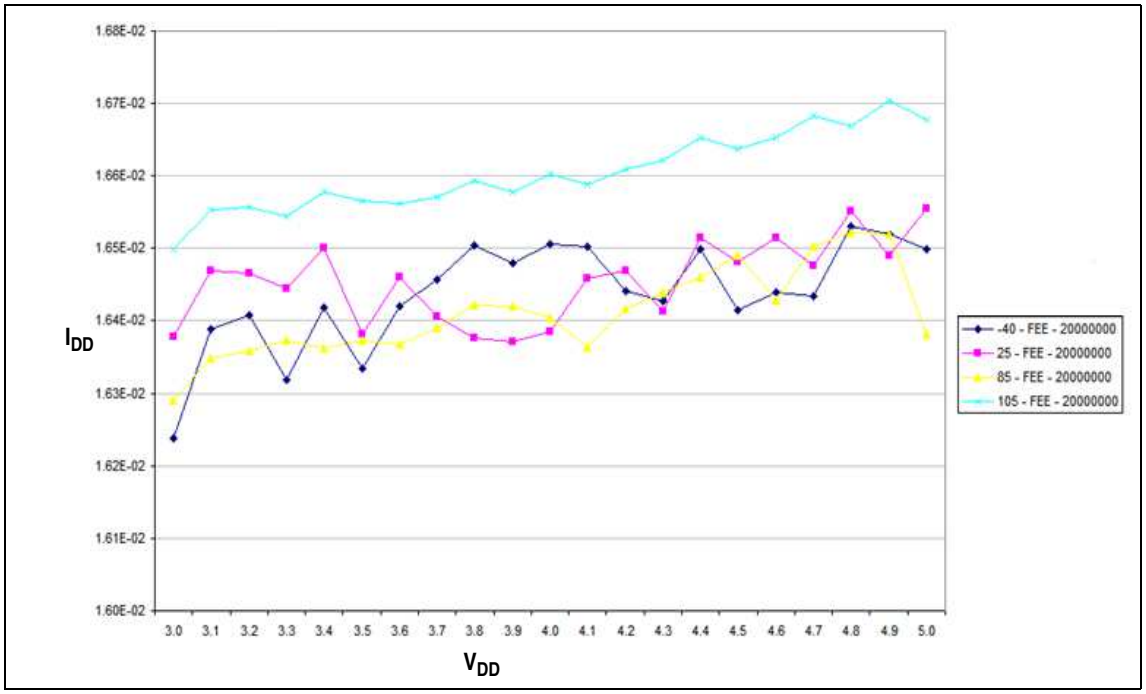

Figure 12. Typical Run I_{DD} for FEE Mode at 20 MHz

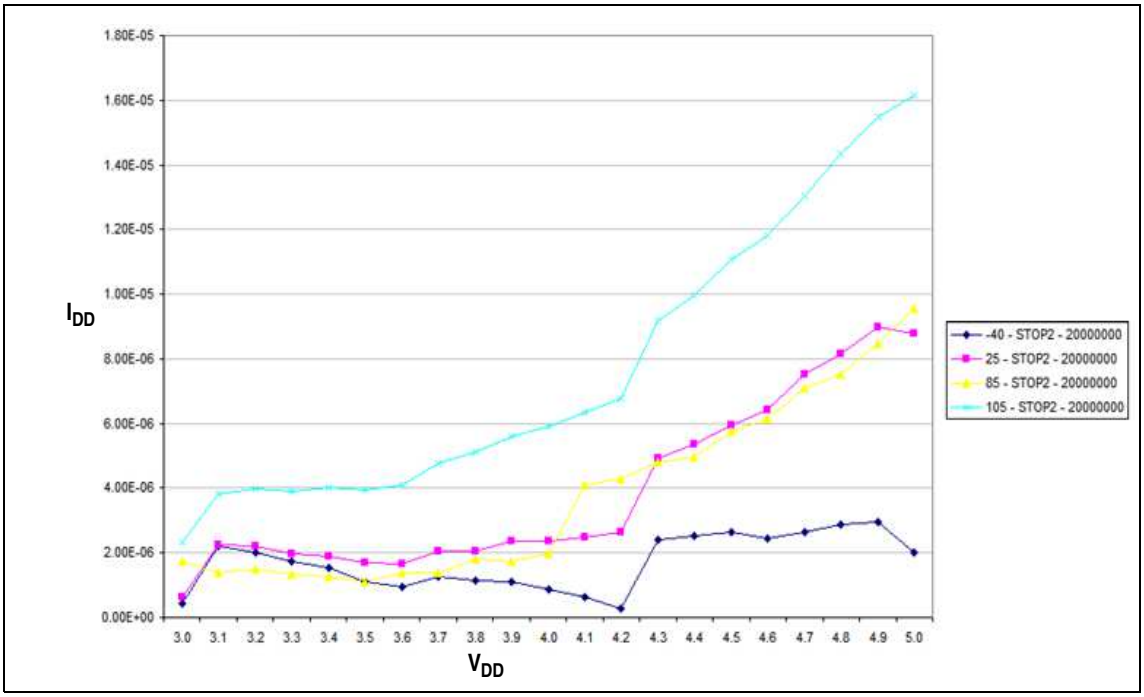

Figure 13. Typical Stop2 I_{DD}

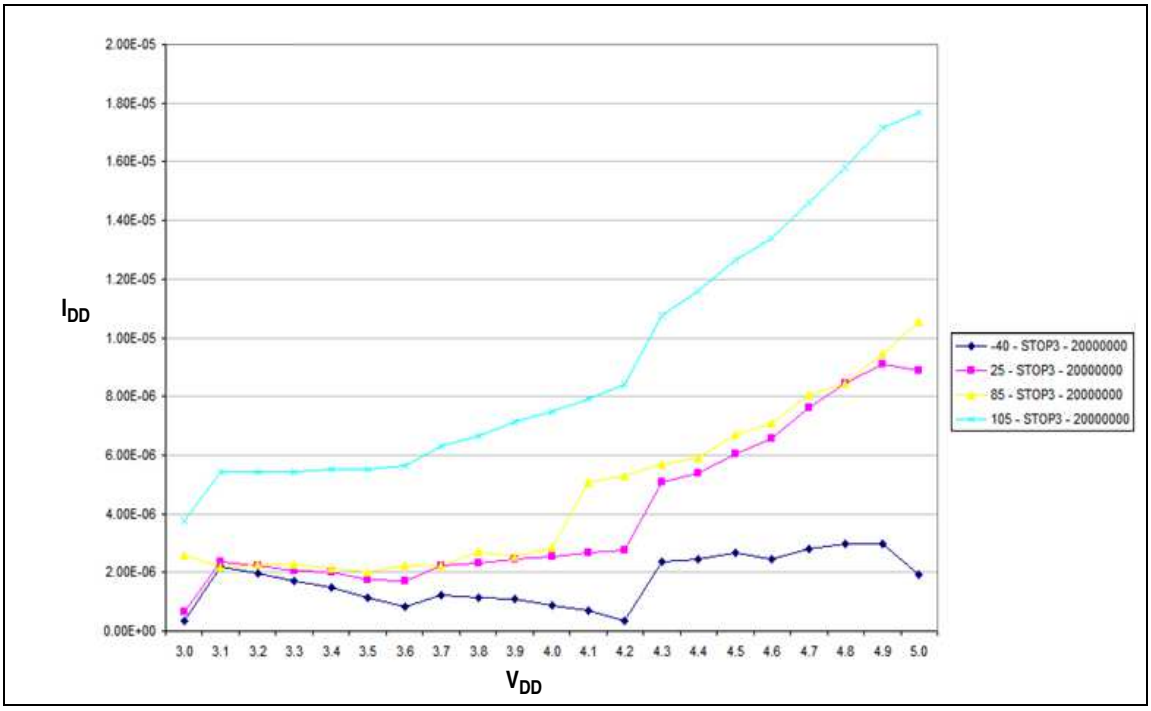

Figure 14. Typical Stop3 I_{DD}

2.8 External Oscillator (XOSC) Characteristics

Table 10. Oscillator Electrical Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	D	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) • Low range (RANGE = 0) • High range (RANGE = 1) FEE or FBE mode[2] • High range (RANGE = 1, HGO = 1) BLPE mode • High range (RANGE = 1, HGO = 0) BLPE mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			

Table 10. Oscillator Electrical Specifications (Temperature Range = –40 °C to 105 °C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
3	D	Feedback resistor • Low range (32 kHz to 100 kHz) • High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	MΩ
4	D	Series resistor • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1)	R_S		 0 100		kΩ
5	D	Series resistor • High range, low gain (RANGE = 1, HGO = 0) • High range, high gain (RANGE = 1, HGO = 1) ≥8 MHz 4 MHz 1 MHz	R_S	 — — —	 0 0 0	 0 10 20	kΩ
6	T	Crystal start-up time[3, 4] • Low range (HGO = 0) • Low range (HGO = 1) • High range (HG0 = 0)[5] • High range (HG0 = 1)[5]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 500 3570 4 4	 — — — —	ms
7	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) • FEE or FBE mode[2] • BLPE mode	f_{extal}	 0.03125 0	 — —	 5 40	MHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 4 MHz crystal

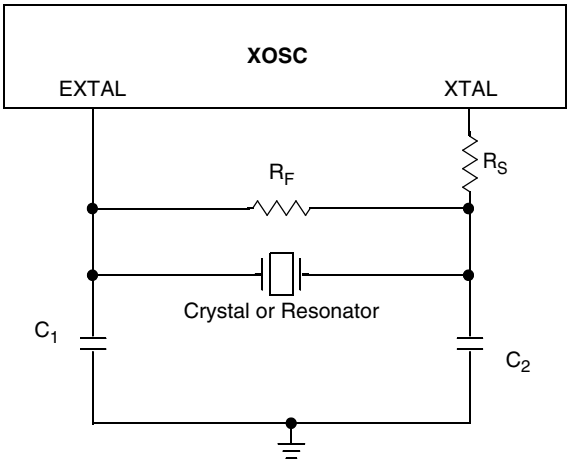

Figure 15. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain