



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



MC9S08PT60 Reference Manual

Supports: MC9S08PT60(A) and MC9S08PT32(A)

Document Number: MC9S08PT60RM
Rev 4, 08/2014

Contents

Section number	Title	Page
Chapter 1		
Device Overview		
1.1	Introduction.....	35
1.2	MCU block diagram.....	36
1.3	System clock distribution.....	38
Chapter 2		
Pins and connections		
2.1	Device pin assignment.....	41
2.2	Pin functions.....	45
2.2.1	Power (VDD, VSS).....	45
2.2.2	Analog power supply and reference pins (VDDA/VREFH and VSSA/VREFL).....	46
2.2.3	Oscillator (XTAL, EXTAL).....	47
2.2.4	External reset pin (RESET) and interrupt pin (IRQ).....	48
2.2.5	Background/mode select (BKGD/MS).....	49
2.2.6	Port A input/output (I/O) pins (PTA7–PTA0).....	50
2.2.7	Port B input/output (I/O) pins (PTB7–PTB0).....	50
2.2.8	Port C input/output (I/O) pins (PTC7–PTC0).....	50
2.2.9	Port D input/output (I/O) pins (PTD7–PTD0).....	50
2.2.10	Port E input/Output (I/O) pins (PTE7–PTE0).....	51
2.2.11	Port F input/output (I/O) pins (PTF7–PTF0).....	51
2.2.12	Port G input/output (I/O) pins (PTG3–PTG0).....	51
2.2.13	Port H input/output (I/O) pins (PTH7–PTH6, PTH2–PTH0).....	51
2.2.14	True open drain pins (PTA3–PTA2).....	51
2.2.15	High current drive pins (PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, PTH1).....	52
2.2.16	Peripheral pinouts.....	52
Chapter 3		
Power management		
3.1	Introduction.....	55

Section number	Title	Page
3.2	Features.....	55
3.2.1	Run mode.....	55
3.2.2	Wait mode.....	56
3.2.3	Stop3 mode.....	56
3.2.4	Active BDM enabled in stop3 mode.....	56
3.2.5	LVD enabled in stop mode.....	57
3.2.6	Power modes behaviors.....	57
3.3	Low voltage detect (LVD) system.....	58
3.3.1	Power-on reset (POR) operation.....	59
3.3.2	LVD reset operation.....	59
3.3.3	Low-voltage warning (LVW).....	59
3.4	Bandgap reference.....	60
3.5	Power management control bits and registers.....	60
3.5.1	System Power Management Status and Control 1 Register (PMC_SPMSC1).....	60
3.5.2	System Power Management Status and Control 2 Register (PMC_SPMSC2).....	62

Chapter 4 Memory map

4.1	Memory map.....	63
4.2	Reset and interrupt vector assignments.....	64
4.3	Register addresses and bit assignments.....	65
4.4	Random-access memory (RAM).....	77
4.5	Flash and EEPROM.....	77
4.5.1	Overview.....	77
4.5.2	Function descriptions.....	79
4.5.2.1	Modes of operation.....	79
4.5.2.2	Flash and EEPROM memory map.....	80
4.5.2.3	Flash and EEPROM initialization after system reset.....	80

Section number	Title	Page
4.5.2.4	Flash and EEPROM command operations.....	81
4.5.2.5	Flash and EEPROM interrupts.....	86
4.5.2.6	Protection.....	87
4.5.2.7	Security.....	91
4.5.2.8	Flash and EEPROM commands.....	93
4.5.2.9	Flash and EEPROM command summary.....	95
4.6	Flash and EEPROM registers descriptions.....	109
4.6.1	Flash Clock Divider Register (NVM_FCLKDIV).....	109
4.6.2	Flash Security Register (NVM_FSEC).....	110
4.6.3	Flash CCOB Index Register (NVM_FCCOBIX).....	111
4.6.4	Flash Configuration Register (NVM_FCENFG).....	111
4.6.5	Flash Error Configuration Register (NVM_FERCENFG).....	112
4.6.6	Flash Status Register (NVM_FSTAT).....	113
4.6.7	Flash Error Status Register (NVM_FERSTAT).....	114
4.6.8	Flash Protection Register (NVM_FPROT).....	115
4.6.9	EEPROM Protection Register (NVM_EEPROT).....	116
4.6.10	Flash Common Command Object Register:High (NVM_FCCOBHI).....	118
4.6.11	Flash Common Command Object Register: Low (NVM_FCCOBLO).....	118
4.6.12	Flash Option Register (NVM_FOPT).....	118

Chapter 5 Interrupt

5.1	Interrupts.....	121
5.1.1	Interrupt stack frame.....	122
5.1.2	Interrupt vectors, sources, and local masks.....	123
5.1.3	Hardware nested interrupt.....	126
5.1.3.1	Interrupt priority level register.....	127
5.1.3.2	Interrupt priority level comparator set.....	128
5.1.3.3	Interrupt priority mask update and restore mechanism.....	128
5.1.3.4	Integration and application of the IPC.....	129

Section number	Title	Page
5.2	IRQ.....	129
5.2.1	Features.....	130
5.2.1.1	Pin configuration options.....	130
5.2.1.2	Edge and level sensitivity.....	131
5.3	Interrupt pin request register.....	131
5.3.1	Interrupt Pin Request Status and Control Register (IRQ_SC).....	132
5.4	Interrupt priority control register.....	133
5.4.1	IPC Status and Control Register (IPC_SC).....	134
5.4.2	Interrupt Priority Mask Pseudo Stack Register (IPC_IPMPS).....	135
5.4.3	Interrupt Level Setting Registers n (IPC_ILRSn).....	135

Chapter 6 System control

6.1	System device identification (SDID).....	137
6.2	Universally unique identification (UUID).....	137
6.3	Reset and system initialization.....	137
6.4	System options.....	138
6.4.1	BKGD pin enable.....	138
6.4.2	RESET pin enable.....	138
6.4.3	SCI0 pin reassignment.....	138
6.4.4	SPI0 pin reassignment.....	139
6.4.5	IIC pins reassignments.....	139
6.4.6	FTM2 channels pin reassignment.....	139
6.4.7	Bus clock output pin enable.....	139
6.5	System interconnection.....	140
6.5.1	ACMP output selection.....	140
6.5.2	SCI0 TxD modulation.....	140
6.5.3	SCI0 RxD capture.....	141
6.5.4	SCI0 RxD filter.....	141
6.5.5	RTC capture.....	142

Section number	Title	Page
6.5.6	FTM2 software synchronization.....	142
6.5.7	ADC hardware trigger.....	142
6.6	System Control Registers.....	143
6.6.1	System Reset Status Register (SYS_SRS).....	143
6.6.2	System Background Debug Force Reset Register (SYS_SBDIFR).....	145
6.6.3	System Device Identification Register: High (SYS_SDIDH).....	146
6.6.4	System Device Identification Register: Low (SYS_SDIDL).....	146
6.6.5	System Options Register 1 (SYS_SOPT1).....	147
6.6.6	System Options Register 2 (SYS_SOPT2).....	148
6.6.7	System Options Register 3 (SYS_SOPT3).....	150
6.6.8	System Options Register 4 (SYS_SOPT4).....	150
6.6.9	Illegal Address Register: High (SYS_ILLAH).....	151
6.6.10	Illegal Address Register: Low (SYS_ILLAL).....	152
6.6.11	Universally Unique Identifier Register 1 (SYS_UUID1).....	152
6.6.12	Universally Unique Identifier Register 2 (SYS_UUID2).....	153
6.6.13	Universally Unique Identifier Register 3 (SYS_UUID3).....	153
6.6.14	Universally Unique Identifier Register 4 (SYS_UUID4).....	154
6.6.15	Universally Unique Identifier Register 5 (SYS_UUID5).....	154
6.6.16	Universally Unique Identifier Register 6 (SYS_UUID6).....	155
6.6.17	Universally Unique Identifier Register 7 (SYS_UUID7).....	155
6.6.18	Universally Unique Identifier Register 8 (SYS_UUID8).....	156

Chapter 7 Parallel input/output

7.1	Introduction.....	157
7.2	Port data and data direction.....	159
7.3	Internal pullup enable.....	160
7.4	Input glitch filter setting.....	160
7.5	High current drive.....	161
7.6	Pin behavior in stop mode.....	161

Section number	Title	Page
7.7	Port data registers.....	161
7.7.1	Port A Data Register (PORT_PTAD).....	162
7.7.2	Port B Data Register (PORT_PTBD).....	163
7.7.3	Port C Data Register (PORT_PTCD).....	163
7.7.4	Port D Data Register (PORT_PTDD).....	164
7.7.5	Port E Data Register (PORT_PTED).....	164
7.7.6	Port F Data Register (PORT_PTFD).....	165
7.7.7	Port G Data Register (PORT_PTGD).....	165
7.7.8	Port H Data Register (PORT_PTHD).....	166
7.7.9	Port High Drive Enable Register (PORT_HDRVE).....	167
7.7.10	Port A Output Enable Register (PORT_PTAOE).....	168
7.7.11	Port B Output Enable Register (PORT_PTBOE).....	169
7.7.12	Port C Output Enable Register (PORT_PTCOE).....	170
7.7.13	Port D Output Enable Register (PORT_PTDOE).....	172
7.7.14	Port E Output Enable Register (PORT_PTEOE).....	173
7.7.15	Port F Output Enable Register (PORT_PTFOE).....	174
7.7.16	Port G Output Enable Register (PORT_PTGOE).....	175
7.7.17	Port H Output Enable Register (PORT_PTHOE).....	176
7.7.18	Port A Input Enable Register (PORT_PTAIE).....	177
7.7.19	Port B Input Enable Register (PORT_PTBEIE).....	178
7.7.20	Port C Input Enable Register (PORT_PTCIE).....	179
7.7.21	Port D Input Enable Register (PORT_PTDIE).....	181
7.7.22	Port E Input Enable Register (PORT_PTEIE).....	182
7.7.23	Port F Input Enable Register (PORT_PTFIE).....	183
7.7.24	Port G Input Enable Register (PORT_PTGIE).....	184
7.7.25	Port H Input Enable Register (PORT_PTHIE).....	185
7.7.26	Port Filter Register 0 (PORT_IOFLT0).....	186
7.7.27	Port Filter Register 1 (PORT_IOFLT1).....	187
7.7.28	Port Filter Register 2 (PORT_IOFLT2).....	188

Section number	Title	Page
7.7.29	Port Clock Division Register (PORT_FCLKDIV).....	189
7.7.30	Port A Pullup Enable Register (PORT_PTAPE).....	190
7.7.31	Port B Pullup Enable Register (PORT_PTBPE).....	191
7.7.32	Port C Pullup Enable Register (PORT_PTCPE).....	192
7.7.33	Port D Pullup Enable Register (PORT_PTDPE).....	194
7.7.34	Port E Pullup Enable Register (PORT_PTEPE).....	195
7.7.35	Port F Pullup Enable Register (PORT_PTFPE).....	196
7.7.36	Port G Pullup Enable Register (PORT_PTGPE).....	198
7.7.37	Port H Pullup Enable Register (PORT_PTHPE).....	199

Chapter 8 Clock management

8.1	Clock module.....	201
8.2	Internal clock source (ICS).....	203
8.2.1	Function description.....	203
8.2.1.1	Bus frequency divider.....	204
8.2.1.2	Low power bit usage.....	204
8.2.1.3	Internal reference clock (ICSIRCLK).....	204
8.2.1.4	Fixed frequency clock (ICSFFCLK).....	205
8.2.1.5	BDC clock.....	206
8.2.2	Modes of operation.....	206
8.2.2.1	FLL engaged internal (FEI).....	207
8.2.2.2	FLL engaged external (FEE).....	208
8.2.2.3	FLL bypassed internal (FBI).....	208
8.2.2.4	FLL bypassed internal low power (FBILP).....	208
8.2.2.5	FLL bypassed external (FBE).....	209
8.2.2.6	FLL bypassed external low power (FBELP).....	209
8.2.2.7	Stop (STOP).....	210
8.2.3	FLL lock and clock monitor.....	211
8.2.3.1	FLL clock lock.....	211

Section number	Title	Page
8.2.3.2	External reference clock monitor.....	211
8.3	Initialization / application information.....	211
8.3.1	Initializing FEI mode.....	212
8.3.2	Initializing FBI mode.....	212
8.3.3	Initializing FEE mode.....	212
8.3.4	Initializing FBE mode.....	213
8.3.5	External oscillator (OSC).....	213
8.3.5.1	Bypass mode.....	214
8.3.5.2	Low-power configuration.....	214
8.3.5.3	High-gain configuration.....	215
8.3.5.4	Initializing external oscillator for peripherals.....	215
8.4	1 kHz low-power oscillator (LPO).....	216
8.5	Peripheral clock gating.....	216
8.6	ICS control registers.....	216
8.6.1	ICS Control Register 1 (ICS_C1).....	217
8.6.2	ICS Control Register 2 (ICS_C2).....	218
8.6.3	ICS Control Register 3 (ICS_C3).....	219
8.6.4	ICS Control Register 4 (ICS_C4).....	219
8.6.5	ICS Status Register (ICS_S).....	220
8.6.6	OSC Status and Control Register (ICS_OSCSC).....	221
8.7	System clock gating control registers.....	222
8.7.1	System Clock Gating Control 1 Register (SCG_C1).....	223
8.7.2	System Clock Gating Control 2 Register (SCG_C2).....	224
8.7.3	System Clock Gating Control 3 Register (SCG_C3).....	225
8.7.4	System Clock Gating Control 4 Register (SCG_C4).....	226

Chapter 9 Chip configurations

9.1	Introduction.....	229
-----	-------------------	-----

Section number	Title	Page
9.2	Core modules.....	229
9.2.1	Central processor unit (CPU).....	229
9.2.2	Debug module (DBG).....	229
9.3	System modules.....	230
9.3.1	Watchdog (WDOG).....	230
9.4	Clock module.....	230
9.5	Memory.....	232
9.5.1	Random-access-memory (RAM).....	232
9.5.2	Non-volatile memory (NVM).....	232
9.6	Power modules.....	232
9.7	Security.....	233
9.7.1	Cyclic redundancy check (CRC).....	233
9.8	Timers.....	235
9.8.1	FlexTimer module (FTM).....	235
9.8.1.1	FTM0 interconnection.....	236
9.8.1.2	FTM1 interconnection.....	237
9.8.1.3	FTM2 interconnection.....	237
9.8.2	8-bit modulo timer (MTIM).....	237
9.8.2.1	MTIM0 as ADC hardware trigger.....	239
9.8.3	Real-time counter (RTC).....	239
9.9	Communication interfaces.....	241
9.9.1	Serial communications interface (SCI).....	241
9.9.1.1	SCI0 infrared functions.....	243
9.9.2	8-Bit Serial Peripheral Interface (8-bit SPI).....	244
9.9.3	16-bit serial peripheral interface (16-bit SPI).....	246
9.9.4	Inter-Integrated Circuit (I2C).....	248
9.10	Analog.....	250
9.10.1	Analog-to-digital converter (ADC).....	250
9.10.1.1	ADC channel assignments.....	251

Section number	Title	Page
9.10.1.2	Alternate clock.....	252
9.10.1.3	Hardware trigger.....	253
9.10.1.4	Temperature sensor.....	253
9.10.2	Analog comparator (ACMP).....	254
9.10.2.1	ACMP configuration information.....	256
9.10.2.2	ACMP in stop3 mode.....	256
9.10.2.3	ACMP to FTM configuration information.....	256
9.10.2.4	ACMP for SCI0 RXD filter.....	256
9.11	Human-machine interfaces HMI.....	257
9.11.1	Keyboard interrupts (KBI).....	257
9.11.2	Touch sense input (TSI).....	259
9.11.2.1	TSI channel assignments.....	260
9.11.2.2	Hardware trigger.....	261

Chapter 10 Central processor unit

10.1	Introduction.....	263
10.1.1	Features.....	263
10.2	Programmer's Model and CPU Registers.....	264
10.2.1	Accumulator (A).....	264
10.2.2	Index Register (H:X).....	265
10.2.3	Stack Pointer (SP).....	265
10.2.4	Program Counter (PC).....	266
10.2.5	Condition Code Register (CCR).....	266
10.3	Addressing Modes.....	267
10.3.1	Inherent Addressing Mode (INH).....	268
10.3.2	Relative Addressing Mode (REL).....	268
10.3.3	Immediate Addressing Mode (IMM).....	268
10.3.4	Direct Addressing Mode (DIR).....	269
10.3.5	Extended Addressing Mode (EXT).....	269

Section number	Title	Page
10.3.6	Indexed Addressing Mode.....	270
10.3.6.1	Indexed, No Offset (IX).....	270
10.3.6.2	Indexed, No Offset with Post Increment (IX+).....	270
10.3.6.3	Indexed, 8-Bit Offset (IX1).....	270
10.3.6.4	Indexed, 8-Bit Offset with Post Increment (IX1+).....	271
10.3.6.5	Indexed, 16-Bit Offset (IX2).....	271
10.3.6.6	SP-Relative, 8-Bit Offset (SP1).....	271
10.3.6.7	SP-Relative, 16-Bit Offset (SP2).....	272
10.3.7	Memory to memory Addressing Mode.....	272
10.3.7.1	Direct to Direct.....	272
10.3.7.2	Immediate to Direct.....	272
10.3.7.3	Indexed to Direct, Post Increment.....	272
10.3.7.4	Direct to Indexed, Post-Increment.....	273
10.4	Operation modes.....	273
10.4.1	Stop mode.....	273
10.4.2	Wait mode.....	273
10.4.3	Background mode.....	274
10.4.4	Security mode.....	275
10.5	HCS08 V6 Opcodes.....	277
10.6	Special Operations.....	277
10.6.1	Reset Sequence.....	277
10.6.2	Interrupt Sequence.....	277
10.7	Instruction Set Summary.....	278

Chapter 11 Keyboard Interrupts (KBI)

11.1	Introduction.....	291
11.1.1	Features.....	291
11.1.2	Modes of Operation.....	291
11.1.2.1	KBI in Wait mode.....	291

Section number	Title	Page
11.1.2.2	KBI in Stop modes.....	292
11.1.2.3	KBI in Active Background mode.....	292
11.1.3	Block Diagram.....	292
11.2	External signals description.....	293
11.3	Register definition.....	293
11.4	Memory Map and Registers.....	293
11.4.1	KBI Status and Control Register (KBIx_SC).....	294
11.4.2	KBIx Pin Enable Register (KBIx_PE).....	294
11.4.3	KBIx Edge Select Register (KBIx_ES).....	295
11.5	Functional Description.....	295
11.5.1	Edge-only sensitivity.....	296
11.5.2	Edge and level sensitivity.....	296
11.5.3	KBI Pullup Resistor.....	296
11.5.4	KBI initialization.....	296
 Chapter 12 FlexTimer Module (FTM) 		
12.1	Introduction.....	299
12.1.1	FlexTimer philosophy.....	299
12.1.2	Features.....	300
12.1.3	Modes of operation.....	301
12.1.4	Block diagram.....	301
12.2	Signal description.....	304
12.2.1	EXTCLK — FTM external clock.....	304
12.2.2	CHn — FTM channel (n) I/O pin.....	304
12.2.3	FAULTj — FTM fault input.....	304
12.3	Memory map and register definition.....	305
12.3.1	Module memory map.....	305
12.3.2	Register descriptions.....	305
12.3.3	Status and Control (FTMx_SC).....	309

Section number	Title	Page
12.3.4	Counter High (FTMx_CNTH).....	310
12.3.5	Counter Low (FTMx_CNTL).....	311
12.3.6	Modulo High (FTMx_MODH).....	311
12.3.7	Modulo Low (FTMx_MODL).....	312
12.3.8	Channel Status and Control (FTMx_CnSC).....	312
12.3.9	Channel Value High (FTMx_CnVH).....	315
12.3.10	Channel Value Low (FTMx_CnVL).....	316
12.3.11	Counter Initial Value High (FTMx_CNTINH).....	316
12.3.12	Counter Initial Value Low (FTMx_CNTINL).....	317
12.3.13	Capture and Compare Status (FTMx_STATUS).....	317
12.3.14	Features Mode Selection (FTMx_MODE).....	319
12.3.15	Synchronization (FTMx_SYNC).....	320
12.3.16	Initial State for Channel Output (FTMx_OUTINIT).....	322
12.3.17	Output Mask (FTMx_OUTMASK).....	324
12.3.18	Function for Linked Channels (FTMx_COMBINE n).....	325
12.3.19	Deadtime Insertion Control (FTMx_DEADTIME).....	327
12.3.20	External Trigger (FTMx_EXTTRIG).....	328
12.3.21	Channels Polarity (FTMx_POL).....	329
12.3.22	Fault Mode Status (FTMx_FMS).....	331
12.3.23	Input Capture Filter Control (FTMx_FILTER n).....	332
12.3.24	Fault Input Filter Control (FTMx_FLTFILTER).....	333
12.3.25	Fault Input Control (FTMx_FLTCTRL).....	334
12.4	Functional Description.....	335
12.4.1	Clock Source.....	336
12.4.1.1	Counter Clock Source.....	336
12.4.2	Prescaler.....	337
12.4.3	Counter.....	337
12.4.3.1	Up counting.....	337
12.4.3.2	Up-down counting.....	340

Section number	Title	Page
12.4.3.3	Free running counter.....	341
12.4.3.4	Counter reset.....	342
12.4.4	Input capture mode.....	342
12.4.4.1	Filter for input capture mode.....	343
12.4.5	Output compare mode.....	344
12.4.6	Edge-aligned PWM (EPWM) mode.....	346
12.4.7	Center-aligned PWM (CPWM) mode.....	348
12.4.8	Combine mode.....	350
12.4.8.1	Asymmetrical PWM.....	357
12.4.9	Complementary mode.....	357
12.4.10	Update of the registers with write buffers.....	358
12.4.10.1	CNTINH:L registers.....	358
12.4.10.2	MODH:L registers.....	358
12.4.10.3	CnVH:L registers.....	359
12.4.11	PWM synchronization.....	360
12.4.11.1	Hardware trigger.....	360
12.4.11.2	Software trigger.....	361
12.4.11.3	Boundary cycle.....	362
12.4.11.4	MODH:L registers synchronization.....	363
12.4.11.5	CnVH:L registers synchronization.....	365
12.4.11.6	OUTMASK register synchronization.....	365
12.4.11.7	FTM counter synchronization.....	367
12.4.11.8	Summary of PWM synchronization.....	369
12.4.12	Deadtime insertion.....	371
12.4.12.1	Deadtime insertion corner cases.....	372
12.4.13	Output mask.....	373
12.4.14	Fault control.....	374
12.4.14.1	Automatic fault clearing.....	376
12.4.14.2	Manual fault clearing.....	377

Section number	Title	Page
12.4.15	Polarity control.....	378
12.4.16	Initialization.....	378
12.4.17	Features priority.....	379
12.4.18	Channel trigger output.....	379
12.4.19	Initialization trigger.....	380
12.4.20	Capture test mode.....	382
12.4.21	Dual edge capture mode.....	383
12.4.21.1	One-shot capture mode.....	385
12.4.21.2	Continuous capture mode.....	385
12.4.21.3	Pulse width measurement.....	386
12.4.21.4	Period measurement.....	388
12.4.21.5	Read coherency mechanism.....	390
12.4.22	TPM emulation.....	392
12.4.22.1	MODH:L and CnVH:L synchronization.....	392
12.4.22.2	Free running counter.....	392
12.4.22.3	Write to SC.....	392
12.4.22.4	Write to CnSC.....	392
12.4.23	BDM mode.....	392
12.5	Reset overview.....	393
12.6	FTM Interrupts.....	395
12.6.1	Timer overflow interrupt.....	395
12.6.2	Channel (n) interrupt.....	395
12.6.3	Fault interrupt.....	395

Chapter 13 8-bit modulo timer (MTIM)

13.1	Introduction.....	397
13.2	Features.....	397
13.3	Modes of operation.....	397
13.3.1	MTIM in wait mode.....	398

Section number	Title	Page
13.3.2	MTIM in stop mode.....	398
13.3.3	MTIM in active background mode.....	398
13.4	Block diagram.....	398
13.5	External signal description.....	399
13.6	Register definition.....	399
13.6.1	MTIM Status and Control Register (MTIMx_SC).....	400
13.6.2	MTIM Clock Configuration Register (MTIMx_CLK).....	401
13.6.3	MTIM Counter Register (MTIMx_CNT).....	402
13.6.4	MTIM Modulo Register (MTIMx_MOD).....	402
13.7	Functional description.....	402
13.7.1	MTIM operation example.....	404

Chapter 14 Real-time counter (RTC)

14.1	Introduction.....	405
14.2	Features.....	405
14.2.1	Modes of operation.....	405
14.2.1.1	Wait mode.....	405
14.2.1.2	Stop modes.....	406
14.2.2	Block diagram.....	406
14.3	External signal description.....	406
14.4	Register definition.....	407
14.4.1	RTC Status and Control Register 1 (RTC_SC1).....	407
14.4.2	RTC Status and Control Register 2 (RTC_SC2).....	408
14.4.3	RTC Modulo Register: High (RTC_MODH).....	409
14.4.4	RTC Modulo Register: Low (RTC_MODL).....	409
14.4.5	RTC Counter Register: High (RTC_CNTH).....	410
14.4.6	RTC Counter Register: Low (RTC_CNTL).....	410
14.5	Functional description.....	411
14.5.1	RTC operation example.....	412

Section number	Title	Page
14.6	Initialization/application information.....	414

Chapter 15 Serial communications interface (SCI)

15.1	Introduction.....	415
15.1.1	Features.....	415
15.1.2	Modes of operation.....	415
15.1.3	Block diagram.....	416
15.2	SCI signal descriptions.....	418
15.2.1	Detailed signal descriptions.....	418
15.3	Register definition.....	418
15.3.1	SCI Baud Rate Register: High (SCIx_BDH).....	419
15.3.2	SCI Baud Rate Register: Low (SCIx_BDL).....	420
15.3.3	SCI Control Register 1 (SCIx_C1).....	421
15.3.4	SCI Control Register 2 (SCIx_C2).....	422
15.3.5	SCI Status Register 1 (SCIx_S1).....	423
15.3.6	SCI Status Register 2 (SCIx_S2).....	425
15.3.7	SCI Control Register 3 (SCIx_C3).....	427
15.3.8	SCI Data Register (SCIx_D).....	428
15.4	Functional description.....	429
15.4.1	Baud rate generation.....	429
15.4.2	Transmitter functional description.....	430
15.4.2.1	Send break and queued idle.....	430
15.4.3	Receiver functional description.....	431
15.4.3.1	Data sampling technique.....	432
15.4.3.2	Receiver wake-up operation.....	433
15.4.4	Interrupts and status flags.....	434
15.4.5	Baud rate tolerance.....	435
15.4.5.1	Slow data tolerance.....	436
15.4.5.2	Fast data tolerance.....	437

Section number	Title	Page
15.4.6	Additional SCI functions.....	438
15.4.6.1	8- and 9-bit data modes.....	438
15.4.6.2	Stop mode operation.....	438
15.4.6.3	Loop mode.....	439
15.4.6.4	Single-wire operation.....	439

Chapter 16

8-Bit Serial Peripheral Interface (8-bit SPI)

16.1	Introduction.....	441
16.1.1	Features.....	441
16.1.2	Modes of Operation.....	442
16.1.3	Block Diagrams.....	442
16.1.3.1	SPI System Block Diagram.....	443
16.1.3.2	SPI Module Block Diagram.....	443
16.2	External Signal Description.....	444
16.2.1	SPSCK — SPI Serial Clock.....	445
16.2.2	MOSI — Master Data Out, Slave Data In.....	445
16.2.3	MISO — Master Data In, Slave Data Out.....	445
16.2.4	SS — Slave Select.....	445
16.3	Register Definition.....	446
16.3.1	SPI control register 1 (SPIx_C1).....	446
16.3.2	SPI control register 2 (SPIx_C2).....	448
16.3.3	SPI baud rate register (SPIx_BR).....	449
16.3.4	SPI status register (SPIx_S).....	450
16.3.5	SPI data register (SPIx_D).....	451
16.3.6	SPI match register (SPIx_M).....	452
16.4	Functional Description.....	452
16.4.1	General.....	452
16.4.2	Master Mode.....	453
16.4.3	Slave Mode.....	454

Section number	Title	Page
16.4.4	SPI Clock Formats.....	456
16.4.5	SPI Baud Rate Generation.....	459
16.4.6	Special Features.....	459
16.4.6.1	SS Output.....	459
16.4.6.2	Bidirectional Mode (MOMI or SISO).....	460
16.4.7	Error Conditions.....	461
16.4.7.1	Mode Fault Error.....	461
16.4.8	Low Power Mode Options.....	462
16.4.8.1	SPI in Run Mode.....	462
16.4.8.2	SPI in Wait Mode.....	462
16.4.8.3	SPI in Stop Mode.....	463
16.4.9	Reset.....	463
16.4.10	Interrupts.....	464
16.4.10.1	MODF.....	464
16.4.10.2	SPRF.....	464
16.4.10.3	SPTEF.....	465
16.4.10.4	SPMF.....	465
16.5	Initialization/Application Information.....	465
16.5.1	Initialization Sequence.....	465
16.5.2	Pseudo-Code Example.....	466

Chapter 17

16-Bit Serial Peripheral Interface (16-Bit SPI)

17.1	Introduction.....	469
17.1.1	Features.....	469
17.1.2	Modes of operation.....	470
17.1.3	Block diagrams.....	471
17.1.3.1	SPI system block diagram.....	471
17.1.3.2	SPI module block diagram.....	471

Section number	Title	Page
17.2	External signal description.....	473
17.2.1	SPSCK — SPI Serial Clock.....	474
17.2.2	MOSI — Master Data Out, Slave Data In.....	474
17.2.3	MISO — Master Data In, Slave Data Out.....	474
17.2.4	SS — Slave Select.....	474
17.3	Memory map/register definition.....	475
17.3.1	SPI Control Register 1 (SPIx_C1).....	475
17.3.2	SPI Control Register 2 (SPIx_C2).....	477
17.3.3	SPI Baud Rate Register (SPIx_BR).....	478
17.3.4	SPI Status Register (SPIx_S).....	479
17.3.5	SPI data register high (SPIx_DH).....	482
17.3.6	SPI Data Register low (SPIx_DL).....	483
17.3.7	SPI match register high (SPIx_MH).....	484
17.3.8	SPI Match Register low (SPIx_ML).....	484
17.3.9	SPI control register 3 (SPIx_C3).....	485
17.3.10	SPI clear interrupt register (SPIx_CI).....	486
17.4	Functional description.....	487
17.4.1	General.....	488
17.4.2	Master mode.....	488
17.4.3	Slave mode.....	489
17.4.4	SPI FIFO Mode.....	491
17.4.5	Data Transmission Length.....	492
17.4.6	SPI clock formats.....	493
17.4.7	SPI baud rate generation.....	496
17.4.8	Special features.....	496
17.4.8.1	SS Output.....	496
17.4.8.2	Bidirectional mode (MOMI or SISO).....	497
17.4.9	Error conditions.....	498
17.4.9.1	Mode fault error.....	498

Section number	Title	Page
17.4.10	Low-power mode options.....	499
17.4.10.1	SPI in Run mode.....	499
17.4.10.2	SPI in Wait mode.....	499
17.4.10.3	SPI in Stop mode.....	500
17.4.11	Reset.....	500
17.4.12	Interrupts.....	501
17.4.12.1	MODF.....	501
17.4.12.2	SPRF.....	501
17.4.12.3	SPTEF.....	502
17.4.12.4	SPMF.....	502
17.4.12.5	TNEAREF	502
17.4.12.6	RNFULLF	502
17.5	Initialization/application information.....	503
17.5.1	Initialization sequence.....	503
17.5.2	Pseudo-Code Example.....	503

Chapter 18 Inter-Integrated Circuit (I2C)

18.1	Introduction.....	507
18.1.1	Features.....	507
18.1.2	Modes of operation.....	508
18.1.3	Block diagram.....	508
18.2	I2C signal descriptions.....	509
18.3	Memory map/register definition.....	510
18.3.1	I2C Address Register 1 (I2C_A1).....	510
18.3.2	I2C Frequency Divider register (I2C_F).....	511
18.3.3	I2C Control Register 1 (I2C_C1).....	512
18.3.4	I2C Status register (I2C_S).....	513
18.3.5	I2C Data I/O register (I2C_D).....	515
18.3.6	I2C Control Register 2 (I2C_C2).....	516

Section number	Title	Page
18.3.7	I2C Programmable Input Glitch Filter Register (I2C_FLT).....	516
18.3.8	I2C Range Address register (I2C_RA).....	517
18.3.9	I2C SMBus Control and Status register (I2C_SMB).....	517
18.3.10	I2C Address Register 2 (I2C_A2).....	519
18.3.11	I2C SCL Low Timeout Register High (I2C_SLTH).....	519
18.3.12	I2C SCL Low Timeout Register Low (I2C_SLTL).....	520
18.4	Functional description.....	520
18.4.1	I2C protocol.....	520
18.4.1.1	START signal.....	521
18.4.1.2	Slave address transmission.....	521
18.4.1.3	Data transfers.....	522
18.4.1.4	STOP signal.....	522
18.4.1.5	Repeated START signal.....	523
18.4.1.6	Arbitration procedure.....	523
18.4.1.7	Clock synchronization.....	523
18.4.1.8	Handshaking.....	524
18.4.1.9	Clock stretching.....	524
18.4.1.10	I2C divider and hold values.....	524
18.4.2	10-bit address.....	525
18.4.2.1	Master-transmitter addresses a slave-receiver.....	526
18.4.2.2	Master-receiver addresses a slave-transmitter.....	526
18.4.3	Address matching.....	527
18.4.4	System management bus specification.....	528
18.4.4.1	Timeouts.....	528
18.4.4.2	FAST ACK and NACK.....	530
18.4.5	Resets.....	530
18.4.6	Interrupts.....	530
18.4.6.1	Byte transfer interrupt.....	531
18.4.6.2	Address detect interrupt.....	531

Section number	Title	Page
18.4.6.3	Exit from low-power/stop modes.....	531
18.4.6.4	Arbitration lost interrupt.....	532
18.4.6.5	Timeout interrupt in SMBus.....	532
18.4.7	Programmable input glitch filter.....	533
18.4.8	Address matching wake-up.....	533
18.5	Initialization/application information.....	534

Chapter 19

Analog-to-digital converter (ADC)

19.1	Introduction.....	537
19.1.1	Features.....	537
19.1.2	Block Diagram.....	538
19.2	External Signal Description.....	538
19.2.1	Analog Power (VDDA).....	539
19.2.2	Analog Ground (VSSA).....	539
19.2.3	Voltage Reference High (VREFH).....	539
19.2.4	Voltage Reference Low (VREFL).....	539
19.2.5	Analog Channel Inputs (ADx).....	539
19.3	ADC Control Registers.....	540
19.3.1	Status and Control Register 1 (ADC_SC1).....	540
19.3.2	Status and Control Register 2 (ADC_SC2).....	542
19.3.3	Status and Control Register 3 (ADC_SC3).....	543
19.3.4	Status and Control Register 4 (ADC_SC4).....	544
19.3.5	Conversion Result High Register (ADC_RH).....	545
19.3.6	Conversion Result Low Register (ADC_RL).....	546
19.3.7	Compare Value High Register (ADC_CVH).....	547
19.3.8	Compare Value Low Register (ADC_CVL).....	547
19.3.9	Pin Control 1 Register (ADC_APCTL1).....	548
19.3.10	Pin Control 2 Register (ADC_APCTL2).....	549