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Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D



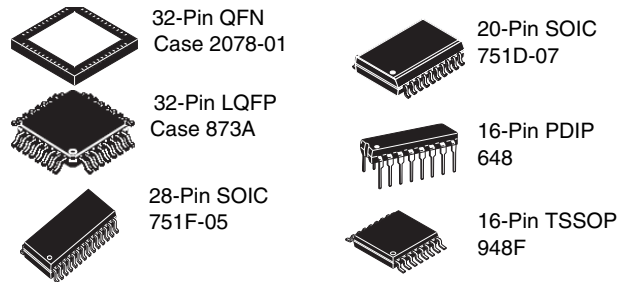
MC9S08QE8 Series

Covers: MC9S08QE8 and MC9S08QE4

Features

- 8-Bit HCS08 Central Processor Unit (CPU)
 - Up to 20 MHz CPU at 3.6 V to 1.8 V across temperature range of –40 °C to 85 °C
 - HC08 instruction set with added BGND instruction
 - Support for up to 32 interrupt/reset sources
- On-Chip Memory
 - Flash read/program/erase over full operating voltage and temperature
 - Random-access memory (RAM)
 - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
 - Two low power stop modes
 - Reduced power wait mode
 - Low power run and wait modes allow peripherals to run while voltage regulator is in standby
 - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
 - Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
 - 6 μs typical wake-up time from stop3 mode
- Clock Source Options
 - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies from 1 MHz to 10 MHz
- System Protection
 - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
 - Low-voltage warning with interrupt
 - Low-voltage detection with reset or interrupt
 - Illegal opcode detection with reset
 - Illegal address detection with reset
 - Flash block protection
- Development Support
 - Single-wire background debug interface
 - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)

MC9S08QE8



- On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
- Peripherals
 - **ADC** — 10-channel, 12-bit resolution; 2.5 μs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
 - **ACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
 - **SCI** — Full-duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake-up on active edge
 - **SPI** — Full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
 - **IIC** — Up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supporting broadcast mode and 10-bit addressing
 - **TPMx** — Two 3-channel (TPM1 and TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
 - **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wakeup without external components; runs in all MCU modes
- Input/Output
 - 26 GPIOs, one output-only pin and one input-only pin
 - Eight KBI interrupts with selectable polarity
 - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins.
- Package Options
 - 32-pin LQFP, 32-pin QFN, 28-pin SOIC, 20-pin SOIC, 16-pin PDIP, 16-pin TSSOP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
2	Nov 7 2007	Initial preliminary product preview release.
3	Jan 22 2008	Initial public release.
4	March 13 2008	Added Figure 11 .
5	October 8 2008	Updated the Stop2 and Stop3 mode supply current in the Table 8 . Replaced the stop mode adders section from Table 8 with an individual Table 9 with new specifications. Added a footnote to the Min. of the supply voltage in Table 7 . Changed the typical value of $ I_{IN} $ and $ I_{OZ} $ to — (no typical value) in Table 7 . Added t_{VRR} to Table 12 . Updated “How to reach us” information.
6	Nov. 4 2008	Updated the operating voltage in Table 7 .
7	April 29 2009	Changed V_{DDAD} to V_{DDA} , I_{DDAD} to I_{DDA} , and V_{SSAD} to V_{SSA} . In Table 7 , added I_{OZTOT} . In Table 11 , updated the DCO output frequency range-trimmed, and changed some symbols. Updated typicals and Max. for t_{IRST} . Updated Table 17 .
8	April 12, 2011	Added 32-pin QFN package.

Related Documentation

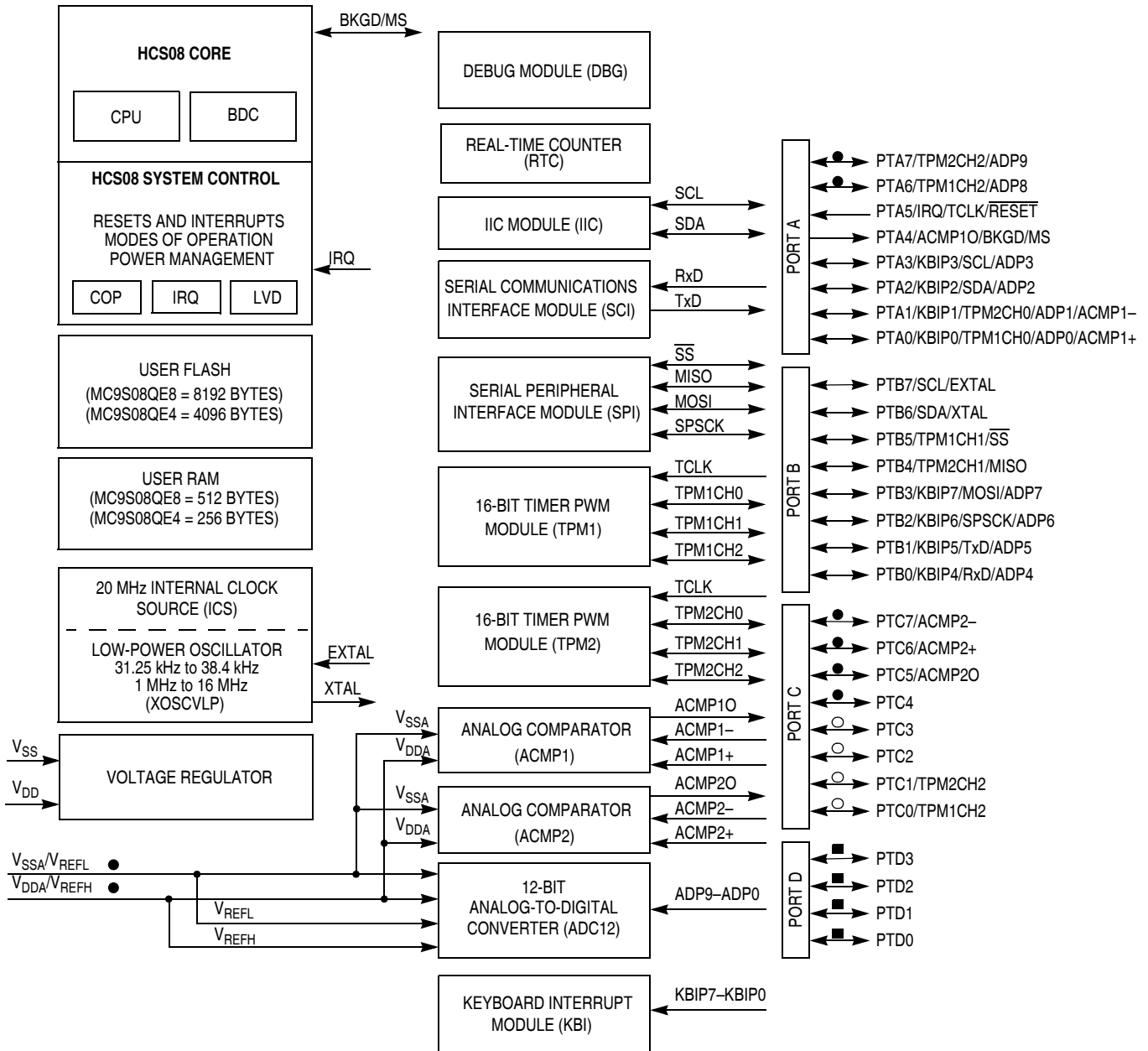
Find the most current versions of all documents at: <http://www.freescale.com>

Reference Manual (MC9S08QE8RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, [Figure 1](#), shows the structure of MC9S08QE8 series MCU.



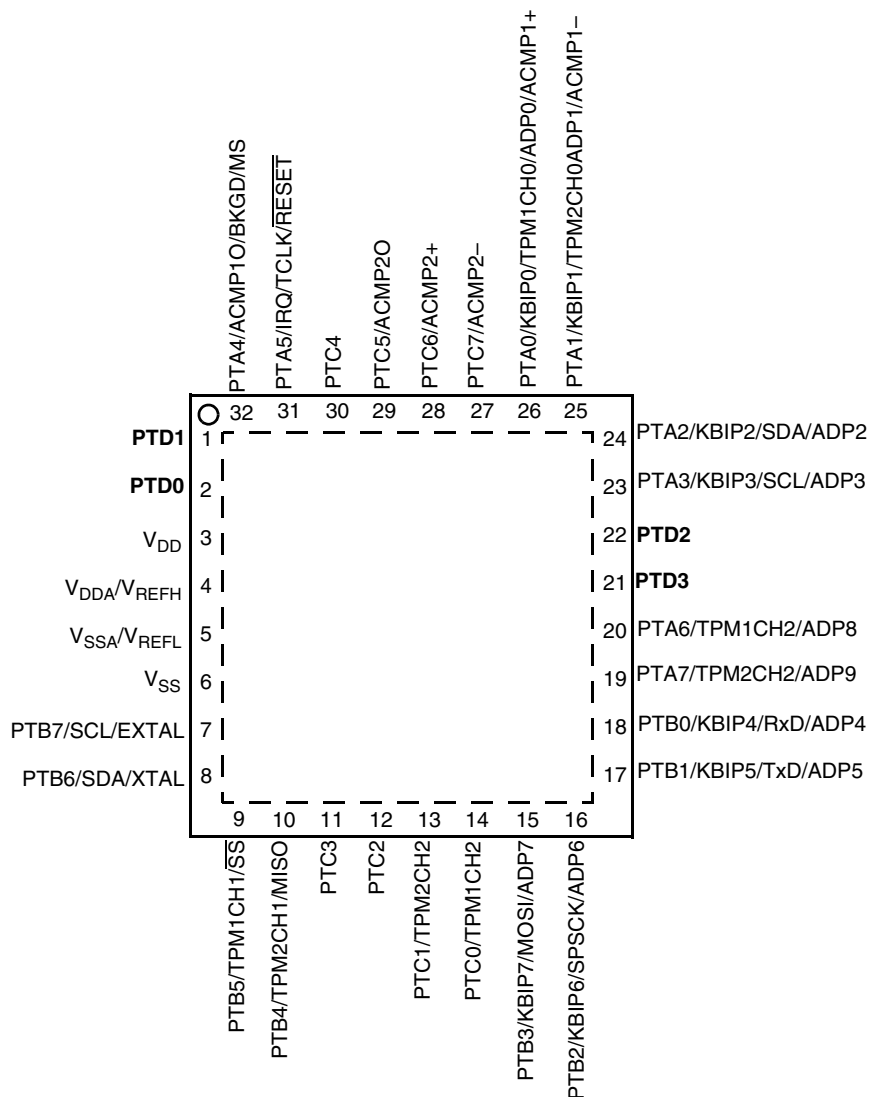
- pins not available on 16-pin packages
- pins not available on 16-pin or 20-pin packages
- pins not available on 16-pin, 20-pin or 28-pin packages

Notes: When PTA5 is configured as $\overline{\text{RESET}}$, pin becomes bi-directional with output being open-drain drive containing an internal pullup device.
 When PTA4 is configured as BKGD, pin becomes bi-directional.
 For the 16-pin and 20-pin packages, V_{SSA}/V_{REFL} and V_{DDA}/V_{REFH} are double bonded to V_{SS} and V_{DD} respectively.

Figure 1. MC9S08QE8 Series Block Diagram

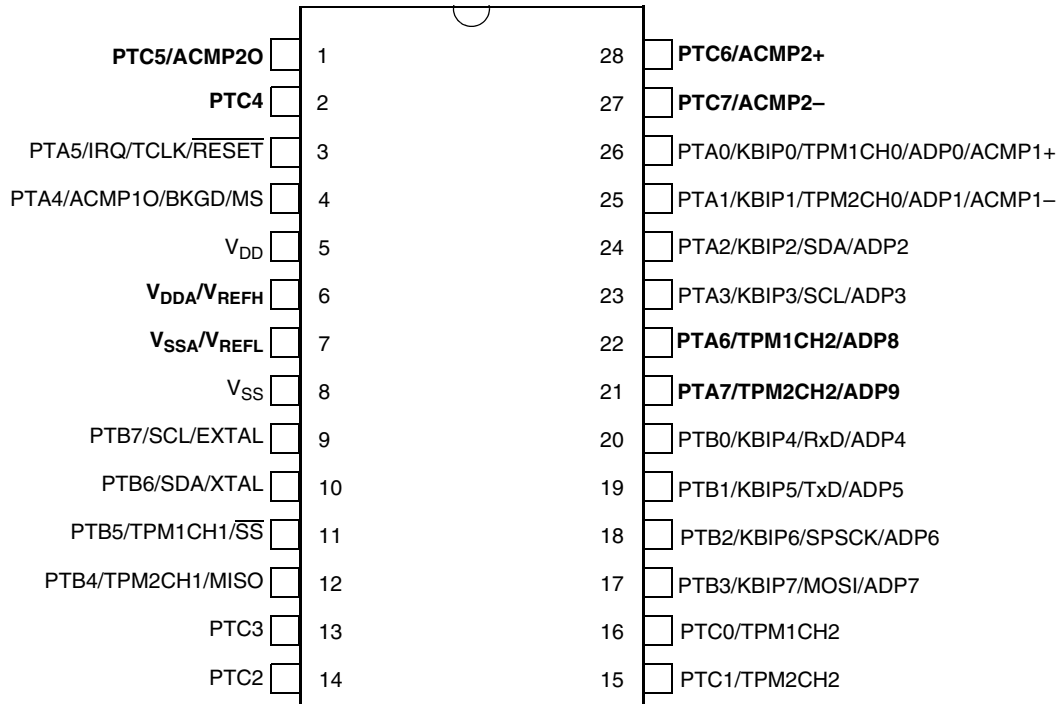
2 Pin Assignments

This section shows the pin assignments for the MC9S08QE8 series devices.



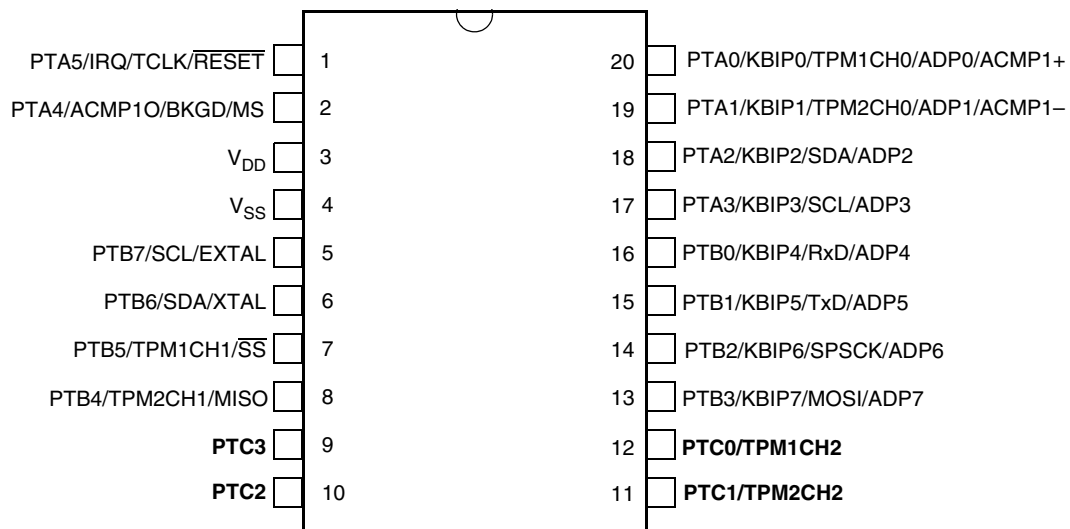
Pins shown in bold type are lost in the next lower pin count package.

Figure 2. MC9S08QE8 Series in 32-Pin LQFP/QFN Package



Pins shown in bold type are lost in the next lower pin count package.

Figure 3. MC9S08QE8 Series in 28-pin SOIC Package



Pins shown in bold type are lost in the next lower pin count package.

Figure 4. MC9S08QE8 Series in 20-pin SOIC Package

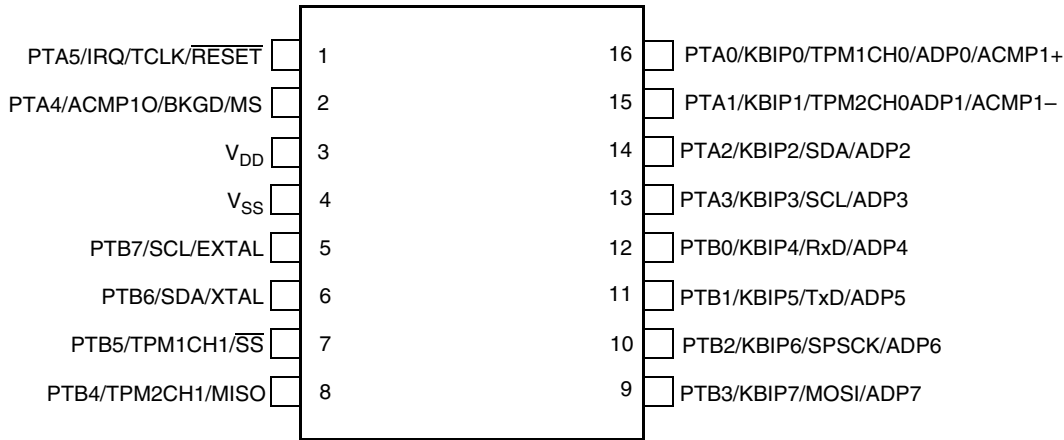


Figure 5. MC9S08QE8 Series in 16-pin PDIP and TSSOP Packages

Table 1. Pin Availability by Package Pin-Count

Pin Number				<-- Lowest Priority --> Highest				
32	28	20	16	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	—	—	—	PTD1				
2	—	—	—	PTD0				
3	5	3	3					V _{DD}
4	6	—	—					V _{DDA} /V _{REFH}
5	7	—	—					V _{SSA} /V _{REFL}
6	8	4	4					V _{SS}
7	9	5	5	PTB7	SCL ¹			EXTAL
8	10	6	6	PTB6	SDA ¹			XTAL
9	11	7	7	PTB5	TPM1CH1	SS		
10	12	8	8	PTB4	TPM2CH1	MISO		
11	13	9	—	PTC3				
12	14	10	—	PTC2				
13	15	11	—	PTC1	TPM2CH2 ²			
14	16	12	—	PTC0	TPM1CH2 ³			
15	17	13	9	PTB3	KBIP7	MOSI	ADP7	
16	18	14	10	PTB2	KBIP6	SPSCK	ADP6	
17	19	15	11	PTB1	KBIP5	TxD	ADP5	
18	20	16	12	PTB0	KBIP4	RxD	ADP4	
19	21	—	—	PTA7	TPM2CH2 ²		ADP9	
20	22	—	—	PTA6	TPM1CH2 ³		ADP8	
21	—	—	—	PTD3				
22	—	—	—	PTD2				
23	23	17	13	PTA3	KBIP3	SCL ¹	ADP3	
24	24	18	14	PTA2	KBIP2	SDA ¹	ADP2	
25	25	19	15	PTA1	KBIP1	TPM2CH0	ADP1 ⁴	ACMP1- ⁴

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number				<-- Lowest Priority --> Highest				
32	28	20	16	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
26	26	20	16	PTA0	KBIP0	TPM1CH0	ADP0 ⁴	ACMP1+ ⁴
27	27	—	—	PTC7				ACMP2–
28	28	—	—	PTC6				ACMP2+
29	1	—	—	PTC5				ACMP2O
30	2	—	—	PTC4				
31	3	1	1	PTA5	IRQ	TCLK	RESET	
32	4	2	2	PTA4	ACMP1O	BKGD	MS	

¹ IIC pins, SCL and SDA can be repositioned using IICPS in SOPT2, default reset locations are PTA3 and PTA2.

² TPM2CH2 pin can be repositioned using TPM2CH2PS in SOPT2, default reset location is PTA7.

³ TPM1CH2 pin can be repositioned using TPM1CH2PS in SOPT2, default reset location is PTA6.

⁴ If ADC and ACMP1 are enabled, both modules will have access to the pin.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 to 3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	±25	mA
Storage temperature range	T_{stg}	-55 to 150	°C

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 85	$^{\circ}\text{C}$
Maximum junction temperature	T_{JM}	95	$^{\circ}\text{C}$
Thermal resistance Single-layer board			
32-pin QFN	θ_{JA}	110	$^{\circ}\text{C}/\text{W}$
32-pin LQFP		66	
28-pin SOIC		57	
20-pin SOIC		71	
16-pin PDIP		64	
16-pin TSSOP		108	
Thermal resistance Four-layer board			
32-pin QFN	θ_{JA}	42	$^{\circ}\text{C}/\text{W}$
32-pin LQFP		47	
28-pin SOIC		42	
20-pin SOIC		52	
16-pin PDIP		47	
16-pin TSSOP		78	

The average chip-junction temperature (T_J) in $^{\circ}\text{C}$ can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, $^{\circ}\text{C}$

θ_{JA} = Package thermal resistance, junction-to-ambient, $^{\circ}\text{C}/\text{W}$

$P_D = P_{\text{int}} + P_{I/O}$

$P_{\text{int}} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{\text{int}}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273 \text{ }^{\circ}\text{C}) \quad \text{Eqn. 2}$$

Solving [Equation 1](#) and [Equation 2](#) for K gives:

$$K = P_D \times (T_A + 273 \text{ }^{\circ}\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating ¹	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Machine model (MM)	V_{MM}	± 200	—	V
3	Charge device model (CDM)	V_{CDM}	± 500	—	V
4	Latch-up current at $T_A = 85^\circ\text{C}$	I_{LAT}	± 100	—	mA

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min.	Typical ¹	Max.	Unit
1		Operating voltage V_{DD} rising V_{DD} falling			2.0 ² 1.8		3.6	V
2	C	Output high voltage	V_{OH}	All I/O pins, low-drive strength $V_{DD} > 1.8\text{ V}$, $I_{Load} = -2\text{ mA}$	$V_{DD} - 0.5$	—	—	V
	P			All I/O pins, high-drive strength $V_{DD} > 2.7\text{ V}$, $I_{Load} = -10\text{ mA}$	$V_{DD} - 0.5$	—	—	
	C			$V_{DD} > 1.8\text{ V}$, $I_{Load} = -2\text{ mA}$	$V_{DD} - 0.5$	—	—	
3	D	Output high current Max total I_{OH} for all ports	I_{OHT}	—	—	—	100	mA
4	C	Output low voltage	V_{OL}	All I/O pins, low-drive strength $V_{DD} > 1.8\text{ V}$, $I_{Load} = 0.6\text{ mA}$	—	—	0.5	V
	P			All I/O pins, high-drive strength $V_{DD} > 2.7\text{ V}$, $I_{Load} = 10\text{ mA}$	—	—	0.5	
	C			$V_{DD} > 1.8\text{ V}$, $I_{Load} = 3\text{ mA}$	—	—	0.5	
5	D	Output low current Max total I_{OL} for all ports	I_{OLT}	—	—	—	100	mA
6	P	Input high voltage All digital inputs	V_{IH}	$V_{DD} > 2.7\text{ V}$	$0.70 \times V_{DD}$	—	—	V
	C			$V_{DD} > 1.8\text{ V}$	$0.85 \times V_{DD}$	—	—	
7	P	Input low voltage All digital inputs	V_{IL}	$V_{DD} > 2.7\text{ V}$	—	—	$0.35 \times V_{DD}$	V
	C			$V_{DD} > 1.8\text{ V}$	—	—	$0.30 \times V_{DD}$	
8	C	Input hysteresis All digital inputs	V_{hys}	—	$0.06 \times V_{DD}$	—	—	mV
9	P	Input leakage current All input only pins (per pin)	$ I_{In} $	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
10	P	Hi-Z (off-state) leakage current All input/output (per pin)	$ I_{OZ} $	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
11	P	Total leakage combined for all inputs and Hi-Z pins All input only and I/O	$ I_{OZTOT} $	$V_{In} = V_{DD}$ or V_{SS}	—	—	2	μA
12a	P	Pullup, pulldown resistors All digital inputs, when enabled (all I/O pins other than PTA5/IRQ/TCLK/RESET)	R_{PU} , R_{PD}	—	17.5	—	52.5	$\text{k}\Omega$

Table 7. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min.	Typical ¹	Max.	Unit
12b	C	Pullup, pulldown resistors (PTA5/IRQ/TCLK/RESET)	R_{PU} , R_{PD} (Note ³)	—	17.5	—	52.5	k Ω
13	C	DC injection current ^{4, 5, 6}	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-0.2	—	0.2	mA
		Total MCU limit, includes sum of all stressed pins	I_{IC}		-5	—	5	mA
14	C	Input capacitance, all pins	C_{in}	—	—	—	8	pF
15	C	RAM retention voltage	V_{RAM}	—	—	0.6	1.0	V
16	C	POR re-arm voltage ⁷	V_{POR}	—	0.9	1.4	2.0	V
17	D	POR re-arm time	t_{POR}	—	10	—	—	μ s
18	P	Low-voltage detection threshold	V_{LVD}	V_{DD} falling	1.80	1.84	1.88	V
				V_{DD} rising	1.88	1.92	1.96	
19	P	Low-voltage warning threshold	V_{LVW}	V_{DD} falling	2.08	2.14	2.24	V
				V_{DD} rising				
20	P	Low-voltage inhibit reset/recover hysteresis	V_{hys}	—	—	80	—	mV
21	P	Bandgap voltage reference ⁸	V_{BG}	—	1.15	1.17	1.18	V

¹ Typical values are measured at 25 °C. Characterized, not tested

² As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL} .

³ The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear higher when measured externally on the pin.

⁴ All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD} .

⁵ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁶ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁷ Maximum is highest voltage that POR is guaranteed.

⁸ Factory trimmed at $V_{DD} = 3.0$ V, Temp = 25 °C

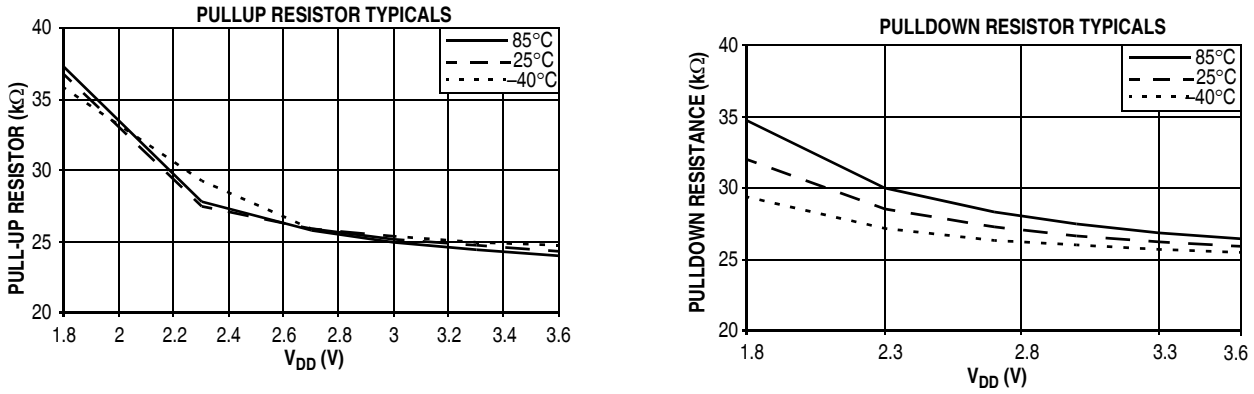


Figure 6. Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

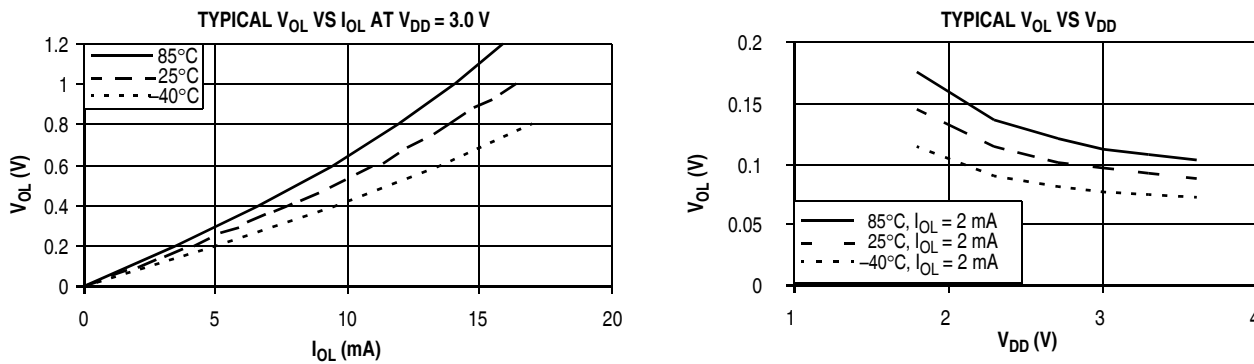


Figure 7. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

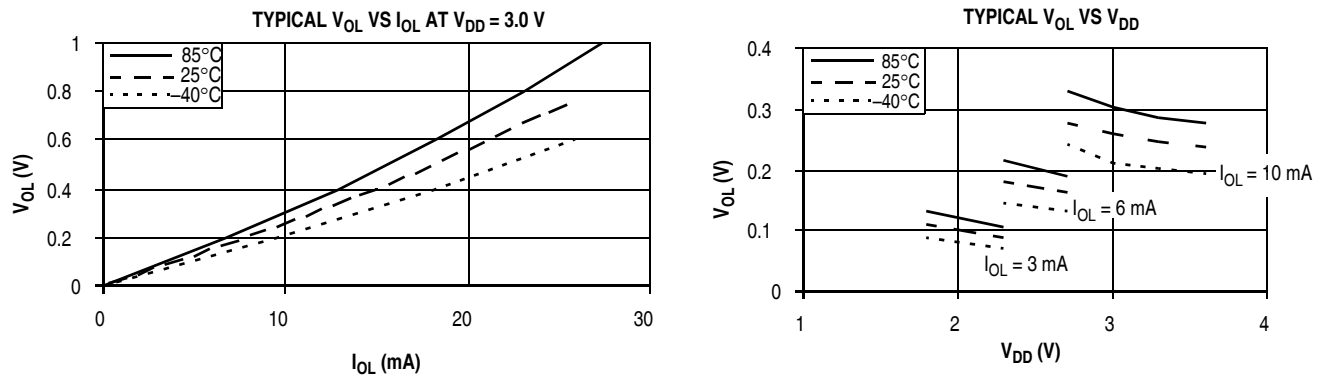


Figure 8. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

Electrical Characteristics

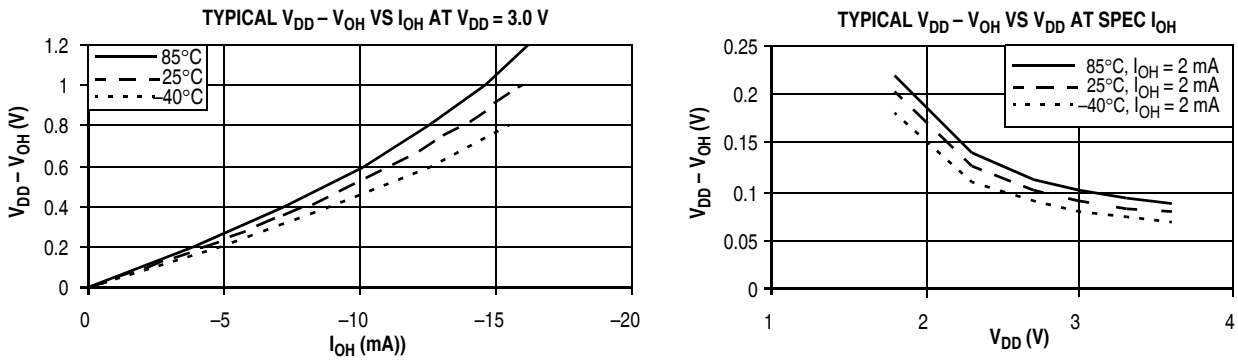


Figure 9. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

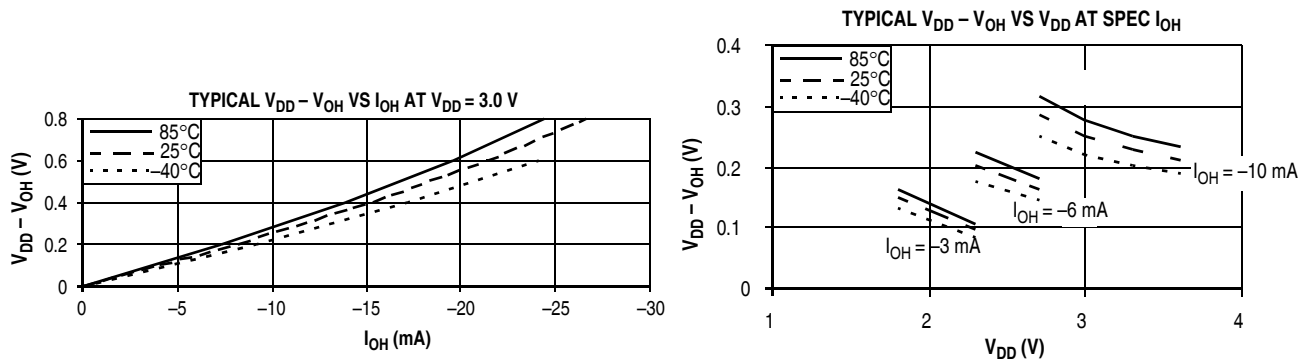


Figure 10. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical ¹	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	$R_{I_{DD}}$	10 MHz	3	5.60	8.2	mA	-40 to 85 °C
	1 MHz			0.80		—			
2	T	Run supply current FEI mode, all modules off	$R_{I_{DD}}$	10 MHz	3	3.60	—	mA	-40 to 85 °C
	T			1 MHz		0.51	—		
3	T	Run supply current LPRS = 0, all modules off	$R_{I_{DD}}$	16 kHz FBILP	3	165	—	μ A	-40 to 85 °C
	T			16 kHz FBELP		105	—		
4	T	Run supply current LPRS = 1, all modules off; running from flash	$R_{I_{DD}}$	16 kHz FBILP	3	77	—	μ A	-40 to 85 °C
	T			16 kHz FBELP		21	—		

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp (°C)
5	T	Run supply current LPRS = 1, all modules off; running from RAM	RI _{DD}	16 kHz FBILP	3	77	—	μA	-40 to 85 °C
	T			16 kHz FBELP		7.3	—		
6	T	Wait mode supply current FEI mode, all modules off	WI _{DD}	10 MHz	3	570	—	μA	-40 to 85 °C
	T			1 MHz		290	—		
7	T	Wait mode supply current LPRS = 1, all modules off	WI _{DD}	16 kHz FBELP	3	1	—	μA	-40 to 85 °C
8	P	Stop2 mode supply current	S2I _{DD}	—	3	0.3	0.65	μA	-40 to 25 °C
	C			—		0.5	0.8		70 °C
	P			—		1	2.5		85 °C
	C			—	2	0.25	0.50		-40 to 25 °C
	C			—		0.3	0.6		70 °C
	C			—		0.7	2.0		85 °C
9	P	Stop3 mode supply current no clocks active	S3I _{DD}	—	3	0.4	0.8	μA	-40 to 25 °C
	C			—		1.0	1.8		70 °C
	P			—		3	6		85 °C
	C			—	2	0.35	0.60		-40 to 25 °C
	C			—		0.8	1.5		70 °C
	C			—		2.5	5.5		85 °C

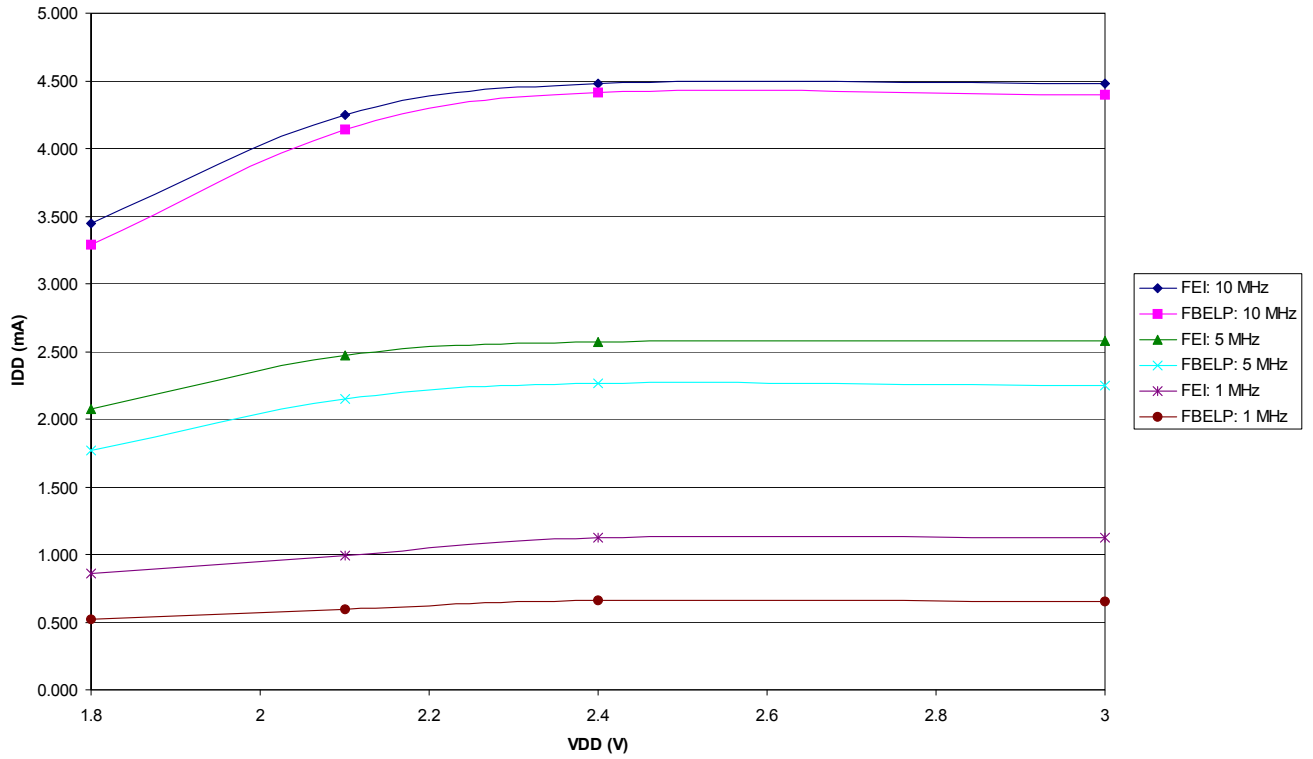
¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				-40°C	25°C	70°C	85°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN ¹	—	63	70	77	81	μA
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD ¹	LVDSE = 1	90	100	110	115	μA
6	T	ACMP ¹	Not using the bandgap (BGBE = 0)	18	20	22	23	μA
7	T	ADC ¹	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	μA

¹ Not available in stop2 mode.

Electrical Characteristics



**Figure 11. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD}
(ADC off, All Other Modules Enabled)**

3.8 External Oscillator (XOSCVLP) Characteristics

Refer to [Figure 12](#) and [Figure 13](#) for crystal or resonator circuits.

Table 10. XOSCVLP Specifications (Temperature Range = -40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical ¹	Max.	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	f_{lo}	32	—	38.4	kHz MHz MHz
		Low range (RANGE = 0)	f_{hi}	1	—	16	
		High range (RANGE = 1), high gain (HGO = 1), FBELP mode High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	1	—	8	
2	D	Load capacitors Low range (RANGE=0), low power (HGO = 0) Other oscillator settings	C_1, C_2	See Note ² See Note ³			
3	D	Feedback resistor	R_F	—	—	—	M Ω
		Low range, low power (RANGE = 0, HGO = 0) ²		—	10	—	
		Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)		—	1	—	
4	D	Series resistor —	R_S	—	—	—	k Ω
		Low range, low power (RANGE = 0, HGO = 0) ²		—	100	—	
		Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0)		—	0	—	
		High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
1 MHz	—	0	20				
5	C	Crystal start-up time ⁴	t_{CSTL}	—	600	—	ms
		Low range, low power		—	400	—	
		Low range, high gain		—	5	—	
		High range, low power High range, high gain		—	15	—	
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)	f_{extal}	0.03125	—	20	MHz MHz
		FEE mode FBE or FBELP mode		0	—	20	

¹ Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

² Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.

³ See crystal or resonator manufacturer's recommendation.

⁴ Proper PC board layout procedures must be followed to achieve specifications.

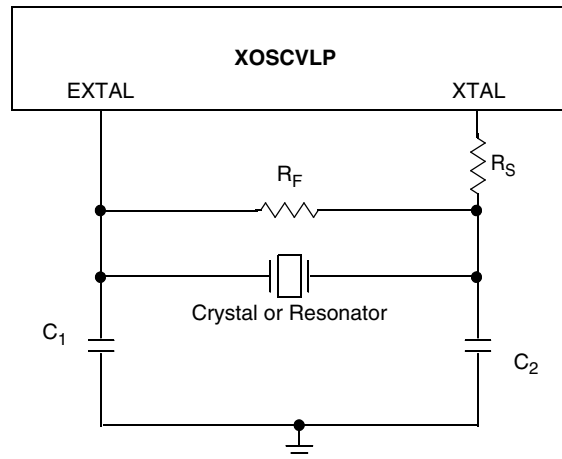


Figure 12. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

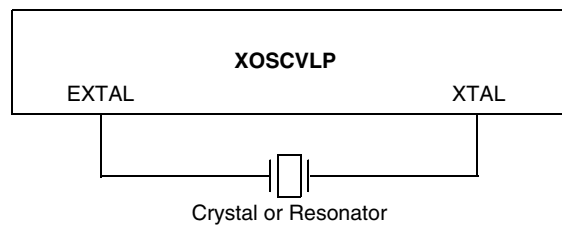


Figure 13. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical ¹	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at $V_{DD} = 3.6\text{ V}$ and temperature = 25 °C	f_{int_t}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed	f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time	t_{IRST}	—	5	10	μs
4	P	DCO output frequency range — trimmed ²	f_{dco_t}	16	—	20	MHz
		Low range (DRS = 00)					
5	P	DCO output frequency ² Reference = 32768 Hz and DMX32 = 1	f_{dco_DMX32}	—	19.92	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco_res_t}$	—	±0.1	±0.2	% f_{dco}

Table 11. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min.	Typical ¹	Max.	Unit
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{\text{dco_res_t}}$	—	± 0.2	± 0.4	% f_{dco}
8	C	Total deviation of DCO output from trimmed frequency ³ Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	$\Delta f_{\text{dco_t}}$	—	-1.0 to 0.5 ± 0.5	± 2 ± 1	% f_{dco}
10	C	FLL acquisition time ⁴	t_{Acquire}	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) ⁵	C_{Jitter}	—	0.02	0.2	% f_{dco}

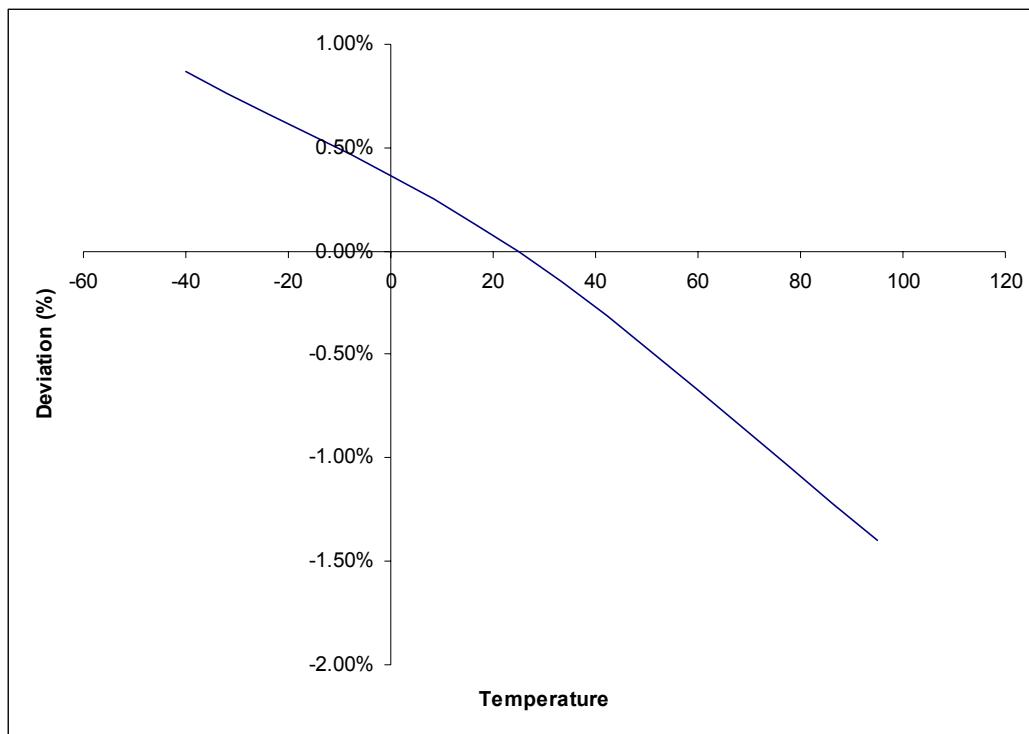
¹ Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

² The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

³ This parameter is characterized and not tested on each device.

⁴ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁵ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.


Figure 14. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 12. Control Timing

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	μs
3	D	External reset pulse width ²	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³	t_{MSH}	100	—	—	μs
7	D	IRQ pulse width Asynchronous path ² Synchronous path ⁴	t_{LIH}, t_{HIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path ² Synchronous path ⁴	t_{LIH}, t_{HIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) ⁵ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	16 23	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) ⁵ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	5 9	— —	ns
10	C	Voltage regulator recovery time	t_{VRR}	—	4	—	μs

¹ Typical values are based on characterization data at $V_{DD} = 3.0 V$, 25 °C unless otherwise stated.
² This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
³ To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .
⁴ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
⁵ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40^{\circ}C$ to $85^{\circ}C$.

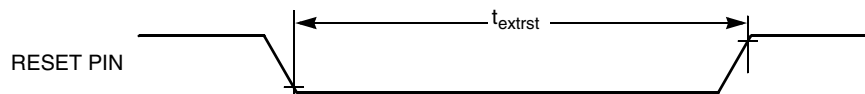
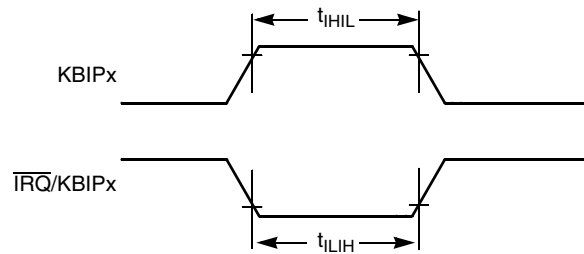


Figure 15. Reset Timing


 Figure 16. $\overline{\text{IRQ}}/\text{KBIPx}$ Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 13. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{\text{Bus}}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

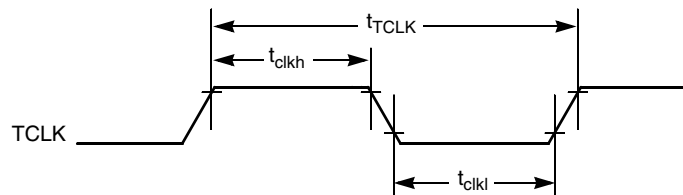


Figure 17. Timer External Clock

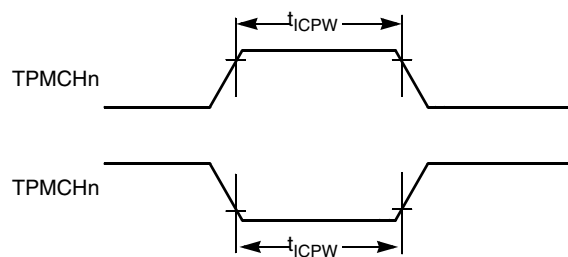


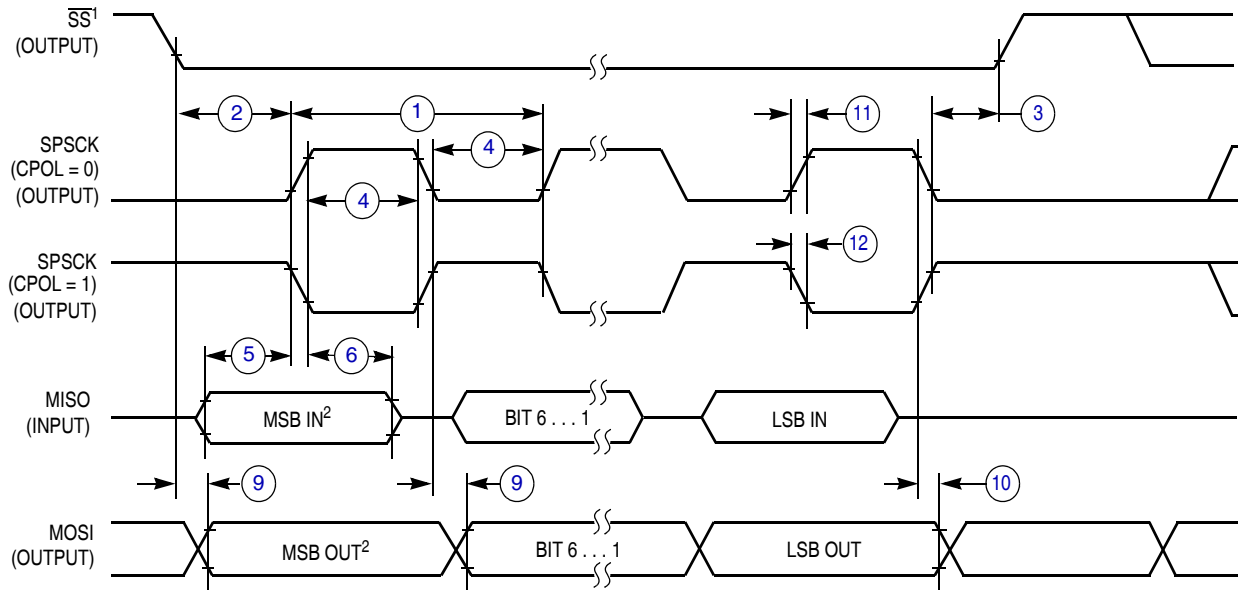
Figure 18. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 14 and Figure 19 through Figure 22 describe the timing requirements for the SPI system.

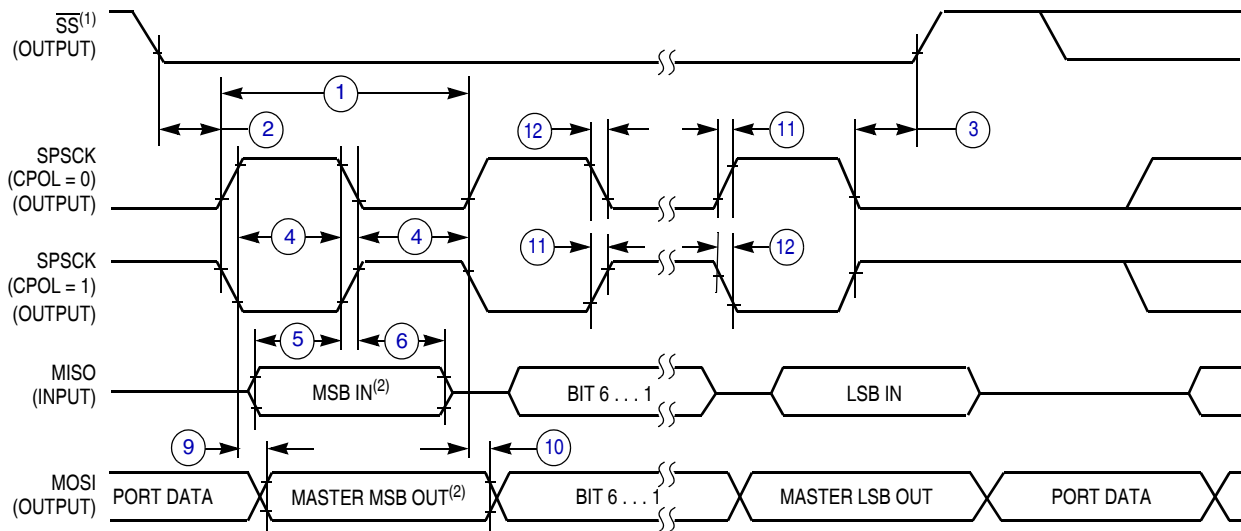
Table 14. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTES:

1. $\overline{SS}^{(1)}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. SPI Master Timing (CPHA = 0)


NOTES:

1. $\overline{SS}^{(1)}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 20. SPI Master Timing (CPHA = 1)