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Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC9S08QG8
MC9S08QG4

Data Sheet

HCS08
Microcontrollers

MC9S08QG8
Rev. 5
11/2009

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MC9S08QG8/4 Features

8-Bit HCS08 Central Processor Unit (CPU)

- 20-MHz HCS08 CPU (central processor unit)
- HC08 instruction set with added BGND instruction
- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data Debug module supports both tag and force breakpoints
- Support for up to 32 interrupt/reset sources

Memory Options

- FLASH read/program/erase over full operating voltage and temperature
- MC9S08QG8 — 8 Kbytes FLASH, 512 bytes RAM MC9S08QG4 — 4 Kbytes FLASH, 256 bytes RAM

Power-Saving Modes

- Wait plus three stops

Clock Source Options

- **ICS** — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 10 MHz
- **XOSC** — Low-power oscillator module with software selectable crystal or ceramic resonator range, 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz, and supports external clock source input up to 20 MHz

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect

Peripherals

- **ADC** — 8-channel, 10-bit analog-to-digital converter with automatic compare function, asynchronous clock source, temperature sensor, and internal bandgap reference channel; ADC is hardware triggerable using the RTI counter
- **ACMP** — Analog comparator module with option to compare to internal reference; output can be optionally routed to TPM module
- **SCI** — Serial communications interface module with option for 13-bit break capabilities
- **SPI** — Serial peripheral interface module
- **IIC** — Inter-integrated circuit bus module
- **TPM**— 2-channel timer/pulse-width modulator; each channel can be used for input capture, output compare, buffered edge-aligned PWM, or buffered center-aligned PWM
- **MTIM** — 8-bit modulo timer module with 8-bit prescaler
- **KBI** — 8-pin keyboard interrupt module with software selectable polarity on edge or edge/level modes

Input/Output

- 12 general-purpose input/output (I/O) pins, one input-only pin and one output-only pin; outputs 10 mA each, 60 mA max for package
- Software selectable pullups on ports when used as input
- Software selectable slew rate control and drive strength on ports when used as output
- Internal pullup on $\overline{\text{RESET}}$ and $\overline{\text{IRQ}}$ pins to reduce customer system cost

Development Support

- Single-wire background debug interface
- On-chip, in-circuit emulation (ICE) with real-time bus capture

Package Options

- 24-pin quad flat no lead (QFN) package
- 16-pin plastic dual in-line package (PDIP) — MC9S08QG8 only
- 16-pin quad flat no lead (QFN) package
- 16-pin thin shrink small outline package (TSSOP)
- 8-pin dual flat no lead (DFN) package
- 8-pin PDIP — *MC9S08QG4 only*
- 8-pin narrow body small outline integrated circuit (SOIC) package

MC9S08QG8 Data Sheet

Covers MC9S08QG8
MC9S08QG4

MC9S08QG8
Rev. 5
11/2009

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev No.	Revision Date	Description of Changes
2 Draft A	06/08/2006	Previous version was 1.01; revision numbering will increment by integers from now on. Clarified PTA5 pullup behavior note; clarified that FCDIV is write once after reset; expanded FPROT/NVPROT register description added note for servicing the COP if the COP is enabled during an erase function; added requirements for using ACMP0 in ACMP introduction; added factory trim value section to ICS introduction; debug section added to Development Support chapter; updated RTI period and added RTI graph to control timing section; other minor grammar edits.
3	10/2007	Added 24-pin QFN package and updated the A-5. DC Characteristics table Supply Voltage row.
4	2/2008	Incorporated core team markups from shared review. See Project Sync issue #3313 for archive.
5	11/2009	Added new part number information for the maskset revision 4. Corrected bit 0 of KBISC register in the Table 4-2.

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Chapter 1
Device Overview

1.1 Introduction

The MC9S08QG8 is a member of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types. Refer to Table 1-1 for features associated with each device in this series.

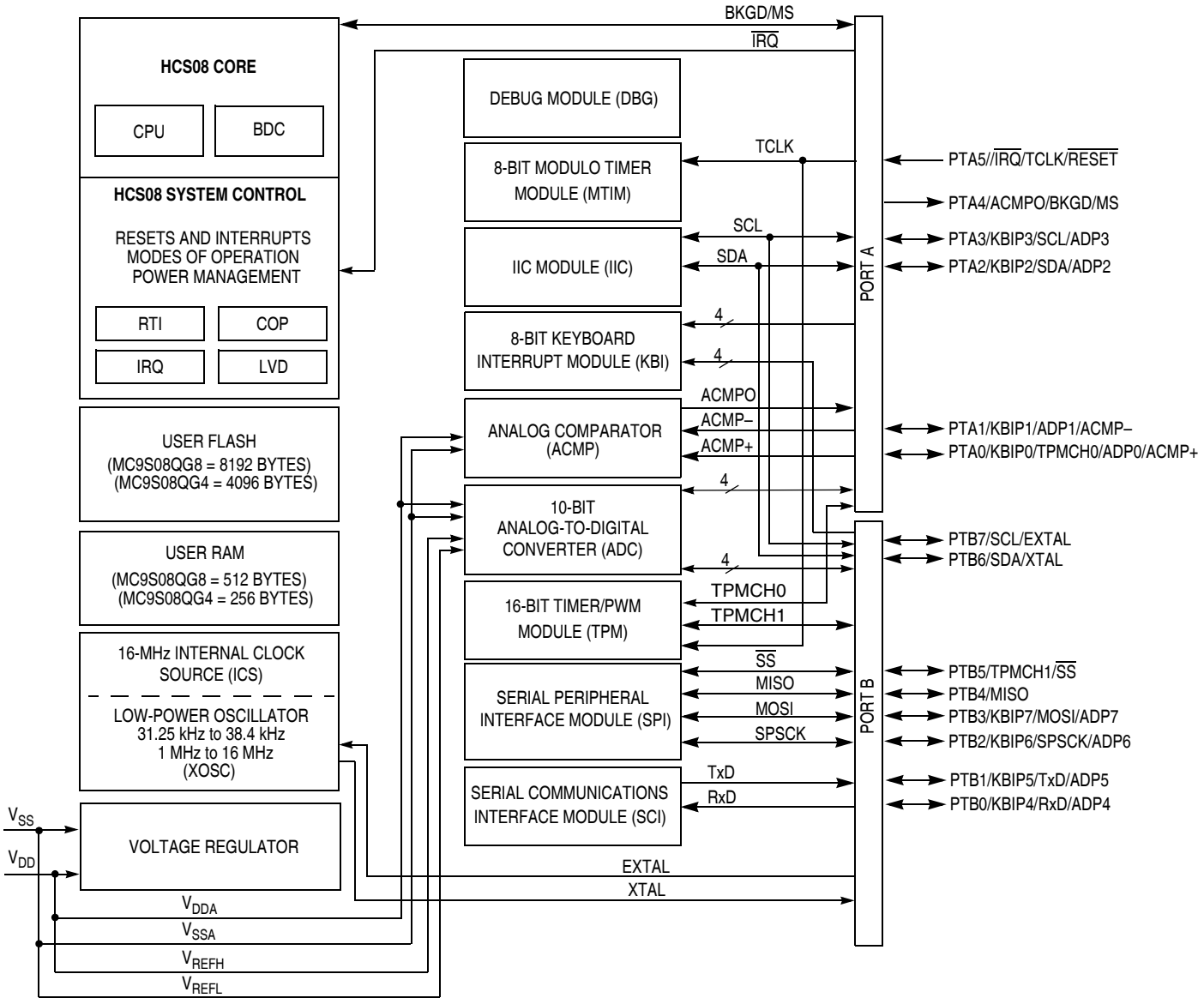
1.1.1 Devices in the MC9S08QG8/4 Series

Table 1-1 summarizes the features available in the MC9S08QG8/4 series of MCUs.

Table 1-1. Devices in the MC9S08QG8/4 Series

Feature	Device					
	MC9S08QG8			MC9S08QG4		
Package	24-Pin	16-Pin	8-Pin	24-Pin	16-Pin	8-Pin
FLASH	8K			4K		
RAM	512			256		
XOSC	yes	yes	no	yes	yes	no
ICS	yes			yes		
ACMP	yes			yes		
ADC	8-ch	8-ch	4-ch	8-ch	8-ch	4-ch
DBG	yes			yes	yes	yes
IIC	yes			yes		
IRQ	yes			yes		
KBI	8-pin	8-pin	4-pin	8-pin	8-pin	4-pin
MTIM	yes			yes		
SCI	yes	yes	no	yes	yes	no
SPI	yes	yes	no	yes	yes	no
TPM	2-ch	2-ch	1-ch	2-ch	2-ch	1-ch
I/O pins	12 I/O 1 Output only 1 Input only	12 I/O 1 Output only 1 Input only	4 I/O 1 Output only 1 Input only	12 I/O 1 Output only 1 Input only	12 I/O 1 Output only 1 Input only	4 I/O 1 Output only 1 Input only
Package Types	24 QFN	16 PDIP 16 QFN 16 TSSOP	8 DFN 8 SOIC	24 QFN	16 QFN 16 TSSOP	8 DFN 8 PDIP 8 SOIC

1.1.2 MCU Block Diagram



NOTES:
1. Not all pins or pin functions are available on all devices; see Table 1-1 for available functions on each device.
2. Port pins are software configurable with pullup device if input port.
3. Port pins are software configurable for output drive strength.
4. Port pins are software configurable for output slew rate control.
5. $\overline{IRQ}$ contains a software configurable (IRQPDD) pullup device if PTA5 enabled as $\overline{IRQ}$ pin function (IRQPE = 1).
6. $\overline{RESET}$ contains integrated pullup device if PTA5 enabled as reset pin function (RSTPE = 1).
7. PTA4 contains integrated pullup device if BKGD enabled (BKGDPE = 1).
8. SDA and SCL pin locations can be repositioned under software control (IICPS), defaults on PTA2 and PTA3.
9. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

Figure 1-1. MC9S08QG8/4 Block Diagram

Table 1-2 provides the functional versions of the on-chip modules.

Table 1-2. Versions of On-Chip Modules

Module		Version
Analog Comparator	(ACMP)	2
Analog-to-Digital Converter	(ADC)	1
Central Processing Unit	(CPU)	2
IIC Module	(IIC)	1
Internal Clock Source	(ICS)	1
Keyboard Interrupt	(KBI)	2
Modulo Timer	(MTIM)	1
Serial Communications Interface	(SCI)	3
Serial Peripheral Interface	(SPI)	3
Timer Pulse-Width Modulator	(TPM)	2
Low-Power Oscillator	(XOSC)	1
Debug Module	(DBG)	2

System Clock Distribution

Figure 1-2 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function. All memory mapped registers associated with the modules are clocked with BUSCLK.

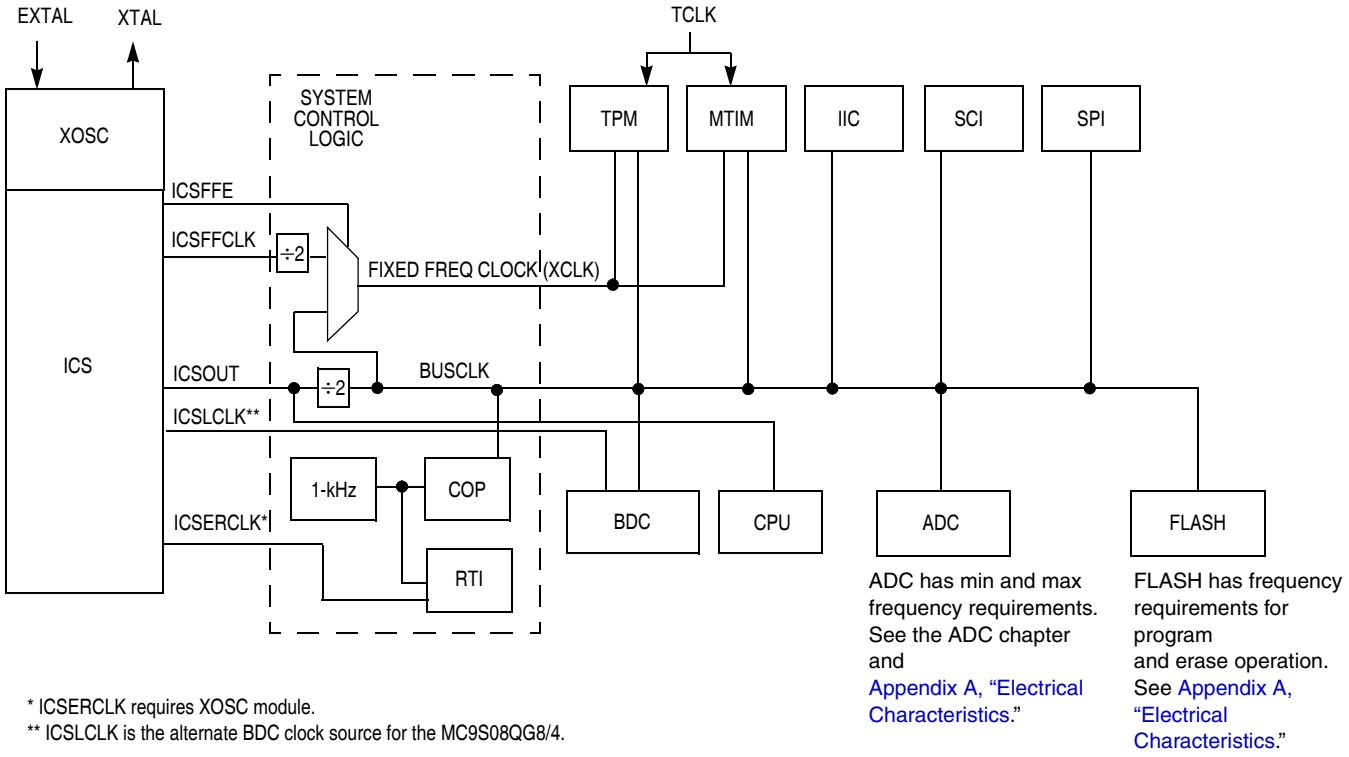


Figure 1-2. System Clock Distribution Diagram