Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC9S08RC8/16/32/60
MC9S08RD8/16/32/60
MC9S08RE8/16/32/60
MC9S08RG32/60

Data Sheet

HCS08
Microcontrollers

MC9S08RG60/D
Rev. 1.11
06/2005

freescale.com

freescale™
semiconductor

MC9S08RG60 Data Sheet

Covers: MC9S08RC8/16/32/60
MC9S08RD8/16/32/60
MC9S08RE8/16/32/60
MC9S08RG32/60

MC9S08RG60/D
Rev. 1.11
06/2005

freescale™
semiconductor

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com

The following revision history table summarizes changes contained in this document.

Version Number	Revision Date	Description of Changes
1.11	06/2005	Added 48 QFN package and official mechanical drawings; suppled TBD values for IRO V_{OL}; updated t_{RTI} values; re-emphasized that KBI2 will not wake the MCU from stop2 mode.

List of Chapters

Contents

Section Number **Title** **Page**

Chapter 1
Introduction

Chapter 2
Pins and Connections

Chapter 3
Modes of Operation

Chapter 4
Memory

Chapter 5
Resets, Interrupts, and System Configuration

Chapter 6
Parallel Input/Output

Chapter 7
Central Processor Unit (S08CPUV2)

Chapter 8
Carrier Modulator Timer (S08CMTV1)

Chapter 9
Keyboard Interrupt (S08KBIV1)

Chapter 10
Timer/PWM Module (S08TPMV1)

Chapter 11
Serial Communications Interface (S08SCIV1)

Chapter 12
Serial Communications Interface (S08SCIV1)

Chapter 13
Serial Peripheral Interface (S08SPIV3)

Chapter 14
Analog Comparator (S08ACMPV1)

Chapter 15
Development Support

Appendix A
Electrical Characteristics

Appendix B
Ordering Information and Mechanical Drawings

Chapter 1
Introduction

1.1 Overview

The MC9S08RC/RD/RE/RG are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in this family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.2 Features

Features of the MC9S08RC/RD/RE/RG Family of devices are listed here. Please see Table 1-1 for the features that are available on the different family members.

HCS08 CPU (Central Processor Unit)	• Object code fully upward-compatible with M68HC05 and M68HC08 Families • HC08 instruction set with added BGND instruction • Support for up to 32 interrupt/reset sources • Power-saving modes: wait plus three stops
On-Chip Memory	• On-chip in-circuit programmable FLASH memory with block protection and security option • On-chip random-access memory (RAM)
Oscillator (OSC)	• Low power oscillator capable of operating from crystal or resonator from 1 to 16 MHz • 8 MHz internal bus frequency
Analog Comparator (ACMP1)	• On-chip analog comparator with internal reference (ACMP1) • Full rail-to-rail supply operation • Option to compare to a fixed internal bandgap reference voltage
Serial Communications Interface Module (SCI1)	• Full-duplex, standard non-return-to-zero (NRZ) format • Double-buffered transmitter and receiver with separate enables • Programmable 8-bit or 9-bit character length • Programmable baud rates (13-bit modulo divider)
Serial Peripheral Interface Module (SPI1)	• Master or slave mode operation • Full-duplex or single-wire bidirectional option • Programmable transmit bit rate • Double-buffered transmit and receive • Serial clock phase and polarity options • Slave select output • Selectable MSB-first or LSB-first shifting

Timer/Pulse-Width Modulator (TPM1)	• 2-channel, 16-bit timer/pulse-width modulator (TPM1) module that can operate as a free-running counter, a modulo counter, or an up-/down-counter when the TPM is configured for center-aligned PWM • Selectable input capture, output compare, and edge-aligned or center-aligned PWM capability on each channel
Keyboard Interrupt Ports (KBI1, KBI2)	• Providing 12 keyboard interrupts • Eight with falling-edge/low-level plus four with selectable polarity • KBI1 inputs can be configured for edge-only sensitivity or edge-and-level sensitivity
Carrier Modulator Timer (CMT)	• Dedicated infrared output (IRO) pin • Drives IRO pin for remote control communications • Can be disconnected from IRO pin and used as output compare timer • IRO output pin has high-current sink capability
Development Support	• Background debugging system (see also the Development Support chapter) • Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module) • Debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Debug module supports both tag and force breakpoints.
Port Pins	• Eight high-current pins (limited by maximum package dissipation) • Software selectable pullups on ports when used as input. Selection is on an individual port bit basis. During output mode, pullups are disengaged. • 39 general-purpose input/output (I/O) pins, depending on package selection
Package Options	• 28-pin plastic dual in-line package (PDIP) • 28-pin small outline integrated circuit (SOIC) • 32-pin low-profile quad flat package (LQFP) • 44-pin low-profile quad flat package (LQFP) • 48-pin quad flat package (QFN)
System Protection	• Optional computer operating properly (COP) reset • Low-voltage detection with reset or interrupt • Illegal opcode detection with reset • Illegal address detection with reset (some devices don't have illegal addresses)

1.2.1 Devices in the MC9S08RD/RE/RG Series

Table 1-1 lists the devices available in the MC9S08RD/RE/RG series and summarizes the differences in functions and configuration among them.

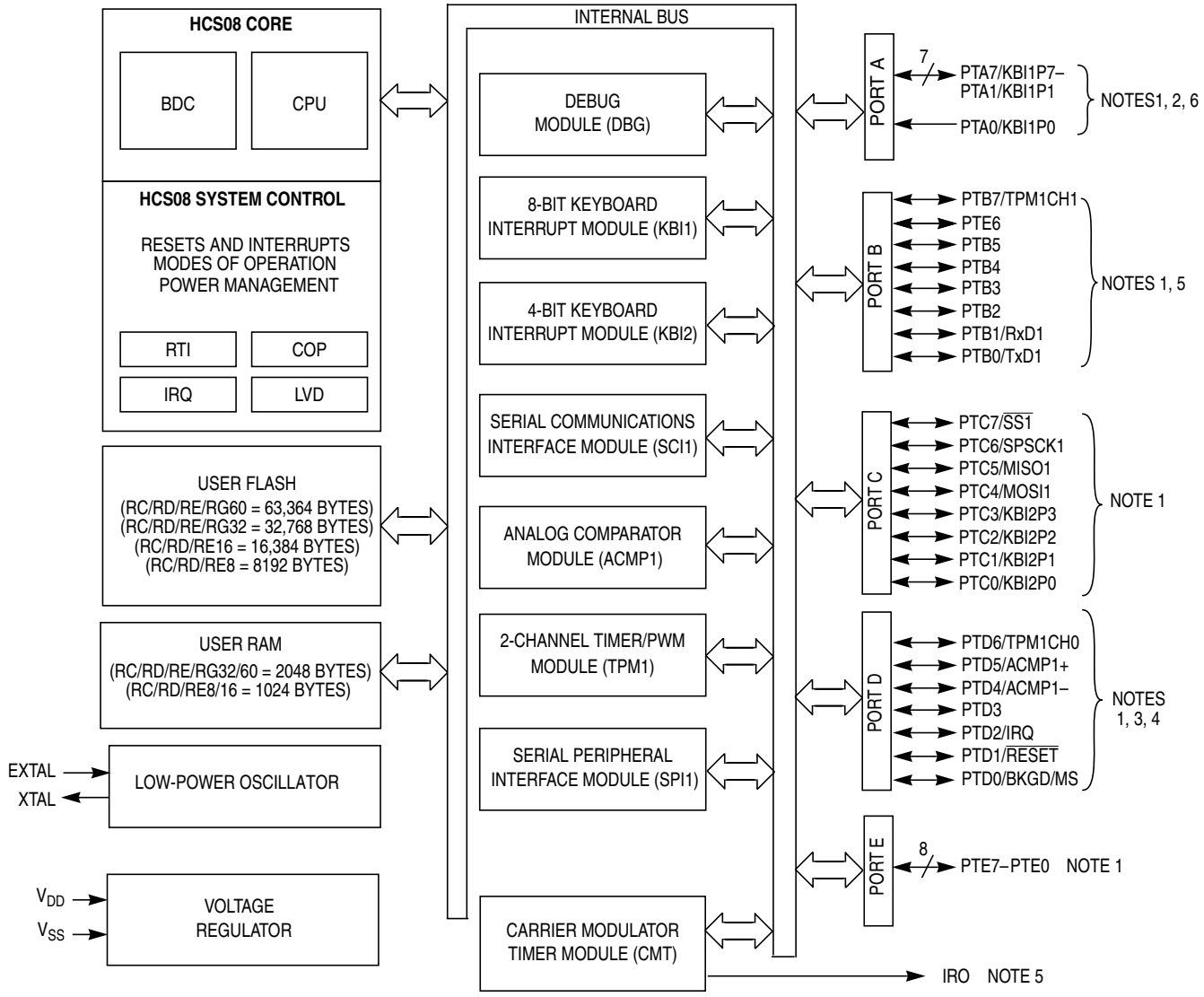
Table 1-1. Devices in the MC9S08RD/RE/RG Series

Device	FLASH	RAM	ACMP(1)	SCI	SPI
9S08RG32/60	32K/60K	2K/2K	Yes	Yes	Yes
9S08RE8/16/32/60	8/16K/32K/60K	1K/1K/2K/2K	Yes	Yes	No
9S08RD8/16/32/60	8/16K/32K/60K	1K/1K/2K/2K	No	Yes	No

1. Available only in 32-, 44-, and 48-pin LQFP packages.

1.3 MCU Block Diagram

This block diagram shows the structure of the MC9S08RC/RD/RE/RG MCUs



NOTES:

1. Port pins are software configurable with pullup device if input port
2. PTA0 does not have a clamp diode to V_{DD}. PTA0 should not be driven above V_{DD}. Also, PTA0 does not pullup to V_{DD} when internal pullup is enabled.
3. IRQ pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1)
4. The RESET pin contains integrated pullup device enabled if reset enabled (RSTPE = 1)
5. High current drive
6. Pins PTA[7:4] contain both pullup and pulldown devices. Pulldown enabled when KBI is enabled (KBIPEn = 1) and rising edge is selected (KBEDGn = 1).

Figure 1-1. MC9S08RC/RD/RE/RG Block Diagram

Table 1-2 lists the functional versions of the on-chip modules.

Table 1-2. Block Versions

Module	Version
Analog Comparator (ACMP)	1
Carrier Modulator Transmitter (CMT)	1
Keyboard Interrupt (KBI)	1
Serial Communications Interface (SCI)	1
Serial Peripheral Interface (SPI)	3
Timer Pulse-Width Modulator (TPM)	1
Central Processing Unit (CPU)	2
Debug Module (DBG)	1
FLASH	1
System Control	2

1.4 System Clock Distribution

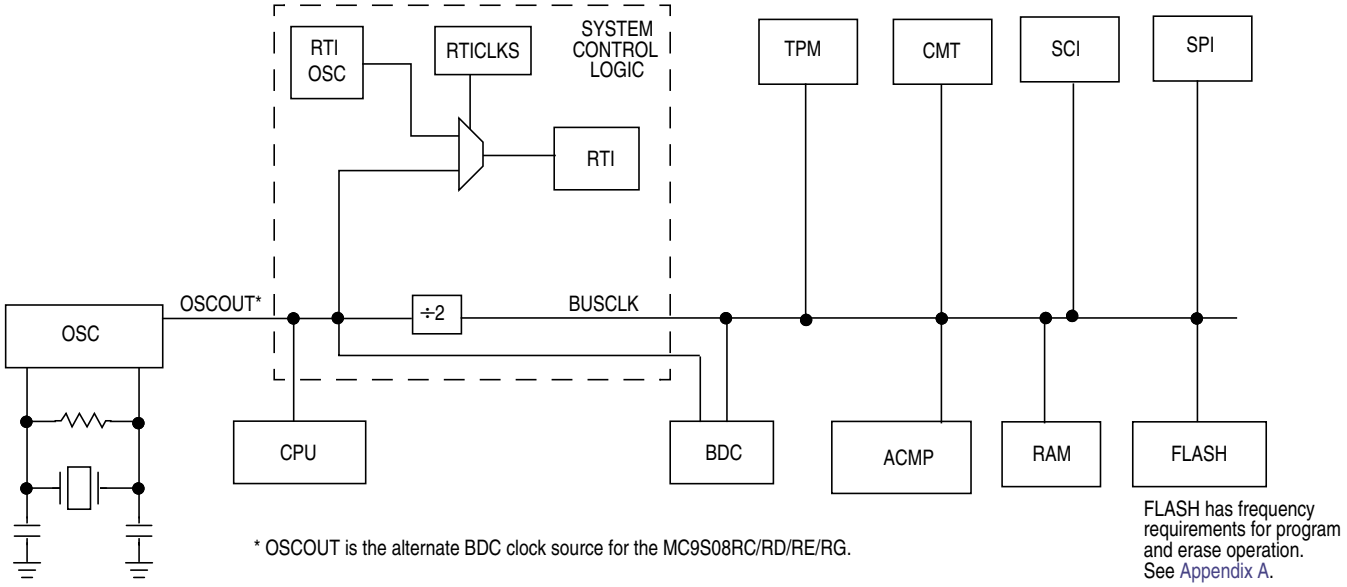


Figure 1-2. System Clock Distribution Diagram

Table 1-2 shows a simplified clock connection diagram for the MCU. The CPU operates at the input frequency of the oscillator. The bus clock frequency is half of the oscillator frequency and is used by all of the internal circuits with the exception of the CPU and RTI. The RTI can use either the oscillator input or the internal RTI oscillator as its clock source.

Chapter 2
Pins and Connections

2.1 Introduction

This section describes signals that connect to package pins. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals.

2.2 Device Pin Assignment

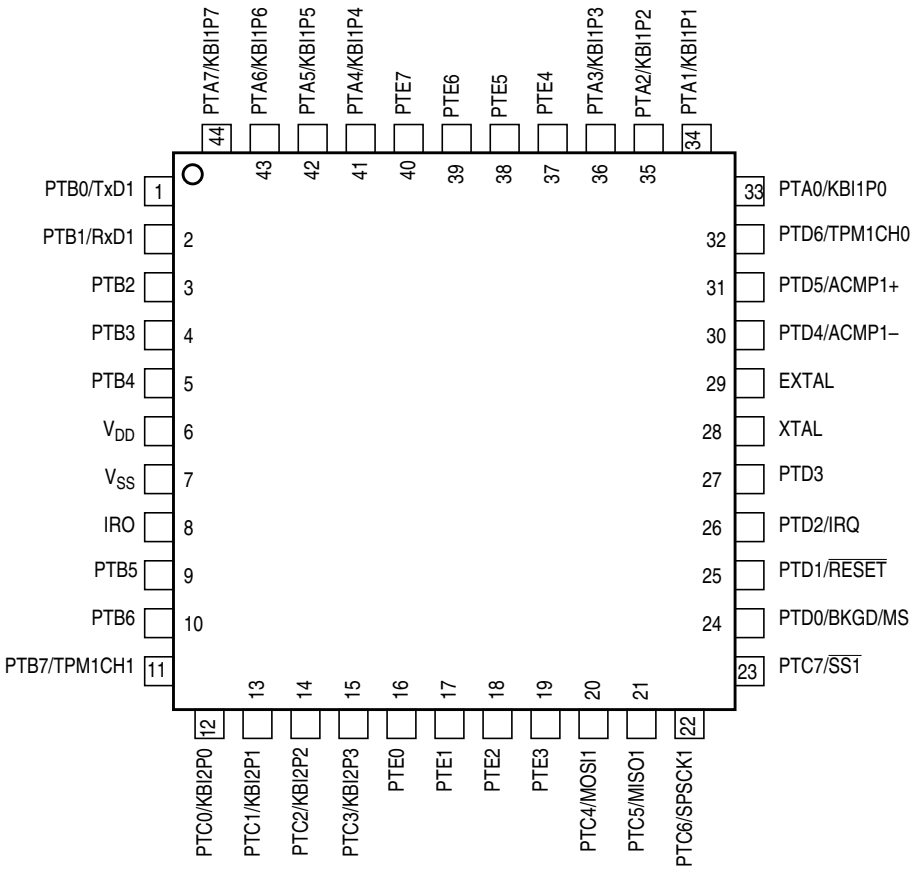


Figure 2-1. MC9S08RC/RD/RE/RG in 44-Pin LQFP Package

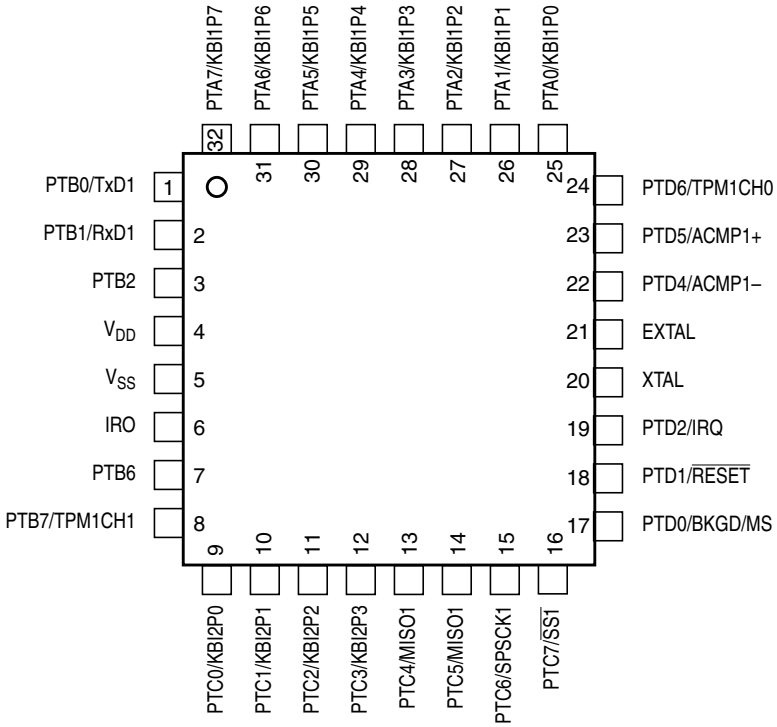


Figure 2-2. MC9S08RC/RD/RE/RG in 32-Pin LQFP Package

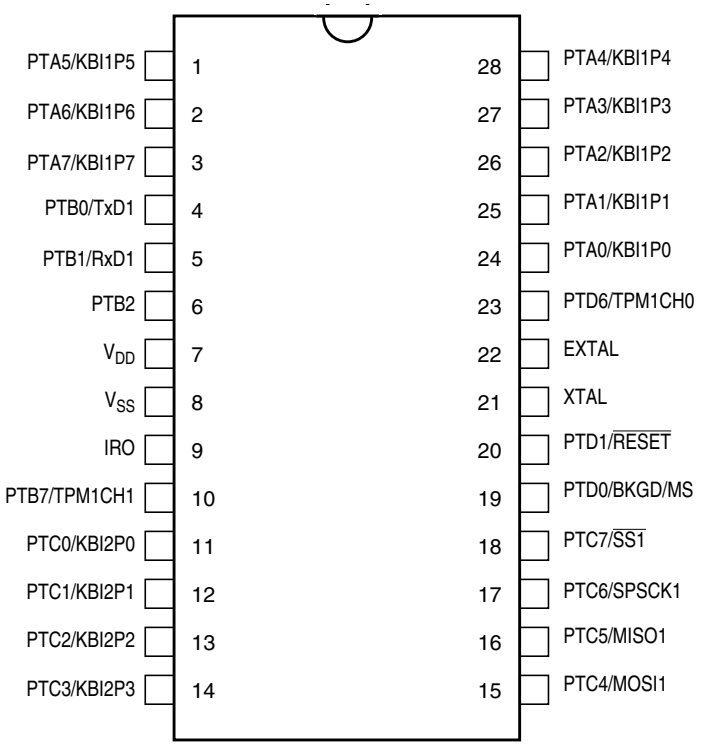


Figure 2-3. MC9S08RC/RD/RE/RG in 28-Pin SOIC Package and 28-Pin PDIP Package

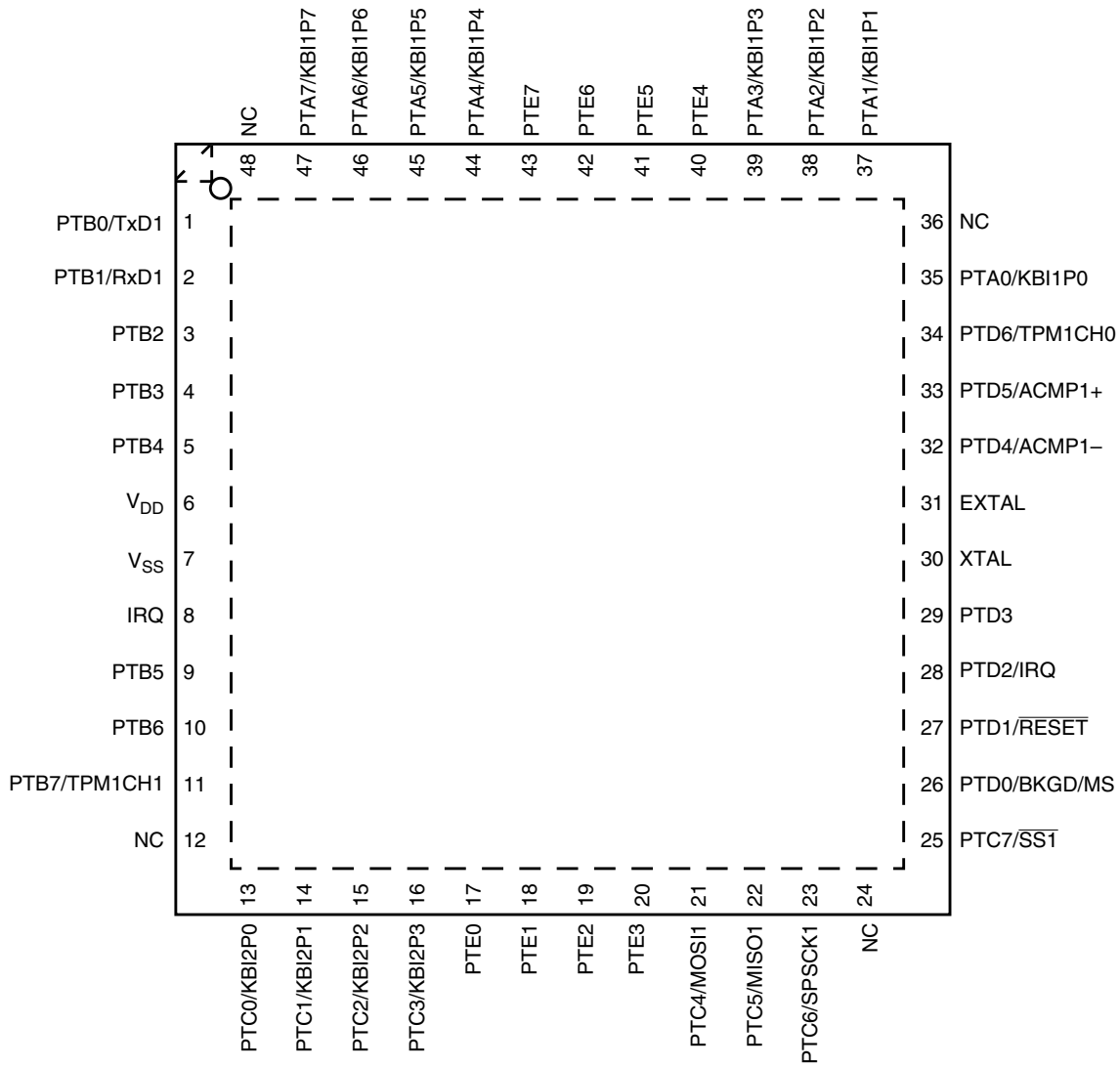
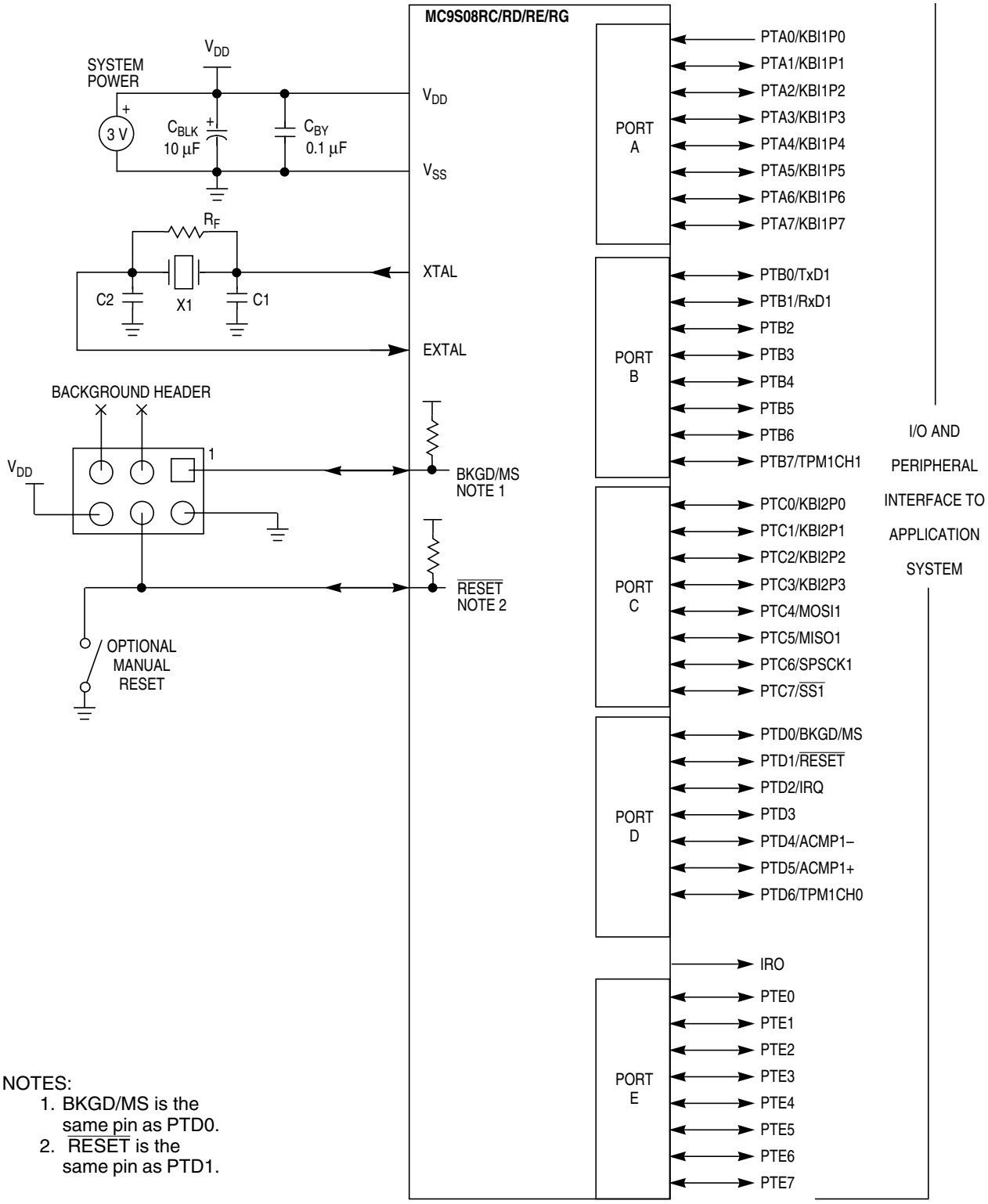


Figure 2-4. MC9S08RC/RD/RE/RG in 48-Pin QFN Package

2.3 Recommended System Connections

Figure 2-5 shows pin connections that are common to almost all MC9S08RC/RD/RE/RG application systems. A more detailed discussion of system connections follows.



NOTES:
1. BKGD/MS is the same pin as PTD0.
2. RESET is the same pin as PTD1.

Figure 2-5. Basic System Connections

2.3.1 Power

V_{DD} and V_{SS} are the primary power supply pins for the MCU. This voltage source supplies power to all I/O buffer circuitry and to an internal voltage regulator. The internal voltage regulator provides a regulated lower-voltage source to the CPU and other internal circuitry of the MCU.

Typically, application systems have two separate capacitors across the power pins. In this case, there should be a bulk electrolytic capacitor, such as a 10-µF tantalum capacitor, to provide bulk charge storage for the overall system and a 0.1-µF ceramic bypass capacitor located as near to the MCU power pins as practical to suppress high-frequency noise.

2.3.2 Oscillator

The oscillator in the MC9S08RC/RD/RE/RG is a traditional Pierce oscillator that can accommodate a crystal or ceramic resonator in the range of 1 MHz to 16 MHz.

Refer to Figure 2-5 for the following discussion. R_F should be a low-inductance resistor such as a carbon composition resistor. Wire-wound resistors, and some metal film resistors, have too much inductance. C1 and C2 normally should be high-quality ceramic capacitors specifically designed for high-frequency applications.

R_F is used to provide a bias path to keep the EXTAL input in its linear range during crystal startup and its value is not generally critical. Typical systems use 1 MΩ. Higher values are sensitive to humidity and lower values reduce gain and (in extreme cases) could prevent startup.

C1 and C2 are typically in the 5-pF to 25-pF range and are chosen to match the requirements of a specific crystal or resonator. Be sure to take into account printed circuit board (PCB) capacitance and MCU pin capacitance when sizing C1 and C2. The crystal manufacturer typically specifies a load capacitance that is the series combination of C1 and C2, which are usually the same size. As a first-order approximation, use 5 pF as an estimate of combined pin and PCB capacitance for each oscillator pin (EXTAL and XTAL).

2.3.3 PTD1/$\overline{\text{RESET}}$

The external pin reset function is shared with an output-only port function on the PTD1/$\overline{\text{RESET}}$ pin. The reset function is enabled when RSTPE in SOPT is set. RSTPE is set following any reset of the MCU and must be cleared in order to use this pin as an output-only port.

Whenever any reset is initiated (whether from an external signal or from an internal system), the reset pin is driven low for about 34 cycles of f_{Self_reset}, released, and sampled again about 38 cycles of f_{Self_reset} later. If reset was caused by an internal source such as low-voltage reset or watchdog timeout, the circuitry expects the reset pin sample to return a logic 1. If the pin is still low at this sample point, the reset is assumed to be from an external source. The reset circuitry decodes the cause of reset and records it by setting a corresponding bit in the system control reset status register (SRS).

Never connect any significant capacitance to the reset pin because that would interfere with the circuit and sequence that detects the source of reset. If an external capacitance prevents the reset pin from rising to a valid logic 1 before the reset sample point, all resets will appear to be external resets.