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MC9S08SH32
MC9S08SH16

Data Sheet

HCS08
Microcontrollers

MC9S08SH32
Rev. 3
3/2014

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MC9S08SH32 Series Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

On-Chip Memory

- FLASH read/program/erase over full operating voltage and temperature
- Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode
- Very low power real time counter for use in run, wait, and stop

Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; 1.5% deviation using internal temperature compensation.
- ICS supports bus frequencies from 2 MHz to 20 MHz.

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect

Development Support

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip, in-circuit emulation (ICE) debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow address and event-only data. Debug module supports both tag and force breakpoints.

Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5 μs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel; runs in stop3
- **ACMP** — Analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be optionally routed to TPM module; runs in stop3
- **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- **SPI** — Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
- **MTIM** — 8-bit modulo counter with 8-bit prescaler and overflow interrupt
- **TPMx** — Two 2-channel timer pwm modules (TPM1, TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
- **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components, runs in all MCU modes

Input/Output

- 23 general purpose I/O pins (GPIOs) and 1 output-only pin
- 8 interrupt pins with selectable polarity
- Ganged output option for PTB[5:2] and PTC[3:0]; allows single write to change state of multiple pins
- Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins.

Package Options

- 28-TSSOP, 28-SOIC, 20-TSSOP, 16-TSSOP

MC9S08SH32 Data Sheet

Covers MC9S08SH32
MC9S08SH16

MC9S08SH32
Rev. 3
3/2014

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	10/2007	Updated The ACMP and TPM modules to version 3 and made numerous revisions to the Electricals. Updated device numbering scheme.
2	4/2008	Updated some electricals and made some minor grammatical/formatting revisions. Corrected the SPI block module version. Removed incorrect ADC temperature sensor value from the Features section. Updated the package information with a sample mask set identifier.
3	3/2014	Added a note to the Section 9.1, “Introduction”; updated Section 11.4.5, “Internal Reference Clock”; updated Section A.14.1, “Radiated Emissions”; updated Figure 4-1, Figure 4-6; updated Table 4-4; updated Table 7-2.

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Chapter 1
Device Overview

The MC9S08SH32 members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.1 Devices in the MC9S08SH32 Series

Table 1-1 summarizes the feature set available in the MC9S08SH32 series of MCUs.

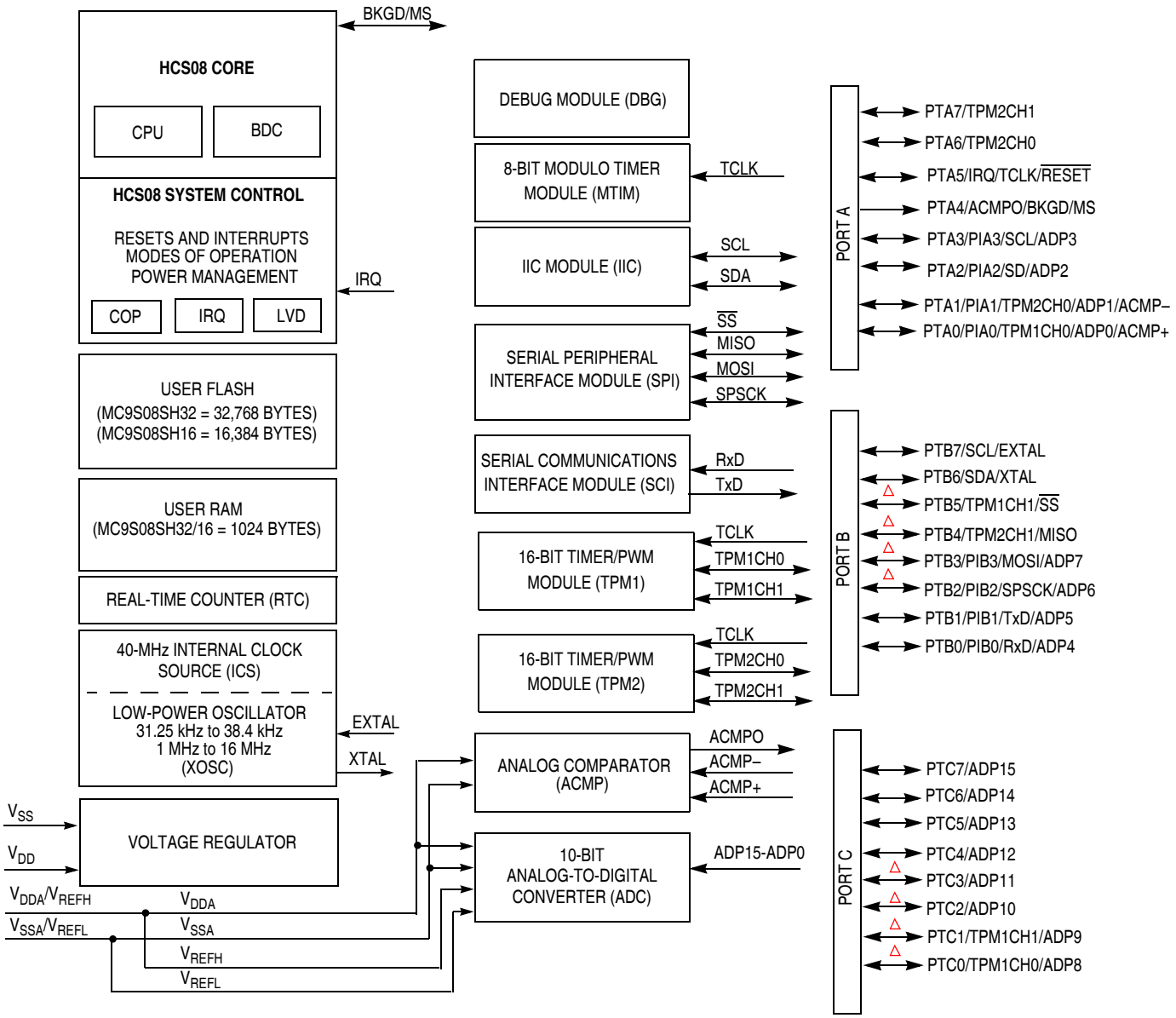
Table 1-1. MC9S08SH32 Series Features by MCU and Package

Feature	9S08SH32			9S08SH16		
FLASH size (bytes)	32768			16384		
RAM size (bytes)	1024					
Pin quantity	28	20	16	28	20	16
ACMP	yes					
ADC channels	16	12	8	16	12	8
DBG	yes					
ICS	yes					
IIC	yes					
IRQ	yes					
MTIM	yes					
Pin Interrupts	8					
Pin I/O [1]	23	17	13	23	17	13
RTC	yes					
SCI	yes					
SPI	yes					
TPM1 channels	2					
TPM2 channels	2					
XOSC	yes					

[1] Port I/O count does not include the output-only PTA4/ACMPO/BKGD/MS.

1.2 MCU Block Diagram

The block diagram in Figure 1-1 shows the structure of the MC9S08SH32 Series MCU.



△ = Pin can be enabled as part of the ganged output drive feature

NOTE: PTC7-PTC0 and PTA7-PTA6 not available on 16--pin Packages

PTC7-PTC4 and PTA7-PTA6 not available on 20-pin Packages

For the 16-pin and 20-pin packages: V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL}, are double bonded to V_{DD} and V_{SS} respectively.

When PTA4 is configured as BKGD, pin becomes bi-directional.

Figure 1-1. MC9S08SH32 Series Block Diagram

Table 1-2 provides the functional version of the on-chip modules

Table 1-2. Module Versions

Module		Version
Analog Comparator (5V)	(ACMP)	3
Analog-to-Digital Converter	(ADC)	1
Central Processor Unit	(CPU)	3
Inter-Integrated Circuit	(IIC)	2
Internal Clock Source	(ICS)	2
Low Power Oscillator	(XOSC)	1
Modulo Timer	(MTIM)	1
On-Chip In-Circuit Emulator	(DBG)	2
Real-Time Counter	(RTC)	1
Serial Peripheral Interface	(SPI)	3
Serial Communications Interface	(SCI)	4
Timer Pulse Width Modulator	(TPM)	3

1.3 System Clock Distribution

Figure 1-2 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function.

The following defines the clocks used in this MCU:

- BUSCLK — The frequency of the bus is always half of ICSOUT.
- ICSOUT — Primary output of the ICS and is twice the bus frequency.
- ICSLCLK — Development tools can select this clock source to speed up BDC communications in systems where the bus clock is configured to run at a very slow frequency.
- ICSERCLK — External reference clock can be selected as the RTC clock source and as the alternate clock for the ADC module.
- ICSIRCLK — Internal reference clock can be selected as the RTC clock source.
- ICSFFCLK — Fixed frequency clock can be selected as clock source for the TPM1, TPM2 and MTIM modules.
- LPOCLK — Independent 1-kHz clock source that can be selected as the clock source for the COP and RTC modules.
- TCLK — External input clock source for TPM1, TPM2 and MTIM and is referenced as TPMCLK in TPM chapters.

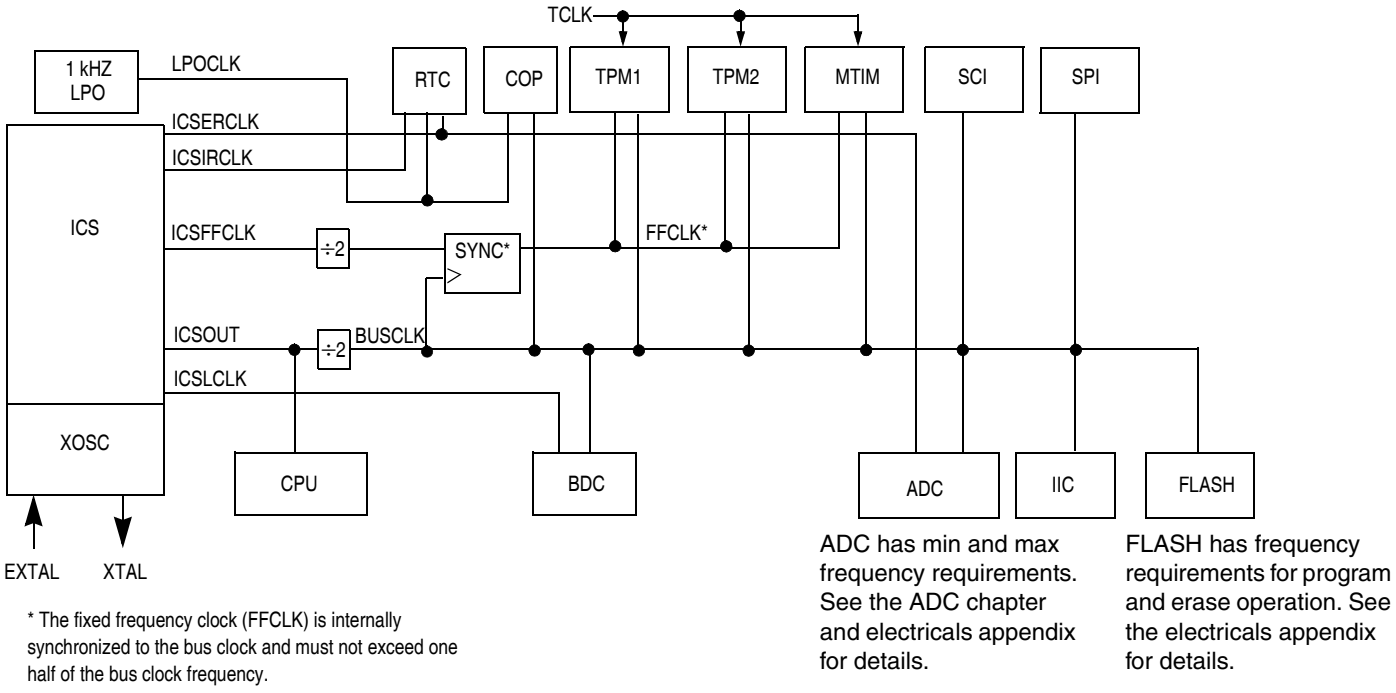


Figure 1-2. System Clock Distribution Diagram

Chapter 2
Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

Figure 2-1 - Figure 2-3 shows the pin assignments for the MC9S08SH32 Series devices.

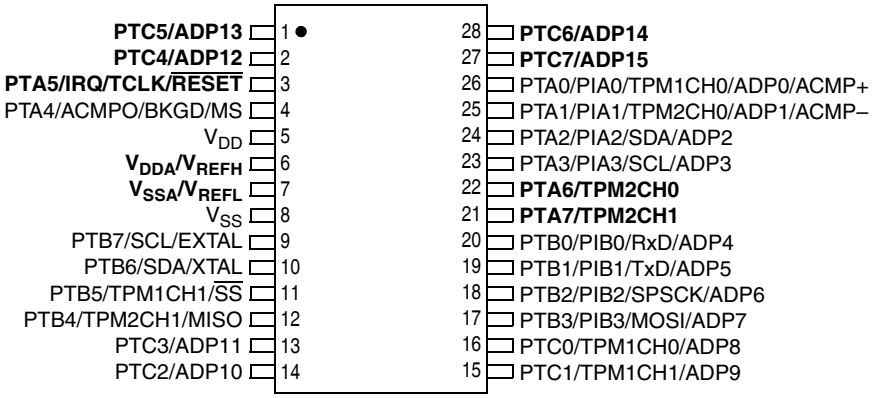


Figure 2-1. 28-Pin SOIC and TSSOP

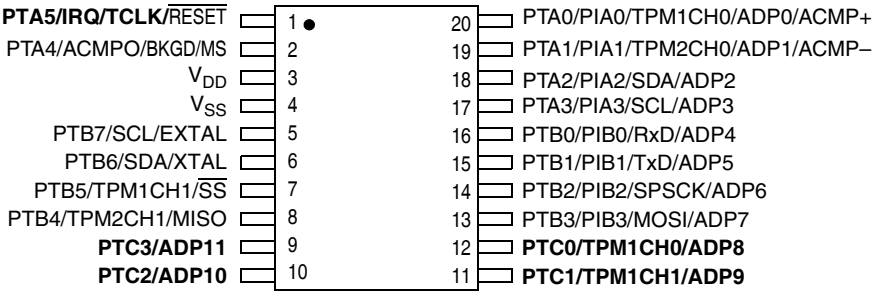


Figure 2-2. 20-Pin TSSOP

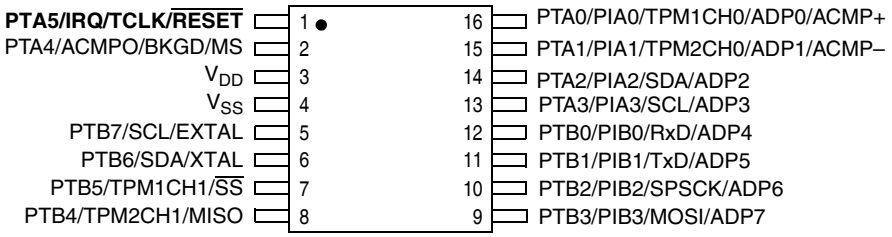
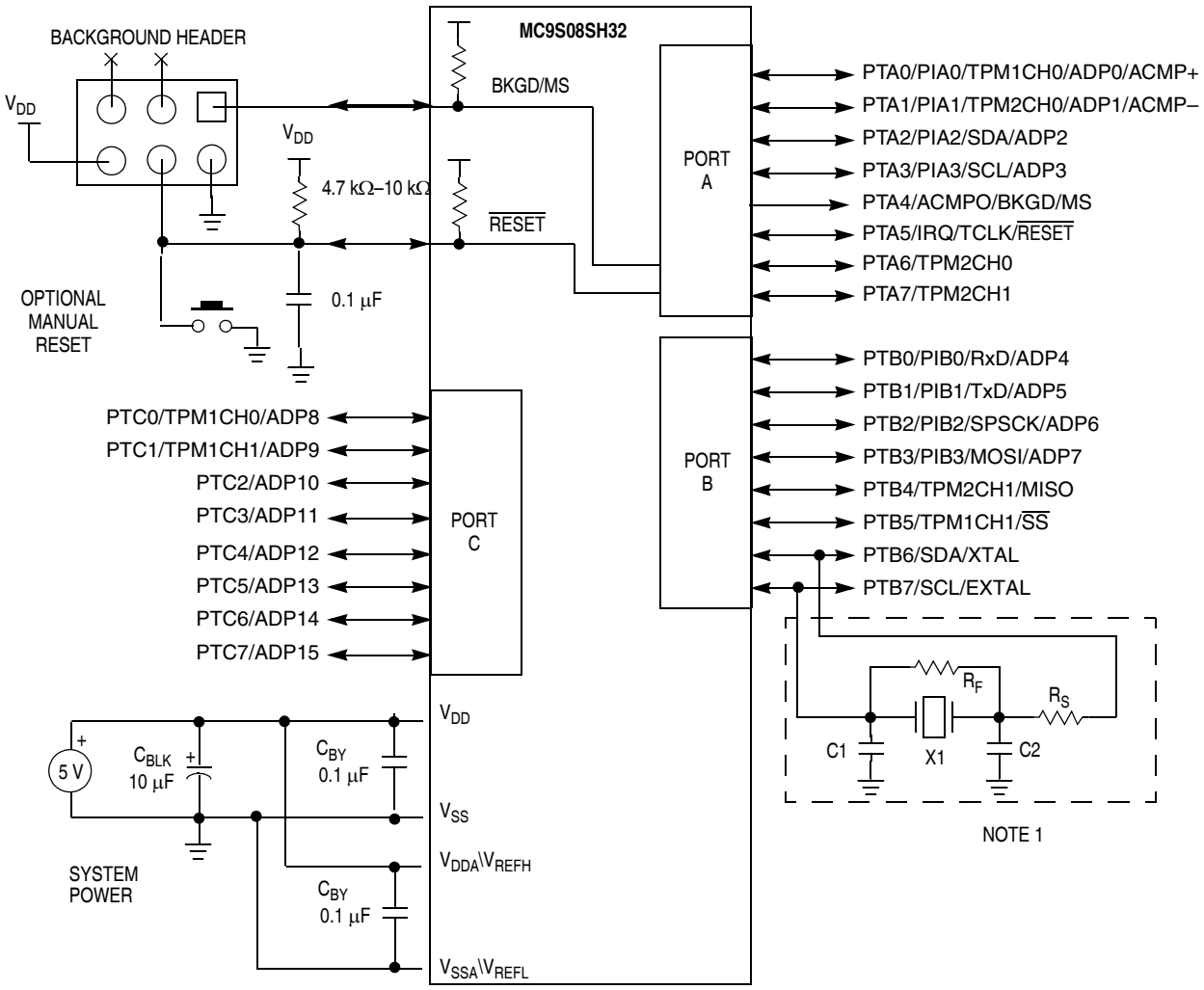


Figure 2-3. 16-Pin TSSOP

2.2 Recommended System Connections

Figure 2-4 shows pin connections that are common to MC9S08SH32 Series application systems.



NOTES:
1. External crystal circuit not required if using the internal clock option.
2. RESET pin can only be used to reset into user mode, you can not enter BDM using RESET pin. BDM can be entered by holding MS low during POR or writing a 1 to BDFR in SBDFR with MS low after issuing BDM command.
3. RC filter on RESET pin recommended for noisy environments.
4. For the 16-pin and 20-pin packages: V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL} are double bonded to V_{DD} and V_{SS} respectively.
5. When PTA4 is configured as BKGD, pin becomes bi-directional.

Figure 2-4. Basic System Connections