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Freescale Semiconductor
Data Sheet: Technical Data

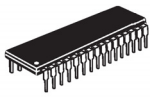
Document Number: MC9S08SV16
Rev. 2, 7/2009

MC9S08SV16 Series

Covers: MC9S08SV16 and MC9S08SV8

MC9S08SV16

32-Pin LQFP
873A-03



32-Pin SDIP
1376-02

Features:

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 2.7 V to 5.5 V across temperature range of –40 °C to 85 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Up to 16 KB flash read/program/erase over full operating voltage and temperature
  - Up to 1024-byte random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low power stop modes; reduced power wait mode
  - Allows clocks to remain enabled to specific peripherals in stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies up to 20 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints)
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes
- Peripherals
  - **IPC** — Interrupt priority controller to provide hardware based nested interrupt mechanism
  - **ADC** — 12-channel, 10-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop; optional hardware trigger; fully functional from 2.7 V to 5.5 V
  - **TPM** — One 6-channel and one 2-channel timer/pulse-width modulators (TPM) modules; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - **MTIM16** — One 16-bit modulo timer
  - **SCI** — One serial communications interface module with optional 13-bit break; LIN extensions
  - **SPI** — One serial peripheral interface module in 8-bit data length mode with a receiving data buffer hardware match function
  - **IIC** — Inter-integrated circuit bus module capable of operation up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt-driven byte-by-byte data transfer; broadcast mode; 10-bit addressing
  - **ACMP** — Analog comparator with option to compare to internal reference
  - **RTC** — Real time counter
  - **KBI**— 8-pin keyboard interrupt module with software selectable polarity on edge or edge/level modes
- Input/Output
  - 30 GPIOs including one output-only pin and one input-only pin
- Package Options
  - 32-pin SDIP
  - 32-pin LQFP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Table of Contents

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
1	4/2/2009	Initial public release.
2	7/20/2009	Updated Section 5.13, “EMC Performance.” Corrected Table 1. Corrected default trim value to 31.25 kHz.

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com

Reference Manual (MC9S08SV16RM)

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of MC9S08SV16 series MCU.

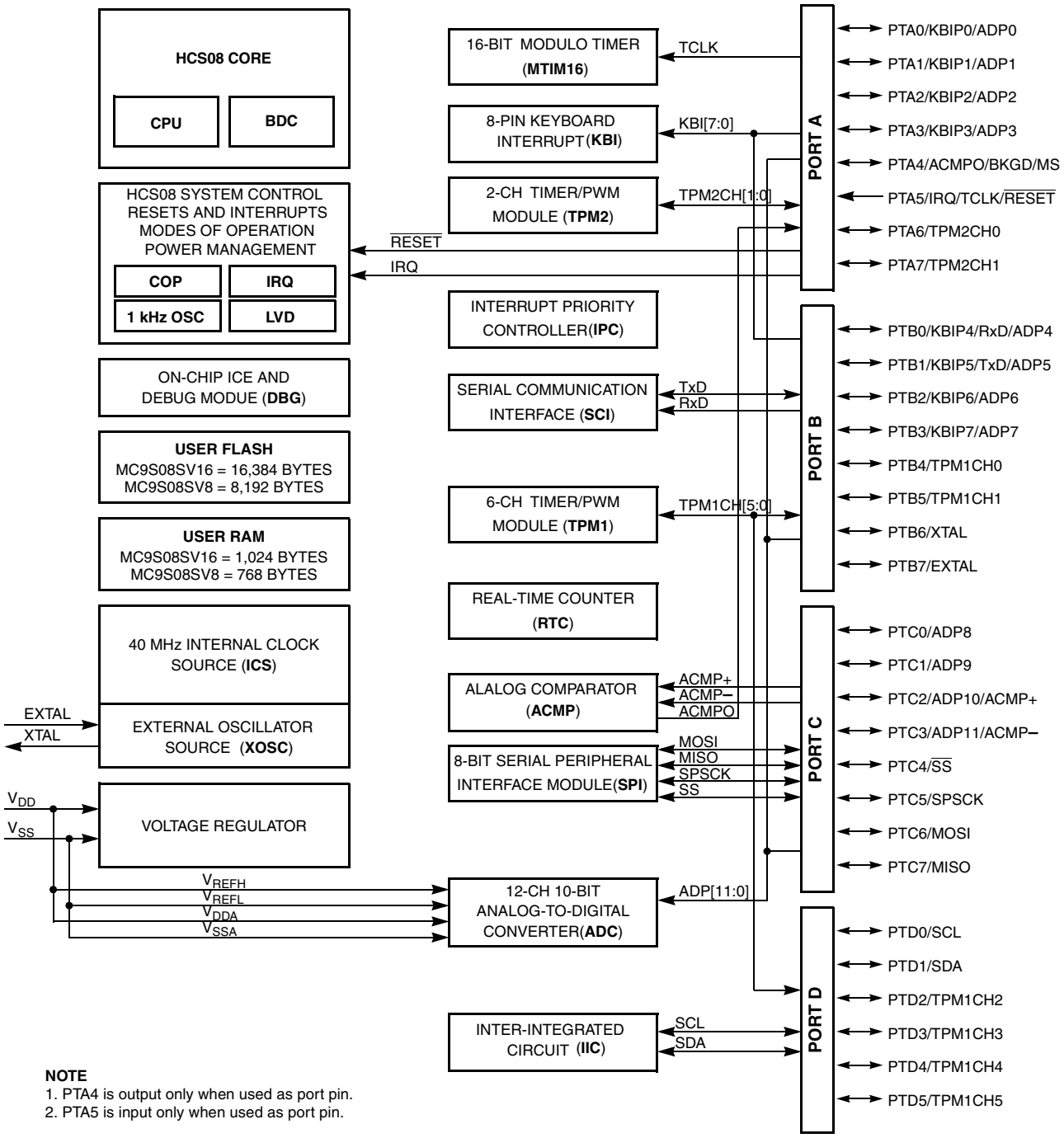


Figure 1. MC9S08SV16 Series Block Diagram

2 System Clock Distribution

MC9S08SV16 series use ICS module as clock sources. The ICS module can use internal or external clock source as reference to provide up to 40 MHz CPU clock. The output of ICS module includes,

- OSCOUT— XOSC output provides EXTAL reference clock to ADC and RTC.
- ICSIRCLK — ICS internal clock reference provides clock source of RTC.
- ICSFFCLK — ICS fixed frequency clock reference (around 32.768 kHz) provides double of the fixed lock signal to TPMs and MTIM16.
- ICSOUT — ICS CPU clock provides double of bus clock which is basic clock reference of peripherals.
- ICSLCLK — Alternate BDC clock provides debug signal to BDC module.

The TCLK pin is an extra external clock source. When TCLK is enabled, it can provide alternate clock source to TPMs and MTIM16. The on-chip 1 kHz clock can provide clock source of RTC and COP modules.

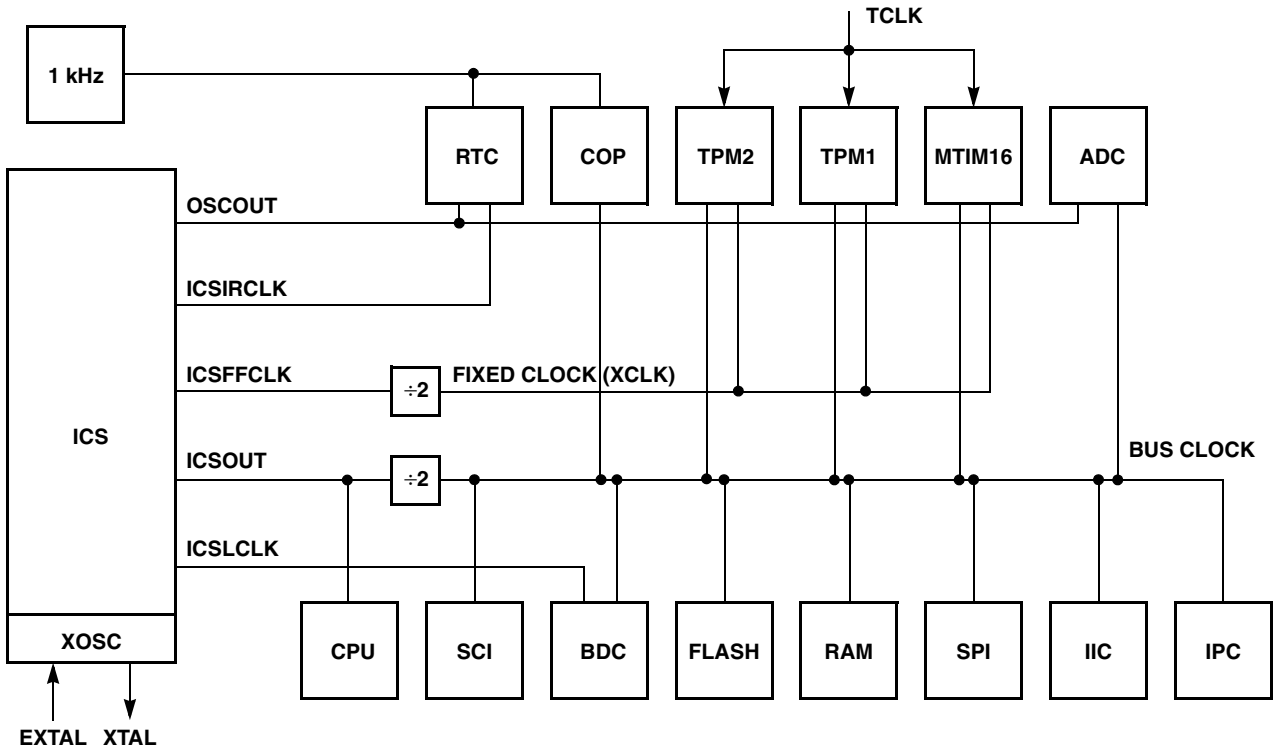


Figure 2. System Clock Distribution Diagram

3 Pin Assignments

This section shows the pin assignments for the MC9S08SV16 series devices.

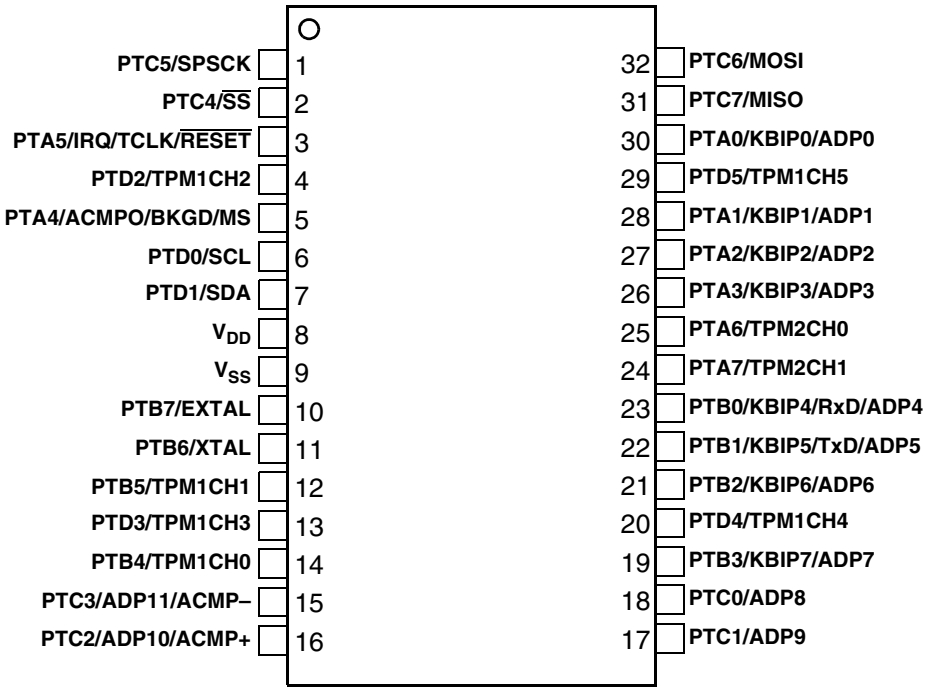


Figure 3. MC9S08SV16 Series 32-Pin SDIP Package

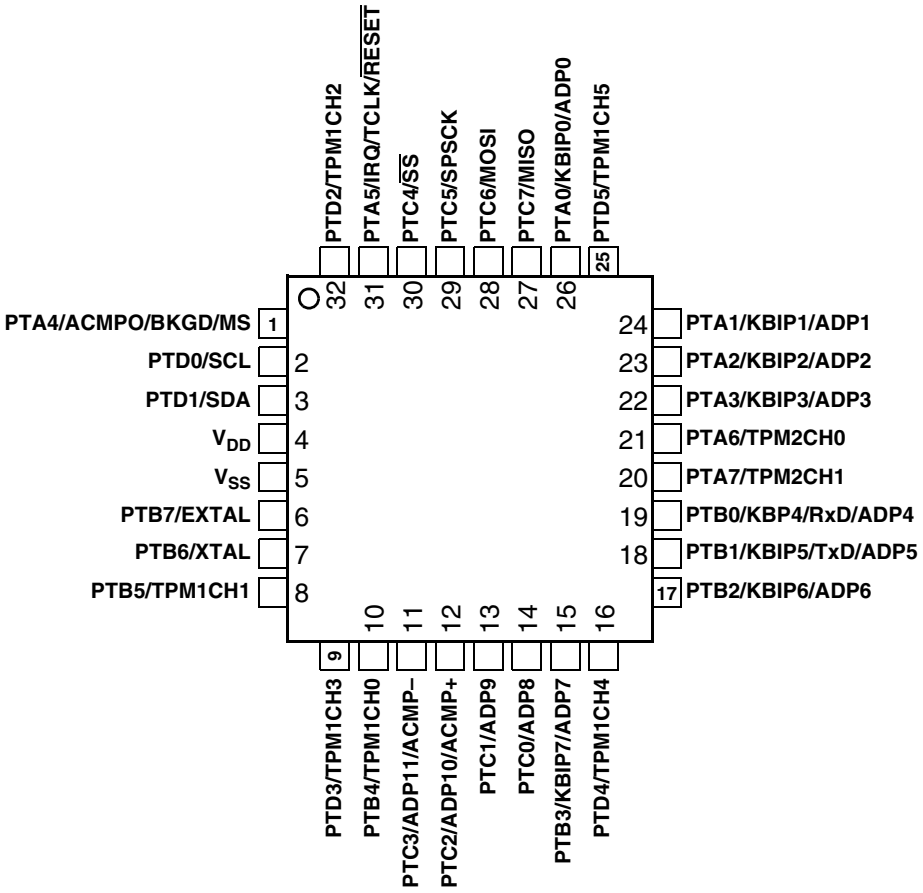


Figure 4. MC9S08SV16 Series 32-Pin LQFP Package

Table 1. Pin Availability by Package Pin-Count

Pin Number		<-- Lowest **Priority** --> Highest							
32-SDIP	**32-LQFP**	**Port Pin**	**I/O**	**Alt 1**	**I/O**	**Alt 2**	**I/O**	**Alt 3**	**I/O**
1	29	PTC5	I/O	SPSCK	I/O				
2	30	PTC4	I/O	$\overline{SS}$	I/O				
3	31	PTA5	I	IRQ	I	TCLK	I	$\overline{RESET}$	I
4	32	PTD2	I/O			TPM1CH2	I/O		
5	1	PTA4	O	ACMPO	O	BKGD	I	MS	I
6	2	PTD0	I/O	SCL	I/O				
7	3	PTD1	I/O	SDA	I/O				
8	4							V_{DD}	I
9	5							V_{SS}	I
10	6	PTB7	I/O	EXTAL	I				
11	7	PTB6	I/O	XTAL	O				
12	8	PTB5	I/O			TPM1CH1	I/O		
13	9	PTD3	I/O			TPM1CH3	I/O		
14	10	PTB4	I/O			TPM1CH0	I/O		

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number		<-- Lowest **Priority** --> Highest							
32-SDIP	**32-LQFP**	**Port Pin**	**I/O**	**Alt 1**	**I/O**	**Alt 2**	**I/O**	**Alt 3**	**I/O**
15	11	PTC3	I/O			ADP11	I	ACMP–	I
16	12	PTC2	I/O			ADP10	I	ACMP+	I
17	13	PTC1	I/O			ADP9	I		
18	14	PTC0	I/O			ADP8	I		
19	15	PTB3	I/O	KBIP7	I	ADP7	I		
20	16	PTD4	I/O			TPM1CH4	I/O		
21	17	PTB2	I/O	KBIP6	I	ADP6	I		
22	18	PTB1	I/O	KBIP5	I	TxD	I/O	ADP5	I
23	19	PTB0	I/O	KBIP4	I	RxD	I	ADP4	I
24	20	PTA7	I/O			TPM2CH1	I/O		
25	21	PTA6	I/O			TPM2CH0	I/O		
26	22	PTA3	I/O	KBIP3	I	ADP3	I		
27	23	PTA2	I/O	KBIP2	I	ADP2	I		
28	24	PTA1	I/O	KBIP1	I	ADP1	I		
29	25	PTD5	I/O			TPM1CH5	I/O		
30	26	PTA0	I/O	KBIP0	I	ADP0	I		
31	27	PTC7	I/O	MISO	I/O				
32	28	PTC6	I/O	MOSI	I/O				

NOTE

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear out any associated flags before interrupts are enabled. Table 1 illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

4 Memory Map

Figure 5 shows the memory map for the MC9S08SV16 series. On-chip memory in the MC9S08SV16 series of MCUs consist of RAM, flash program memory for nonvolatile data storage, plus I/O and control/status registers. The registers are divided into two groups:

- Direct-page registers (0x0000 through 0x003F)
- High-page registers (0x1800 through 0x187F)

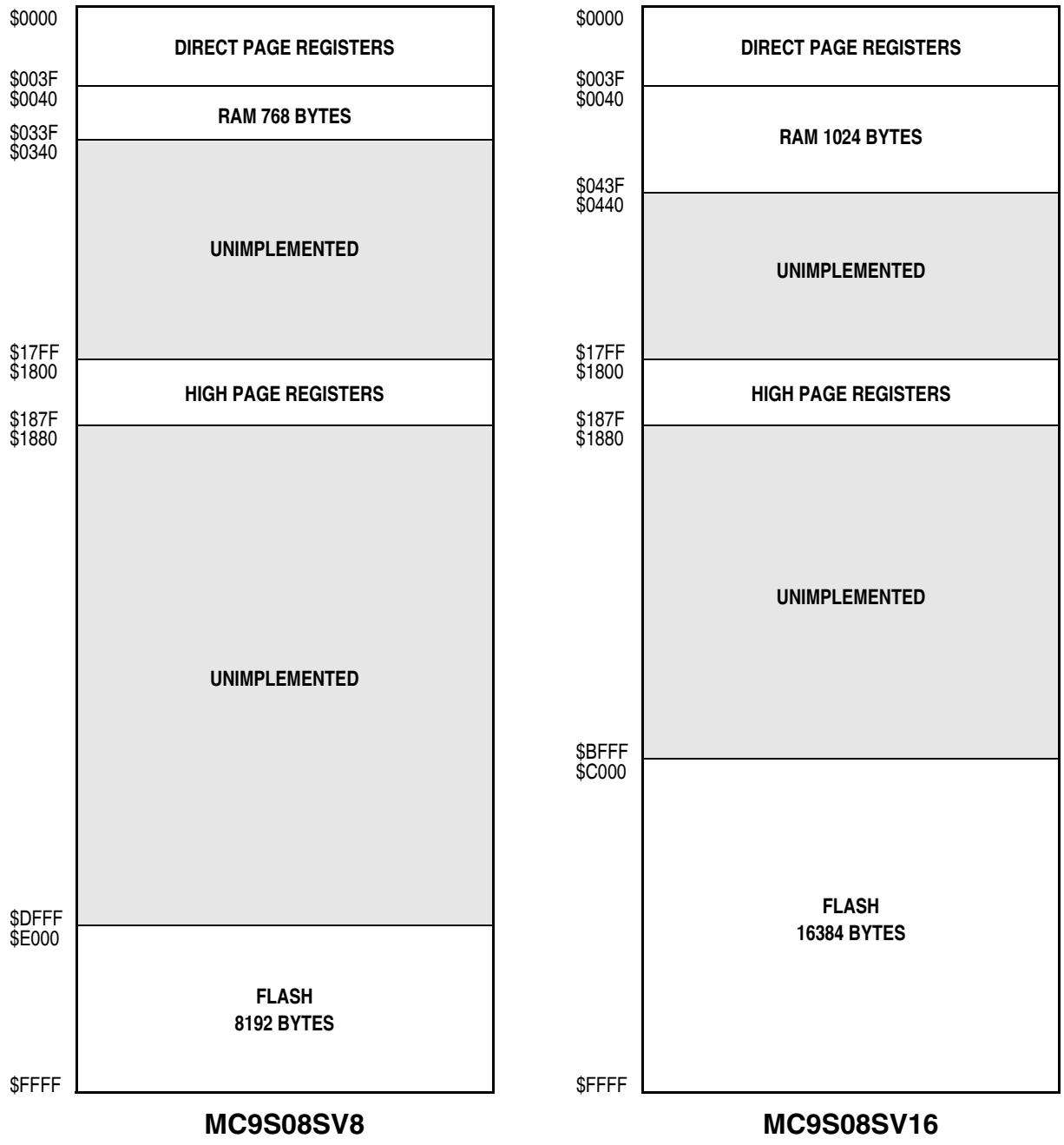


Figure 5. MC9S08SV16 Series Memory Map

5 Electrical Characteristics

5.1 Introduction

This section contains electrical and timing specifications for the MC9S08SV16 series of microcontrollers available at the time of publication.

5.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

5.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

5.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 4. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to 85	°C
Thermal resistance Single-layer board			
32-pin SDIP	θ_{JA}	60	°C/W
32-pin LQFP		85	
Thermal resistance Four-layer board			
32-pin LQFP	θ_{JA}	35	°C/W
32-pin LQFP		56	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

During the device qualification, ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 5. ESD and Latch-Up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	1	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

5.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min.	Typical[1]	Max.	Unit
1	—	Operating voltage		—	—	2.7	—	5.5	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	V_{DD} > 2.7 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		V_{DD} > 4.1 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 2.7 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	V_{DD} > 2.7 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		V_{DD} > 4.1 V, I_{Load} = 10 mA	—	—	0.5	
	C				V_{DD} > 2.7 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	—	100	mA
6	P	Input high voltage	All digital inputs	V_{IH}	V_{DD} > 4.1 V	0.70 × V_{DD}	—	—	V
	C				V_{DD} > 2.7 V	0.85 × V_{DD}	—	—	
7	P	Input low voltage	All digital inputs	V_{IL}	V_{DD} > 4.1 V	—	—	0.35 × V_{DD}	
	C				V_{DD} > 2.7 V	—	—	0.30 × V_{DD}	
8	C	Input hysteresis	All digital inputs	V_{hys}	—	0.06 × V_{DD}	—	—	mV
9	P	Input leakage current	All input only pins (per pin)	$\|I_{In}\|$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA
10	P	Hi-Z (off-state) leakage current	All input/output (per pin)	$\|I_{OZ}\|$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA

Table 7. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min.	Typical[1]	Max.	Unit
11a	P	Pullup, pulldown resistors — All digital inputs, when enabled (all I/O pins other than PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD}	—	17.5	—	52.5	kΩ
11b	C	Pullup, pulldown resistors — (PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD} (Note[2])	—	17.5	—	52.5	kΩ
12	C	DC injection current [3, 4, 5] — Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
		Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
13	C	Input capacitance, all pins	C_{In}	—	—	—	8	pF
14	C	RAM retention voltage	V_{RAM}	—	—	0.6	1.0	V
15	C	POR re-arm voltage[6]	V_{POR}	—	0.9	1.4	2.0	V
16	D	POR re-arm time	t_{POR}	—	10	—	—	µs
17	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	—	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	—	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
18	C	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	—	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	—	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
19	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	—	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
	C	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	—	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
21	C	Low-voltage inhibit reset/recover hysteresis	V_{hys}	—	—	80	—	mV
22	C	Bandgap voltage reference[7]	V_{BG}	—	—	1.21	—	V

1 Typical values are measured at 25 °C. Characterized, not tested.

2 The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear higher when measured externally on the pin.

3 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C

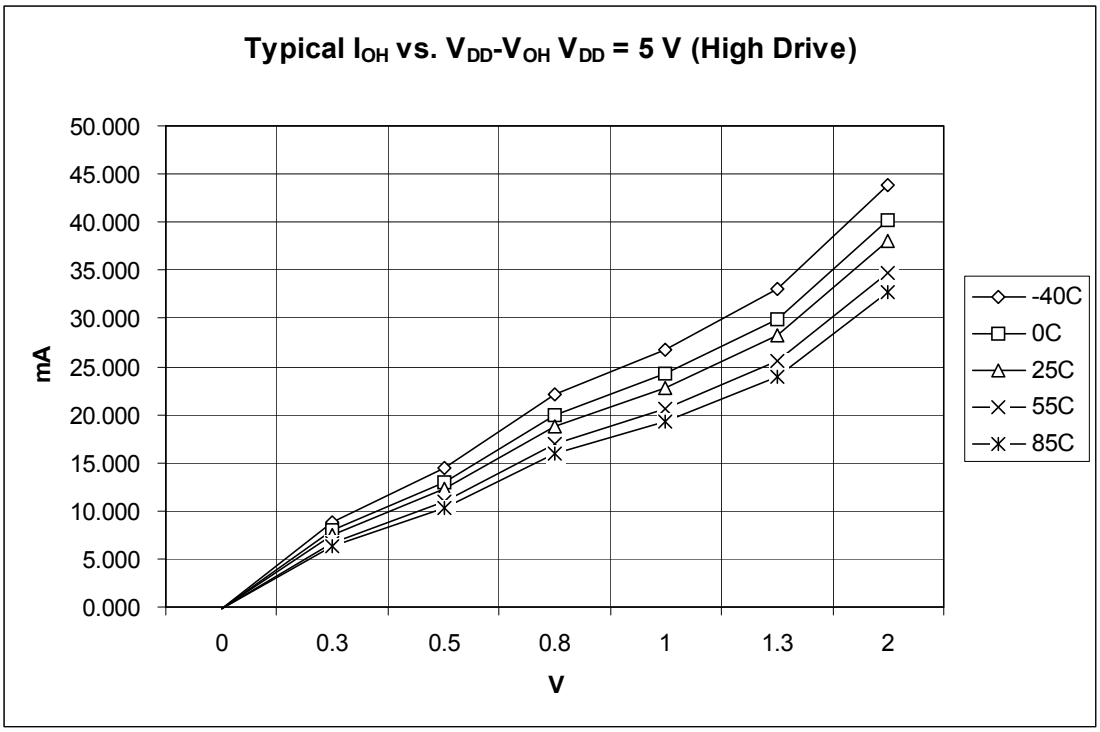


Figure 6. Typical I_{OH} Vs. V_{DD}–V_{OH} (V_{DD} = 5.0 V) (High Drive)

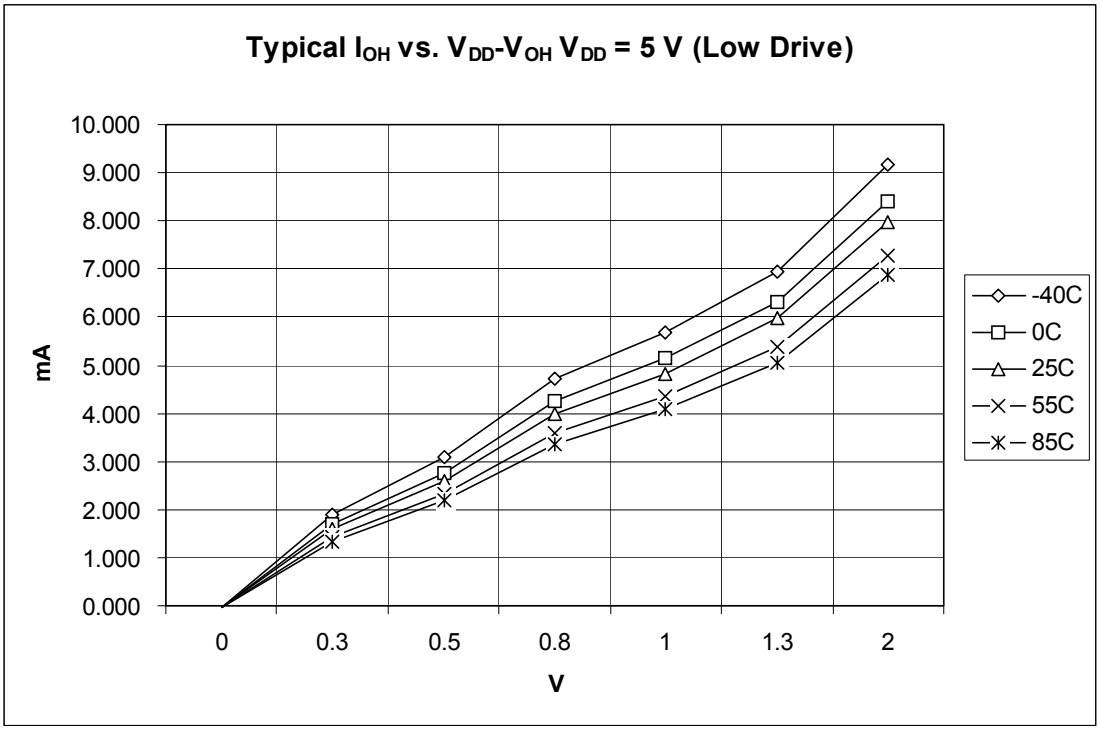


Figure 7. Typical I_{OH} Vs. V_{DD}–V_{OH} (V_{DD} = 5.0 V) (Low Drive)

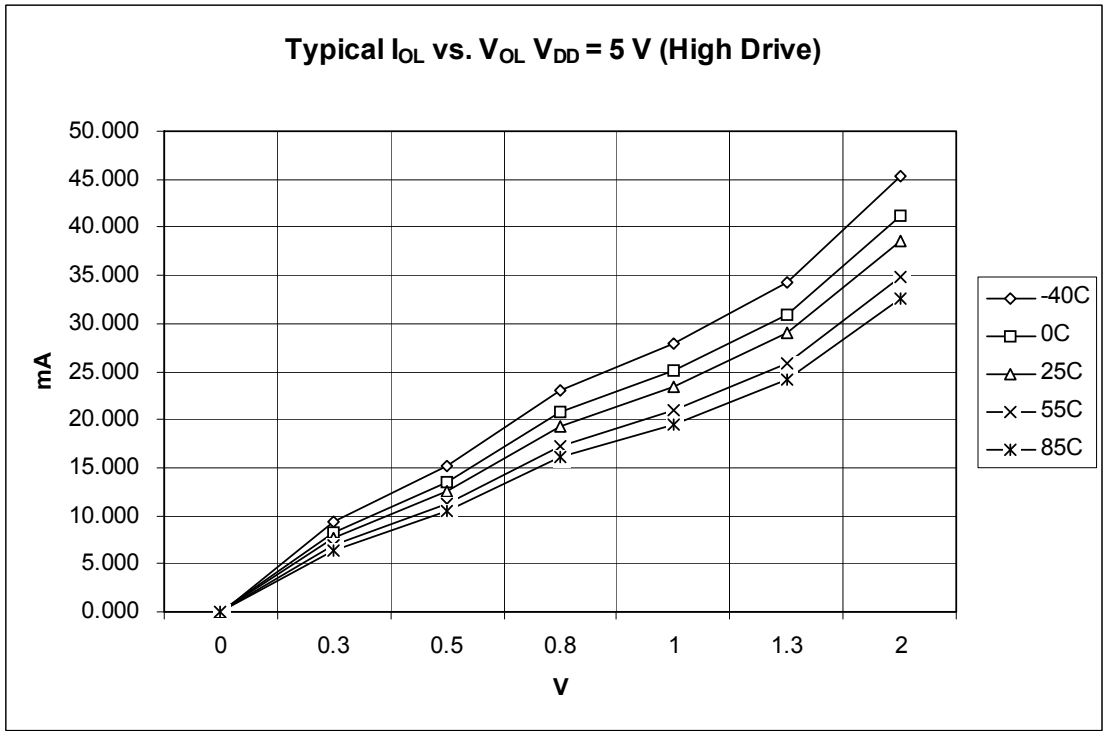


Figure 8. Typical I_{OH} Vs. V_{OL} (V_{DD} = 5.0 V) (High Drive)

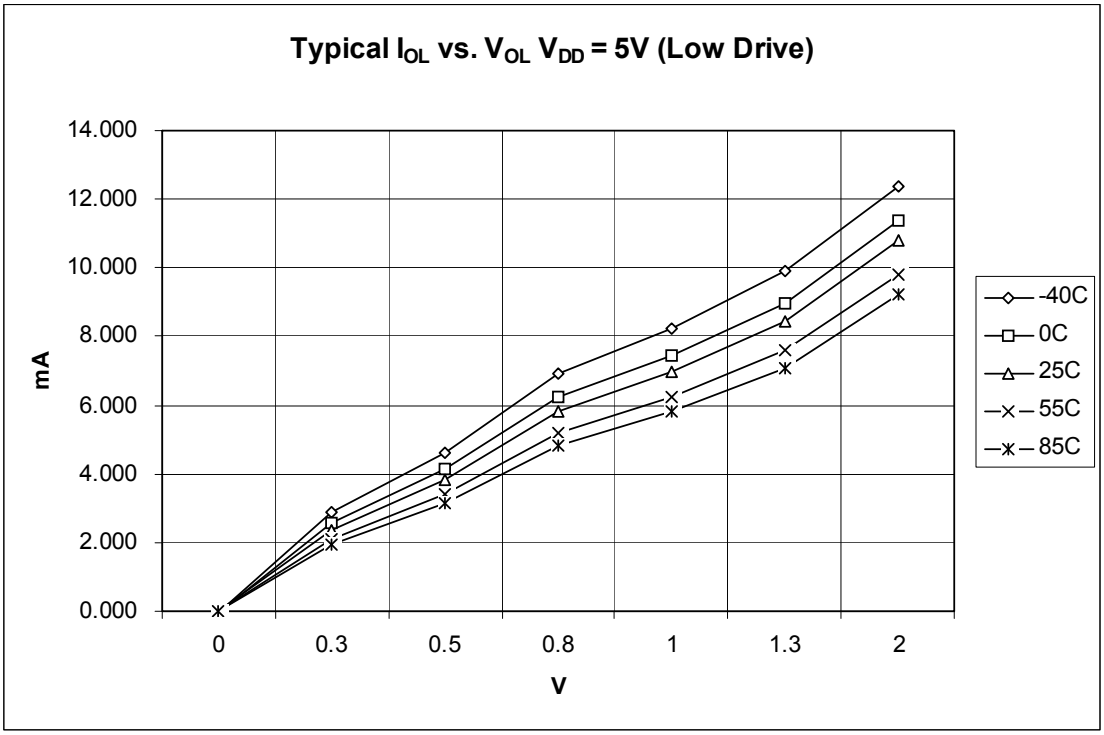


Figure 9. Typical I_{OH} Vs. V_{OL} (V_{DD} = 5.0 V) (Low Drive)

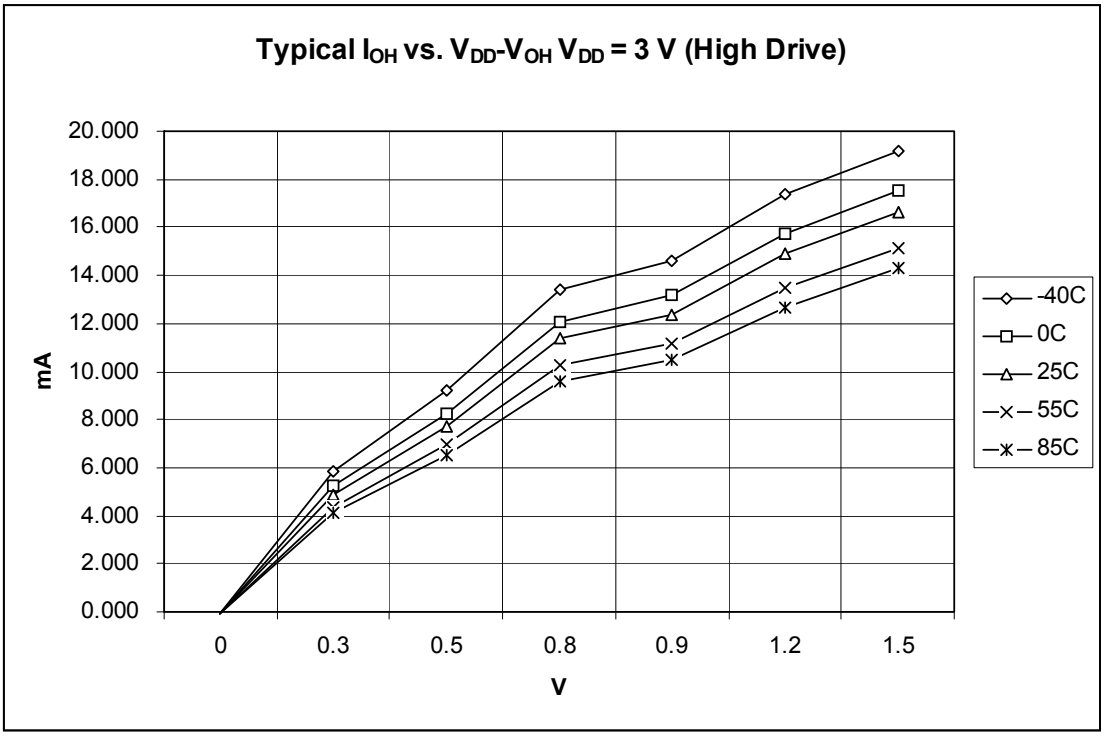


Figure 10. Typical I_{OH} Vs. V_{DD}–V_{OH} (V_{DD} = 3.0 V) (High Drive)

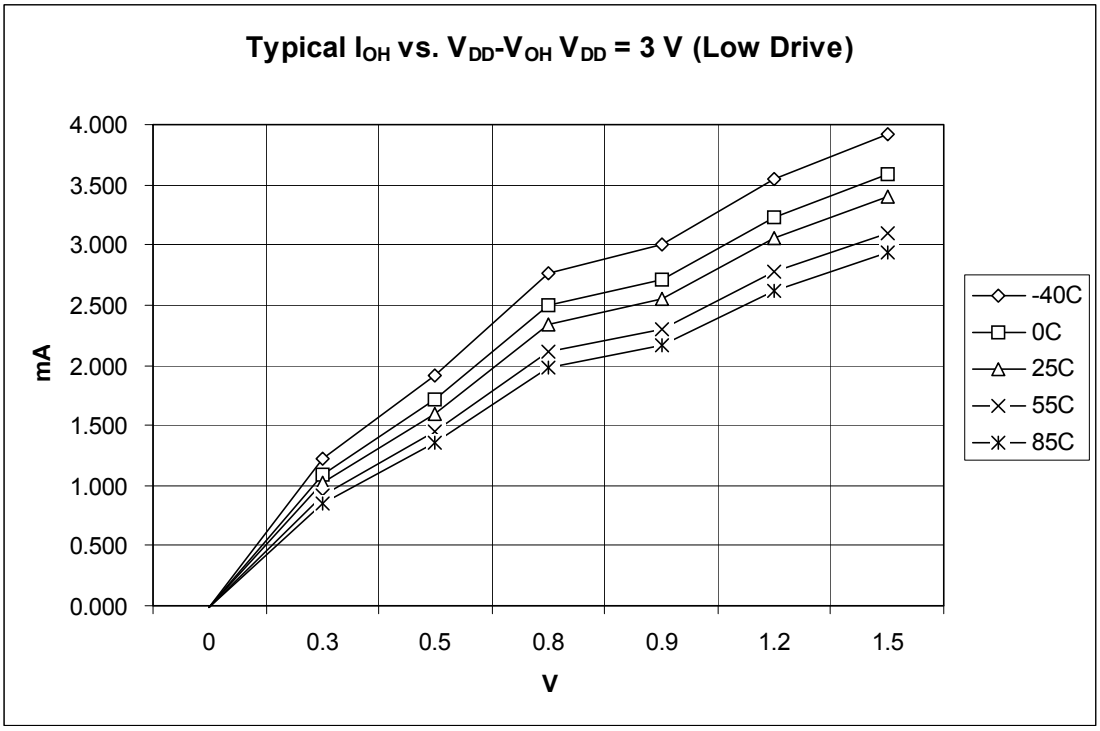


Figure 11. Typical I_{OH} Vs. V_{DD}–V_{OH} (V_{DD} = 3.0 V) (Low Drive)

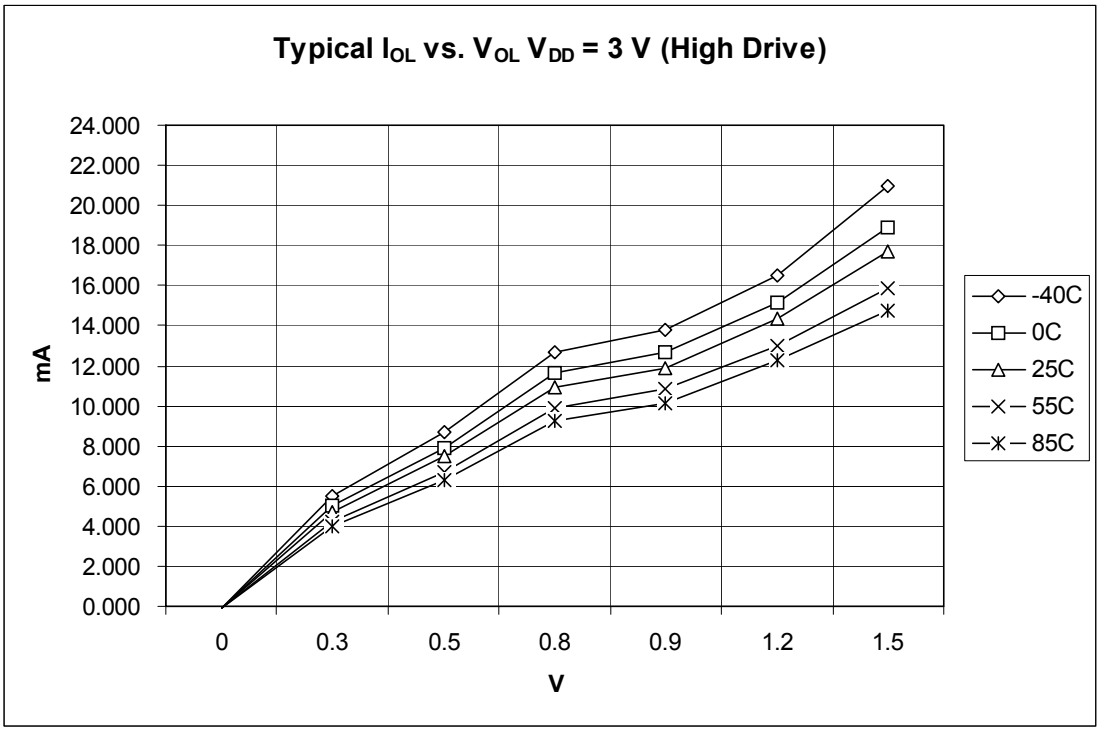


Figure 12. Typical I_{OL} Vs. V_{OL} (V_{DD} = 3.0 V) (High Drive)

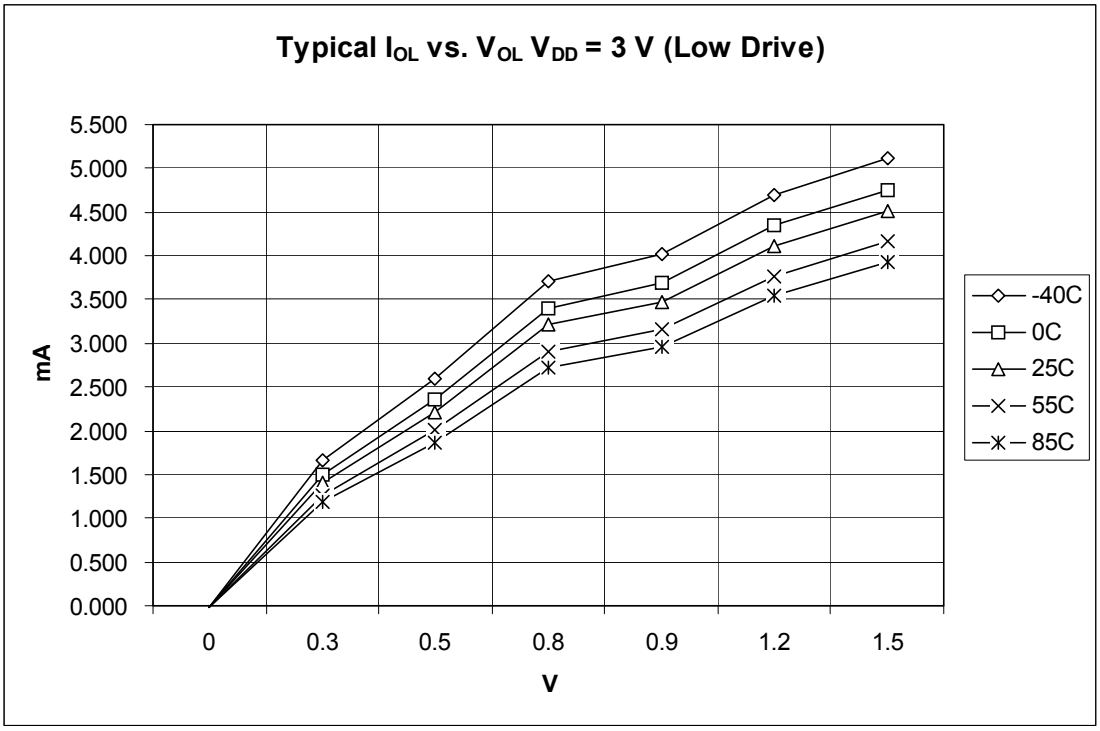


Figure 13. Typical I_{OL} Vs. V_{OL} (V_{DD} = 3.0 V) (Low Drive)

5.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
1	P	Run supply current FBE mode, all modules on	RI_{DD}	20 MHz	5	10.57	12.96	mA	–40 to 85 °C
	C			8 MHz		5.24	6.48		
	C			1 MHz		2.00	2.60		
2	P	Run supply current FBE mode, all modules on	RI_{DD}	20 MHz	3	8.86	10.86	mA	–40 to 85 °C
	C			8 MHz		4.53	5.61		
	C			1 MHz		1.82	2.31		
3	C	Run supply current FBE mode, all modules off	RI_{DD}	20 MHz	5	5.91	7.25	mA	–40 to 85 °C
	C			8 MHz		2.94	3.69		
	C			1 MHz		1.18	1.54		
4	C	Run supply current FBE mode, all modules off	RI_{DD}	20 MHz	3	5.69	6.98	mA	–40 to 85 °C
	C			8 MHz		2.90	3.60		
	C			1 MHz		1.17	1.49		
5	C	Wait mode current FBE mode, all modules off	WI_{DD}	20 MHz	5	4.83	—	mA	–40 to 85 °C
	C			1 MHz		1.06	—		

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
6	C	Wait mode current FBE mode, all modules off	WI_{DD}	20 MHz	3	4.80	—	mA	–40 to 85 °C
	C			1 MHz		1.05	—		
7	P	Stop2 mode supply current	$S2I_{DD}$	—	5	0.85 1.06 2.59	— — —	µA	–40 °C 25 °C 85 °C
	C			—	3	0.76 0.97 2.25	— — —		–40 °C 25 °C 85 °C
8	P	Stop3 mode supply current no clocks active	$S3I_{DD}$	—	5	0.85 1.17 3.56	—	µA	–40 °C 25 °C 85 °C
	C			—	3	0.76 1.07 3.22	—		–40 °C 25 °C 85 °C
9	C	ADC adder to stop3	—	—	5	128.72	—	µA	–40 to 85 °C
				—	3	123.86	—		
10	C	RTC adder to stop3 and stop2	—	—	5	300	—	nA	–40 to 85 °C
	C		—	—	3	300	—		
11	C	LVD adder to stop3 and stop2	—	—	5	106.7	—	µA	–40 to 85 °C
	C		—	—	3	95.6	—		

[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

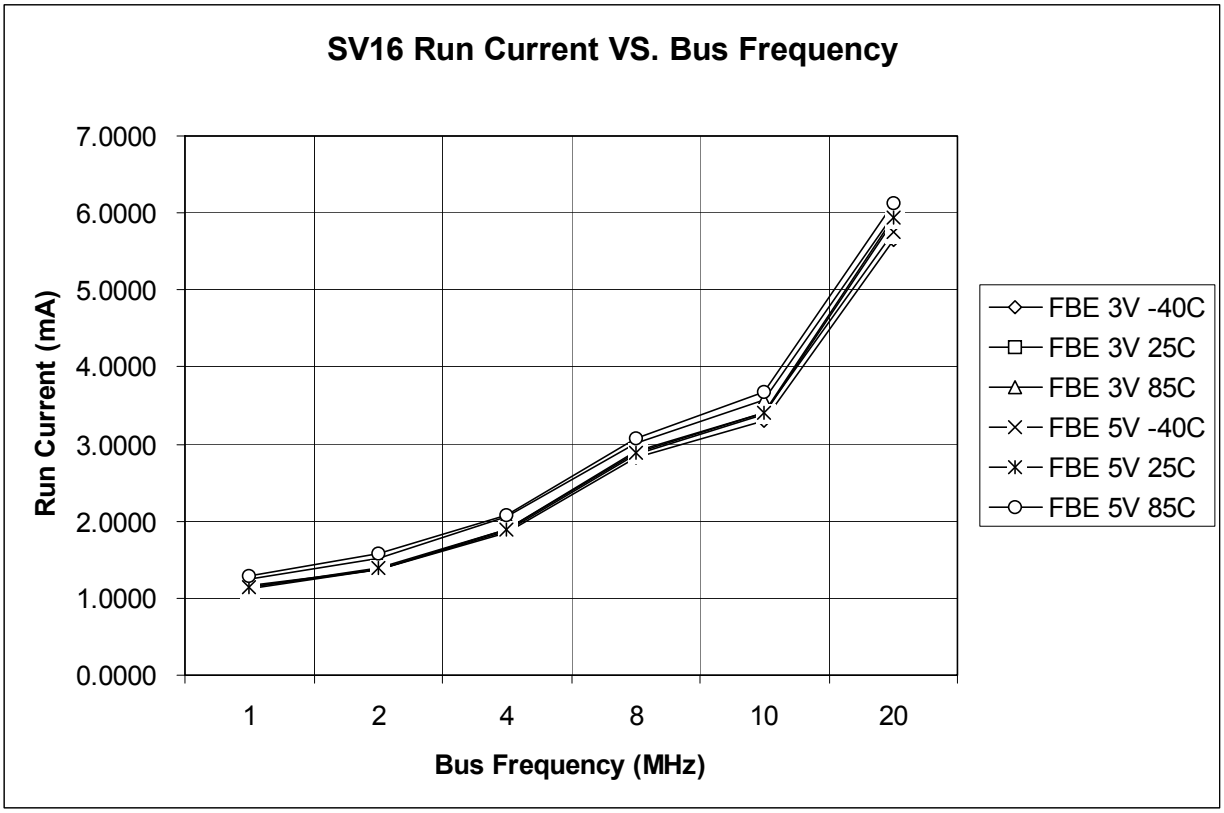


Figure 14. Typical Run I_{DD} for FBE (All Modules Off)

5.8 External Oscillator (XOSC) and ICS Characteristics

Refer to Figure 16 for crystal or resonator circuits.

Table 9. XOSC and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1), high gain (HGO = 1), FBELP mode High range (RANGE = 1), low power (HGO = 0), FBELP mode	 f_{lo} f_{hi} f_{hi} f_{hi}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1 C_2	See Note [3]			
3	D	Feedback resistor Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)	R_F	—	 10 1	—	 MΩ MΩ
4	D	Series resistor — Low range Low gain (HGO = 0) High gain (HGO = 1)	R_S	—	 0 100	—	kΩ
5	D	Series resistor — High range Low gain (HGO = 0) High gain (HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	—	 0 0 0	 0 10 20	kΩ
6	C	Crystal start-up time [4, 5] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH}	 — 	 200 400 5 15	 — 	ms
7	T	Internal reference start-up time	t_{IRST}	—	60	100	µs
8	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode[2] FBELP mode	f_{extal}	 0.03125 0	 —	 5 40	 MHz MHz
9	P	Average internal reference frequency — trimmed	f_{int_t}	—	31.25	—	kHz
10	P	DCO output frequency range — trimmed — Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
	P	Middle range (DRS = 10)		32	—	40	
11	C	Total deviation of DCO output from trimmed frequency[4] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	±2 ±1	$\%f_{dco}$
12	C	FLL acquisition time[4,6]	$t_{Acquire}$	—	—	1	ms
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 See crystal or resonator manufacturer's recommendation.

4 This parameter is characterized and not tested on each device.

5 Proper PC board layout procedures must be followed to achieve specifications.

6 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

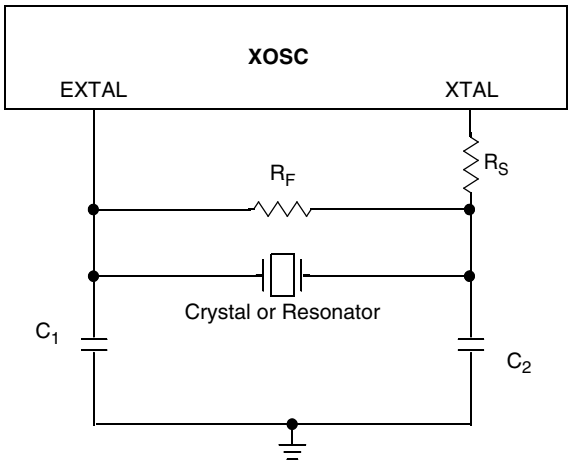


Figure 15. Typical Crystal or Resonator Circuit

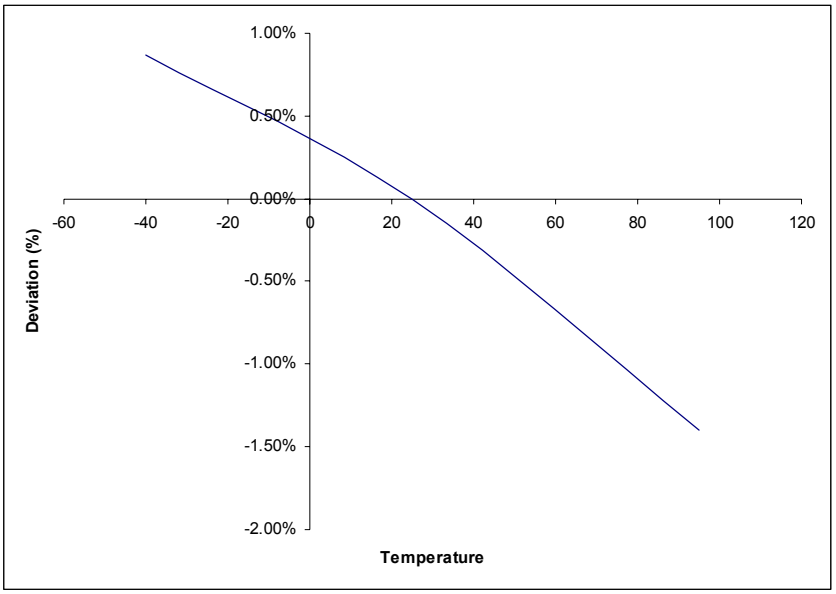


Figure 16. Deviation of DCO Output from Trimmed Frequency (20 MHz, 5.0 V)

5.9 AC Characteristics

This section describes timing characteristics for each peripheral system.

5.9.1 Control Timing

Table 10. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

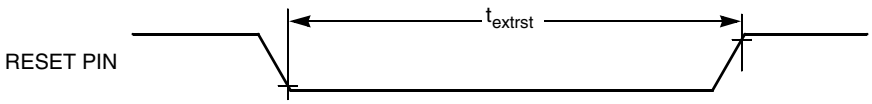


Figure 17. Reset Timing

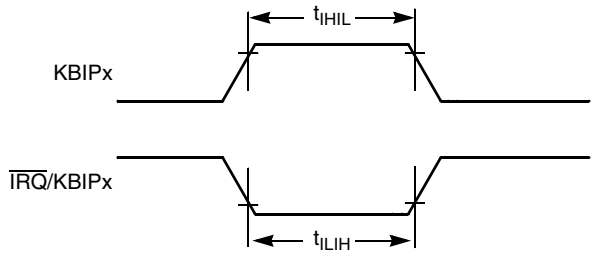


Figure 18. IRQ/KBIPx Timing

5.9.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 11. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

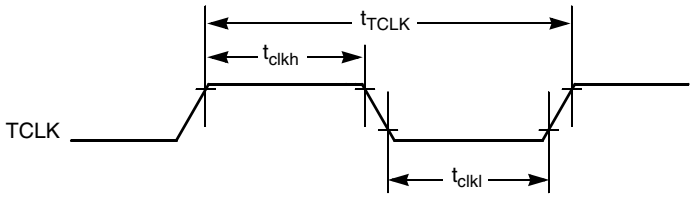


Figure 19. Timer External Clock

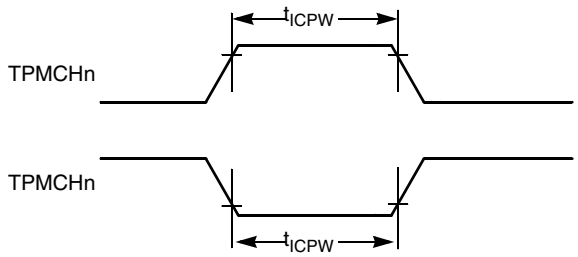


Figure 20. Timer Input Capture Pulse

5.9.3 SPI Timing

Table 12 and Figure 21 through Figure 24 describe the timing requirements for the SPI system.

Table 12. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns