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MC9S12DP512
Device Guide
V01.25

Covers also

MC9S12DT512, MC9S12DJ512,
MC9S12A512

Original Release Date: 27 Nov 2001
Revised: 05 Jul 2005

Freescale Semiconductor, Inc.

freescale™ semiconductor

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	27 Nov 2001	11 Feb 2002		- Initial version based on DP256 V2.09.
V01.01	13 Mar 2002	13 Mar 2002		- Updated document formats. - Removed reference to SIM in overview. - Changed XCLKS to PE7 in signal description. - Removed "Oscillator start-up time from POR or STOP" from Oscillator Characterisitcs. - Changed VDD and VDDPLL to 2.35V. - Updated C_{INS}. - Updated I_{OL}/I_{OH} values. - Updated input capacitance. - Updated NVM timing characteristics.
V01.02	02 Apr 2002	02 Apr 2002		- Updated document reference (SPI, SCI).
V01.03	15 Apr 2002	15 Apr 2002		- Corrected values in device memory map (RAM start, flash protected sector sizes). - Updated document reference (SCI).
V01.04	06 Jun 2002	06 Jun 2002		- Changed all operating frequency references to 50MHz EXTAL and removed references to 80 pin LQFP.
V01.05	05 Jul 2002	05 Jul 2002		- Preface Table "Document References": Changed to full naming for each block. - Table "Interrupt Vector Locations", Column "Local Enable": Corrected several register and bit names. - Table "Signal Properties": Added column "Internal Pull Resistor". - Table "PLL Characteristics": Updated parameters K1 and f1 - Figure "Basic Pll functional diagram": Inserted XFC pin in diagram - Enhanced section "XFC Component Selection" - Added to Sections ATD, ECT and PWM: freeze mode = active BDM mode.

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.06	24 Jul 2002	24 Jul 2002		- Updated SPI electrical characteristics. - Updated Derivative Differences table. - Added ordering number example. - Added Detailed Register Map. - Changed Internal Pull Resistor column of signal table. - Added pull device description for MODC pin. - Corrected XCLKS figure titles. Moved table to section Modes of Operation. - Removed ’1/2’ from BDM in Figure Clock Connections. - Completely reworked section Modes of Operation. Added Chip Configuration Summary and Low Power Mode description. - Changed classification to C for internal pull currents inTable 5V I/O Characteristics. - Changed input leakage to 1uA for all pins. - Updated VREG section and layout recommendation. - Moved Power and Gound Connection Summary table to start of Power Supply Pins section. - Added ROMONE to pinout
V01.07	29 Jul 2002	05 Aug 2002		- Corrected mem map: ’MEBI map x of 3’ - Corrected mem map: KEYEN bits in FSEC. - Added section Printed Circuit Board Layout Proposal. - Corrected addresses in Reserved, CAN and EEP buffer map. - Updated NVM electricals.
V01.08	21 Aug 2002	21 Aug 2002		- Updated table ’Document References’ - Added section ’Oscillator (OSC) Block Description’
V01.09	24 Sep 2002	24 Sep 2002		- Section HCS12 Core Block Desciption: mentioned alternalte clock of BDM to be equivalent to oscillator clock - Corrected tables 0-1 and 0-2
V01.10	18 Oct 2002	18 Oct 2002		- Added derivatives to cover sheet. - Added part ID for 1L00M maskset. - Corrected in footnote of Table "PLL Characteristics": f_{OSC} = 4MHz.
V01.11	29 Oct 2002	29 Oct 2002		- Renamed Preface section to Derivative Differences and Document references. - Added A512 derivative. - Updated module set of DJ512 in Table 0-1. - Added details for derivatives without CAN and/or BDLC modules.
V01.12	03 Dec 2002	03 Dec 2002		- Corrected several entries in ’Detailed Memory Map’. - Removed footnote on input leakage current from table ’5V I/O Characteristics’.
V01.13	08 Jan 2003	08 Jan 2003		- Updated section ’Unsecuring the Microcontroller’. - Updated footnote 1 in table ’Operating Conditions’.
V01.14	23 Jan 2003	23 Jan 2003		- Renamed ROMONE pin to ROMCTL.
V01.15	28 Feb 2003	28 Feb 2003		- Corrected PE[1,0] pull specification in Signal Properties Summary Table.

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.16	31 Mar 2003	31 Mar 2003		- Corrections in App. A 'NVM, Flash and EEPROM': - Number of words per flash row = 64 - Replaced 'burst programming' with 'row programming' - Sector erase size = 1024 bytes - Corrected feature description ECT - Corrected min. bus freq. in table 'Operating Conditions'
V01.17	30 May 2003	30 May 2003		- Replaced references to HCS12 Core Guide with the individual HCS12 Block guides throughout document - Table 'Absolute Maximum Ratings' corrected footnote on clamp of TEST pin
V01.18	23 Jul 2003	23 Jul 2003		- Mentioned 'S12 LRAE' bootloader in Flash section - Document References: corrected S12 CPU document reference
V01.19	24 Jul 2003	24 Jul 2003		- Added part ID for 2L00M maskset.
V01.20	01 Sep 2003	01 Sep 2003		- Added part ID for 3L00M maskset. - Added cycle definition to 'CPU 12 Block Description'. - Diagram 'Clock Connections': Connected Bus Clock to HCS12 Core. - Corrected 'Background Debug Module' to 'HCS12 Breakpoint' at address $0028 - $002F in table 1-1. - Corrected 'Blank Check Time Flash' value in table 'NVM Timing Characteristics' - Added EXTAL pin VIH, VIL and EXTAL pin hysteresis value to 'Oscillator Characteristics'. Updated oscillator description and table note.
V01.21	08 Mar 2004	08 Mar 2004		- Added part ID for 4L00M maskset. - Corrected pin name KWP5 in device pinout.
V01.22	23 Aug 2004	23 Aug 2004		- Updated $V_{IH,EXTAL}$ and $V_{IL,EXTAL}$ in table 'Oscillator Characteristics' - Removed item 'Oscillator' from table 'Operating Conditions' as already covered in table 'Oscillator Characteristics'
V01.23	09 Feb 2005	09 Feb 2005		- Corrected Flash Row Programming Time in NVM Timing Characteristics
V01.24	01 Apr 2005	01 Apr 2005		- Changed T_{Javg} and added footnote to data retention time in NVM Reliability Characteristics
V01.25	05 Jul 2005	05 Jul 2005		- Updated NVM Reliability Characteristics

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Appendix A Electrical Characteristics

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Derivative Differences and Document References

Derivative Differences

Table 0-1 shows the availability of peripheral modules on the various derivatives. For details about the compatibility within the MC9S12D-Family refer also to engineering bulletin EB386.

Table 0-1 Derivative Differences[1]

Modules	MC9S12DP512	MC9S12DT512	MC9S12DJ512	MC9S12A512
# of CANs	5	3	2	0
CAN0	✓	✓	✓	—
CAN1	✓	✓	—	—
CAN2	✓	—	—	—
CAN3	✓	—	—	—
CAN4	✓	✓	✓	—
J1850/BDLC	✓	—	✓	—
Package	112 LQFP	112 LQFP	112 LQFP	112 LQFP
Package Code	PV	PV	PV	PV
Mask set	L00M	L00M	L00M	L00M
Temp Options	M, V, C	M, V, C	M, V, C	C
Notes	An errata exists contact Sales Office	An errata exists contact Sales Office	An errata exists contact Sales Office	An errata exists contact Sales Office

NOTES:
1. ✓: Available for this device, —: Not available for this device

The following figure provides an ordering number example for the MC9S12D-Family devices.

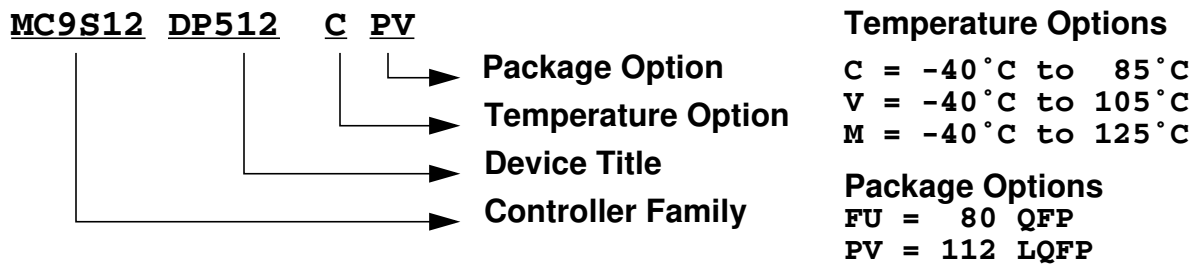


Figure 0-1 Order Part Number Example

The following items should be considered when using a derivative (**Table 0-1**):

- **Registers**
  - Do not write or read CAN0 registers (after reset: address range $0140 - $017F), if using a derivative without CAN0.
  - Do not write or read CAN1registers (after reset: address range $0180 - $01BF), if using a derivative without CAN1.
  - Do not write or read CAN2 registers (after reset: address range $01C0 - $01FF), if using a derivative without CAN2.
  - Do not write or read CAN3 registers (after reset: address range $0200 - $023F), if using a derivative without CAN3.
  - Do not write or read CAN4 registers (after reset: address range $0280 - $02BF), if using a derivative without CAN4.
  - Do not write or read BDLC registers (after reset: address range $00E8 - $00EF), if using a derivative without BDLC.
- **Interrupts**
  - Fill the four CAN0 interrupt vectors ($FFB0 - $FFB7) according to your coding policies for unused interrupts, if using a derivative without CAN0.
  - Fill the four CAN1 interrupt vectors ($FFA8 - $FFAF) according to your coding policies for unused interrupts, if using a derivative without CAN1.
  - Fill the four CAN2 interrupt vectors ($FFA0 - $FFA7) according to your coding policies for unused interrupts, if using a derivative without CAN2.
  - Fill the four CAN3 interrupt vectors ($FF98 - $FF9F) according to your coding policies for unused interrupts, if using a derivative without CAN3.
  - Fill the four CAN4 interrupt vectors ($FF90 - $FF97) according to your coding policies for unused interrupts, if using a derivative without CAN4.
  - Fill the BDLC interrupt vector ($FFC2, $FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC.
- **Ports**
  - The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0.
  - The CAN1 pin functionality (TXCAN1, RXCAN1) is not available on port PM3 and PM2, if using a derivative without CAN1.
  - The CAN2 pin functionality (TXCAN2, RXCAN2) is not available on port PM5 and PM4, if using a derivative without CAN2.
  - The CAN3 pin functionality (TXCAN3, RXCAN3) is not available on port PM7 and PM6, if using a derivative without CAN3.

- The CAN4 pin functionality (TXCAN4, RXCAN4) is not available on port PJ7, PJ6, PM7, PM6, PM5 and PM4, if using a derivative without CAN0.
- The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC.
- Do not write MODRR1 and MODRR0 bits of Module Routing Register (PIM_9DP256 Block Guide), if using a derivative without CAN0.
- Do not write MODRR3 and MODRR2 bits of Module Routing Register (PIM_9DP256 Block Guide), if using a derivative without CAN4.

Document References

The Device Guide provides information about the MC9S12DP512 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes the individual Block Guides of the implemented modules. In an effort to reduce redundancy, all module specific information is located only in the respective Block Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-2** for names and versions of the referenced documents throughout the Device Guide.

Table 0-2 Document References

Block Guide	Version	Document Order Number
HCS12 CPU Reference Manual	V02	S12CPUV2/D
HCS12 Module Mapping Control (MMC) Block Guide	V04	S12MMCV4/D
HCS12 Multiplexed External Bus Interface (MEBI) Block Guide	V03	S12MEBIV3/D
HCS12 Interrupt (INT) Block Guide	V01	S12INTV1/D
HCS12 Background Debug (BDM) Block Guide	V04	S12BDMV4/D
HCS12 Breakpoint (BKP) Block Guide	V01	S12BKPV1/D
Clock and Reset Generator (CRG) Block Guide	V04	S12CRGV4/D
Enhanced Capture Timer 16 Bit 8 Channel (ECT_16B8C) Block Guide	V01	S12ECT16B8V1/D
Analog to Digital Converter 10 Bit 8 Channel (ATD_10B8C) Block Guide	V02	S12ATD10B8CV2/D
Inter IC Bus (IIC) Block Guide	V02	S12IICV2/D
Asynchronous Serial Interface (SCI) Block Guide	V02	S12SCIV2/D
Serial Peripheral Interface (SPI) Block Guide	V03	S12SPIV3/D
Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block Guide	V01	S12PWM8B8CV1/D
512K Byte Flash (FTS512K4) Block Guide	V01	S12FTS512K4V1/D
4K Byte EEPROM (EETS4K) Block Guide	V02	S12EETS4KV2/D
Byte Level Data Link Controller -J1850 (BDLC) Block Guide	V01	S12BDLCV1/D
Freescale Scalable CAN (MSCAN) Block Guide	V02	S12MSCANV2/D
Voltage Regulator (VREG) Block Guide	V01	S12VREGV1/D
Port Integration Module (PIM_9DP256) Block Guide[1]	V03	S12DP256PIMV3/D
Oscillator (OSC) Block Guide	V02	S12OSCV2/D

NOTES:
1. Reused due to functional equivalence.

Section 1 Introduction

1.1 Overview

The MC9S12DP512 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 512K bytes of Flash EEPROM, 14K bytes of RAM, 4K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), three serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wake up capability, five CAN 2.0 A, B software compatible modules (MSCAN12), and an Inter-IC Bus. The MC9S12DP512 has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer's model identical to M68HC11
    iii. Instruction queue
    iv. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)
  - BDM (Background Debug Mode)
- CRG (Clock and Reset Generation)
  - Low current Colpitts oscillator or
  - Pierce oscillator
  - PLL
  - COP watchdog
  - Real Time Interrupt
  - Clock Monitor
- 8-bit and 4-bit ports with interrupt functionality

  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 512K Flash EEPROM
  - 4K byte EEPROM
  - 14K byte RAM
- Two 8-channel Analog-to-Digital Converters
  - 10-bit resolution
  - External conversion trigger capability
- Five 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Enhanced Capture Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Four 8-bit or two 16-bit pulse accumulators
- 8 PWM channels
  - Programmable period and duty cycle
  - 8-bit 8-channel or 16-bit 4-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
  - Usable as interrupt inputs
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Three Synchronous Serial Peripheral Interface (SPI)
- Byte Data Link Controller (BDLC)
  - SAE J1850 Class B Data Communications Network Interface Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications

- Inter-IC Bus (IIC)
  - Compatible with I^2C Bus standard
  - Multi-master operation
  - Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP package
  - I/O lines with 5V input and drive capability
  - 5V A/D converter inputs
  - Operation at 50MHz equivalent to 25MHz Bus Speed over -40˚C <= T_A <= 125˚C
  - Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Freescale use only**)
  - Special Peripheral Mode (**Freescale use only**)

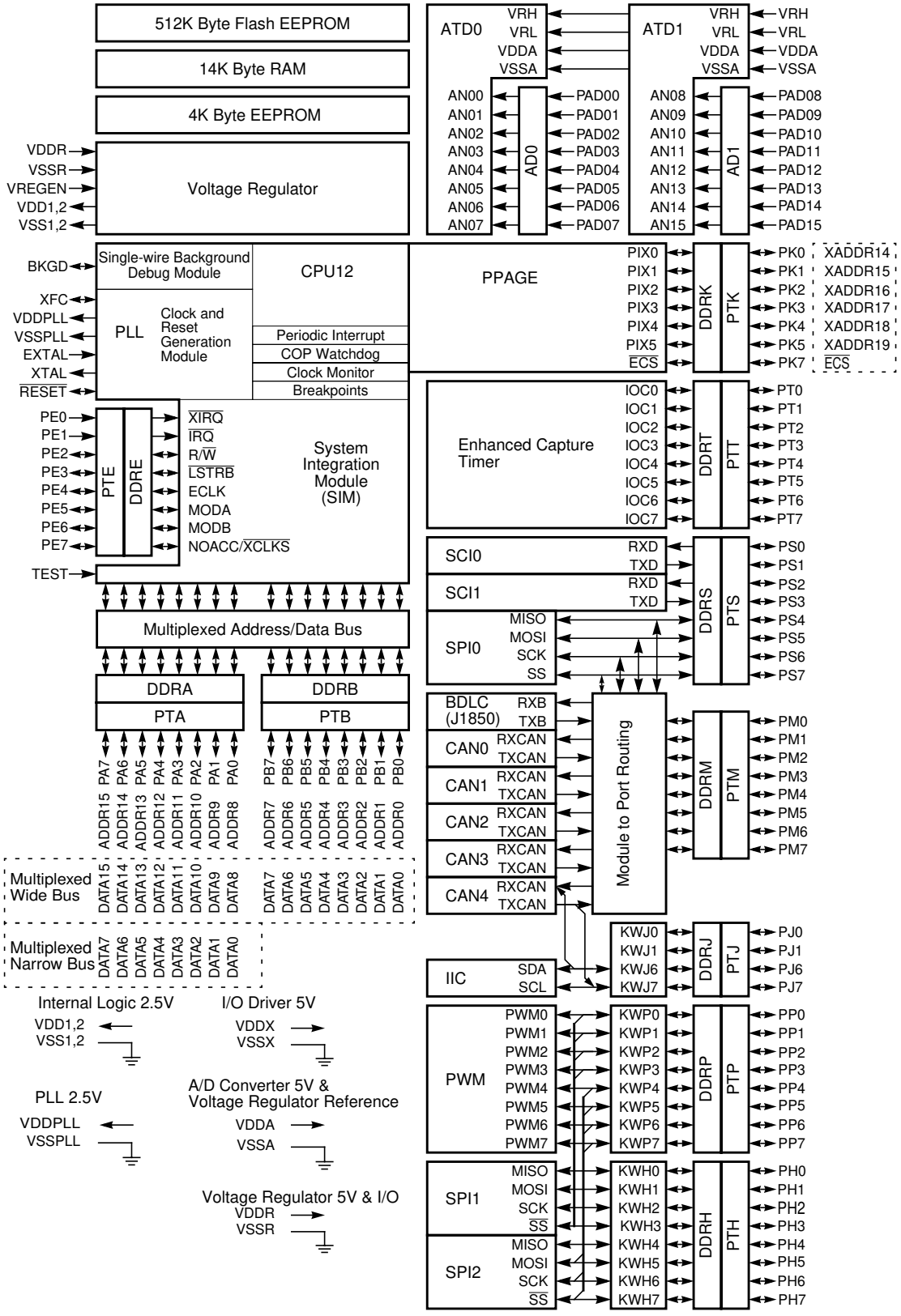
Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12DP512 device.

Figure 1-1 MC9S12DP512 Block Diagram



1.5 Device Memory Map

Table 1-1 and **Figure 1-2** show the device memory map of the MC9S12DP512 after reset. Note that after reset the bottom 1k of the EEPROM ($0000 - $03FF) are hidden by the register space

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$0000 - $000F	HCS12 Multiplexed External Bus Interface	16
$0010 - $0014	HCS12 Module Mapping Control	5
$0015 - $0016	HCS12 Interrupt	2
$0017 - $0019	Reserved	3
$001A - $001B	Device ID register (PARTID)	2
$001C - $001D	HCS12 Module Mapping Control	2
$001E	HCS12 Multiplexed External Bus Interface	1
$001F	HCS12 Interrupt	1
$0020 - $0027	Reserved	8
$0028 - $002F	HCS12 Breakpoint	8
$0030 - $0031	HCS12 Module Mapping Control	2
$0032 - $0033	HCS12 Multiplexed External Bus Interface	2
$0034 - $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 - $007F	Enhanced Capture Timer 16-bit 8 channels	64
$0080 - $009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	32
$00A0 - $00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
$00C8 - $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 - $00D7	Serial Communications Interface 0 (SCI1)	8
$00D8 - $00DF	Serial Peripheral Interface (SPI0)	8
$00E0 - $00E7	Inter IC Bus	8
$00E8 - $00EF	Byte Data Link Controller (BDLC)	8
$00F0 - $00F7	Serial Peripheral Interface (SPI1)	8
$00F8 - $00FF	Serial Peripheral Interface (SPI2)	8
$0100- $010F	Flash Control Register	16
$0110 - $011B	EEPROM Control Register	12
$011C - $011F	Reserved	4
$0120 - $013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	32
$0140 - $017F	Freescale Scalable Can (CAN	64
$0180 - $01BF	Freescale Scalable Ca	64
$01C0 - $01FF	Freescale Scalable Can (CAN	64
$0200 - $023F	Freescale Scalable Can (CAN3)	64
$0240 - $027F	Port Integration Module (PIM)	64
$0280 - $02BF	Freescale Scalable Can (CAN4)	64
$02C0 - $03FF	Reserved	320
$0000 - $0FFF	EEPROM array	4096
$0800 - $3FFF	RAM array	14336
$4000 - $7FFF	Fixed Flash EEPROM array incl. 1K, 2K, 4K or 8K Protected Sector at start	16384

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$8000 - $BFFF	Flash EEPROM Page Window	16384
$C000 - $FFFF	Fixed Flash EEPROM array incl. 2K, 4K, 8K or 16K Protected Sector at end and 256 bytes of Vector Space at $FF80 - $FFFF	16384