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MC9S12C Family
MC9S12GC Family
Reference Manual

HCS12
Microcontrollers

MC9S12C128
Rev 01.24

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A full list of family members and options is included in the appendices.

The following revision history table summarizes changes contained in this document.

This document contains information for all constituent modules, with the exception of the S12 CPU. For S12 CPU information please refer to the CPU S12 Reference Manual.

Revision History

Date	Revision Level	Description
June, 2005	01.14	New Book
July, 2005	01.15	Removed 16MHz option for 128K, 96K and 64K versions Minor corrections following review
Oct, 2005	01.16	Added outstanding flash module descriptions Added EPP package options Corrected and Enhanced recommended PCB layouts
Dec, 2005	01.17	Added note to PIM block diagram figure
Dec, 2005	01.18	Added PIM rerouting information to 80-pin package diagram
Jan, 2006	01.19	Modified LVI levels in electrical parameter section Corrected TSCR2 typo in timer register listing
Mar, 2006	01.20	Cleaned up Device Overview Section
May, 2006	01.21	Added 0M66G to PartID table Added units to MSCAN timing parameter table Corrected missing overbars on pin names
Dec, 2006	01.22	Corrected CRGFLG contents in register summary Removed non existing part number options Removed unintended symbol fonts from table A6
May, 2007	01.23	Updated ATD section Corrected typos
May, 2010	01.24	Updated TIM section

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Chapter 1
MC9S12C and MC9S12GC Device Overview (MC9S12C128)

1.1 Introduction

The MC9S12C-Family / MC9S12GC-Family are 48/52/80 pin Flash-based MCU families, which deliver the power and flexibility of the 16-bit core to a whole new range of cost and space sensitive, general purpose industrial and automotive network applications. All MC9S12C-Family / MC9S12GC-Family members feature standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 128K bytes of Flash EEPROM, up to 4K bytes of RAM, an asynchronous serial communications interface (SCI), a serial peripheral interface (SPI), an 8-channel 16-bit timer module (TIM), a 6-channel 8-bit pulse width modulator (PWM), an 8-channel, 10-bit analog-to-digital converter (ADC).

The MC9S12C128-Family members also feature a CAN 2.0 A, B software compatible module (MSCAN12).

All MC9S12C-Family / MC9S12GC-Family devices feature full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 10 dedicated I/O port bits are available with wake-up capability from stop or wait mode. The devices are available in 48-, 52-, and 80-pin QFP packages, with the 80-pin version pin compatible to the HCS12 A, B, and D Family derivatives.

1.1.1 Features

- 16-bit HCS12 core:
  - HCS12 CPU
    - Upward compatible with M68HC11 instruction set
    - Interrupt stacking and programmer's model identical to M68HC11
    - Instruction queue
    - Enhanced indexed addressing
  - MMC (memory map and interface)
  - INT (interrupt control)
  - BDM (background debug mode)
  - DBG12 (enhanced debug12 module, including breakpoints and change-of-flow trace buffer)
  - MEBI (multiplexed expansion bus interface) available only in 80-pin package version
- Wake-up interrupt inputs:
  - Up to 12 port bits available for wake up interrupt function with digital filtering

- Memory options:
  - 16K or 32Kbyte Flash EEPROM (erasable in 512-byte sectors)
    64K, 96K, or 128Kbyte Flash EEPROM (erasable in 1024-byte sectors)
  - 1K, 2K or 4K Byte RAM
- Analog-to-digital converters:
  - One 8-channel module with 10-bit resolution
  - External conversion trigger capability
- Available on MC9S12C Family:
  - One 1M bit per second, CAN 2.0 A, B software compatible module
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit, or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error, and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Timer module (TIM):
  - 8-channel timer
  - Each channel configurable as either input capture or output compare
  - Simple PWM mode
  - Modulo reset of timer counter
  - 16-bit pulse accumulator
  - External event counting
  - Gated time accumulation
- PWM module:
  - Programmable period and duty cycle
  - 8-bit 6-channel or 16-bit 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Serial interfaces:
  - One asynchronous serial communications interface (SCI)
  - One synchronous serial peripheral interface (SPI)
- CRG (clock reset generator module)
  - Windowed COP watchdog
  - Real time interrupt
  - Clock monitor
  - Pierce or low current Colpitts oscillator
  - Phase-locked loop clock frequency multiplier
  - Limp home mode in absence of external clock
  - Low power 0.5MHz to 16MHz crystal oscillator reference clock

- Operating frequency:
  - 32MHz equivalent to 16MHz bus speed for single chip
  - 32MHz equivalent to 16MHz bus speed in expanded bus modes
  - Option of 9S12C Family: 50MHz equivalent to 25MHz bus speed
  - All 9S12GC Family members allow a 50MHz operating frequency.
- Internal 2.5V regulator:
  - Supports an input voltage range from 2.97V to 5.5V
  - Low power mode capability
  - Includes low voltage reset (LVR) circuitry
  - Includes low voltage interrupt (LVI) circuitry
- 48-pin LQFP, 52-pin LQFP, or 80-pin QFP package:
  - Up to 58 I/O lines with 5V input and drive capability (80-pin package)
  - Up to 2 dedicated 5V input only lines (IRQ, XIRQ)
  - 5V 8 A/D converter inputs and 5V I/O
- Development support:
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints
  - Enhanced DBG12 debug features

1.1.2 Modes of Operation

User modes (expanded modes are only available in the 80-pin package version).

- Normal and emulation operating modes:
  - Normal single-chip mode
  - Normal expanded wide mode
  - Normal expanded narrow mode
  - Emulation expanded wide mode
  - Emulation expanded narrow mode
- Special operating modes:
  - Special single-chip mode with active background debug mode
  - Special test mode **(Freescale use only)**
  - Special peripheral mode **(Freescale use only)**
- Low power modes:
  - Stop mode
  - Pseudo stop mode
  - Wait mode

1.1.3 Block Diagram

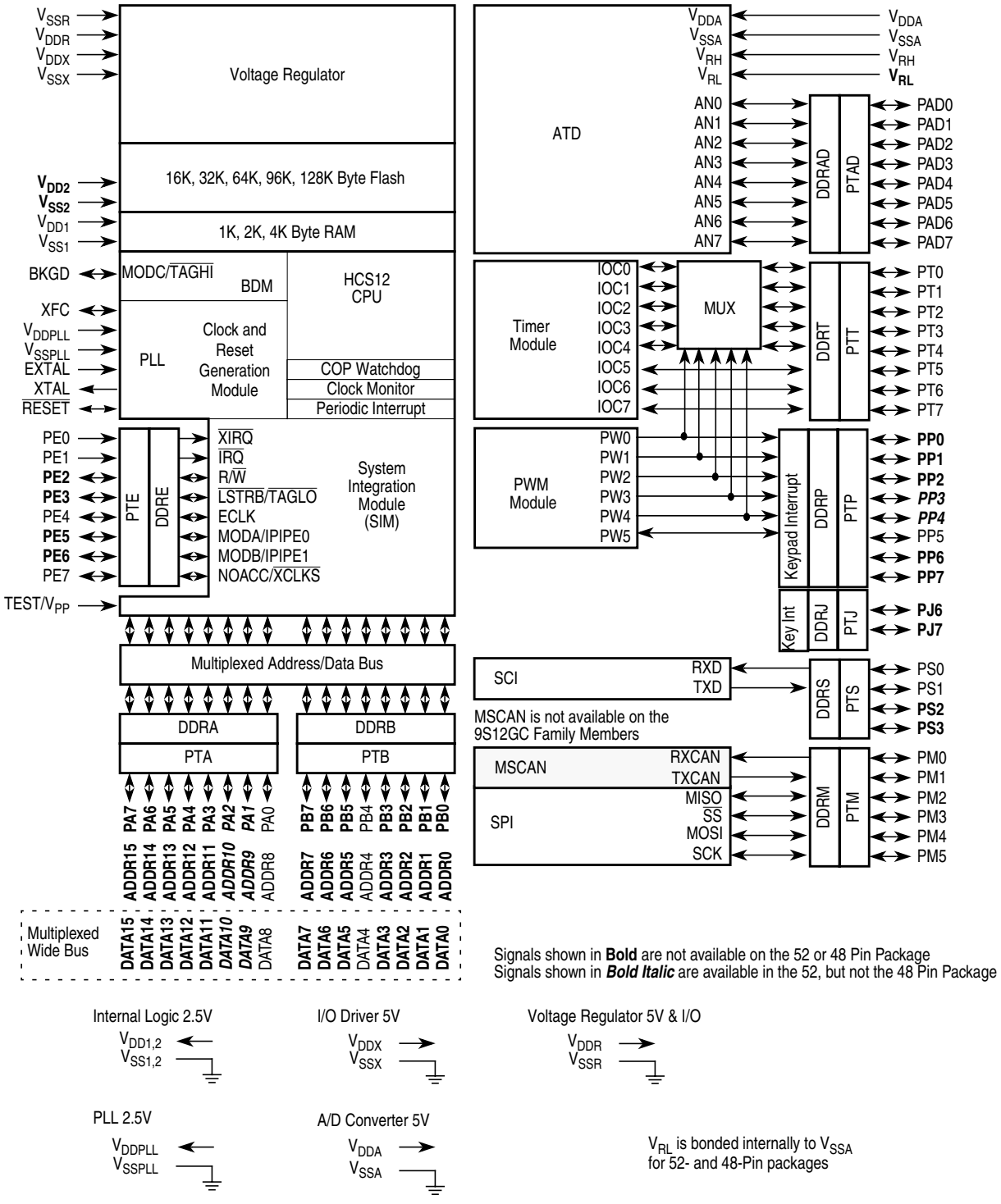


Figure 1-1. MC9S12C-Family / MC9S12GC-Family Block Diagram

1.2 Memory Map and Registers

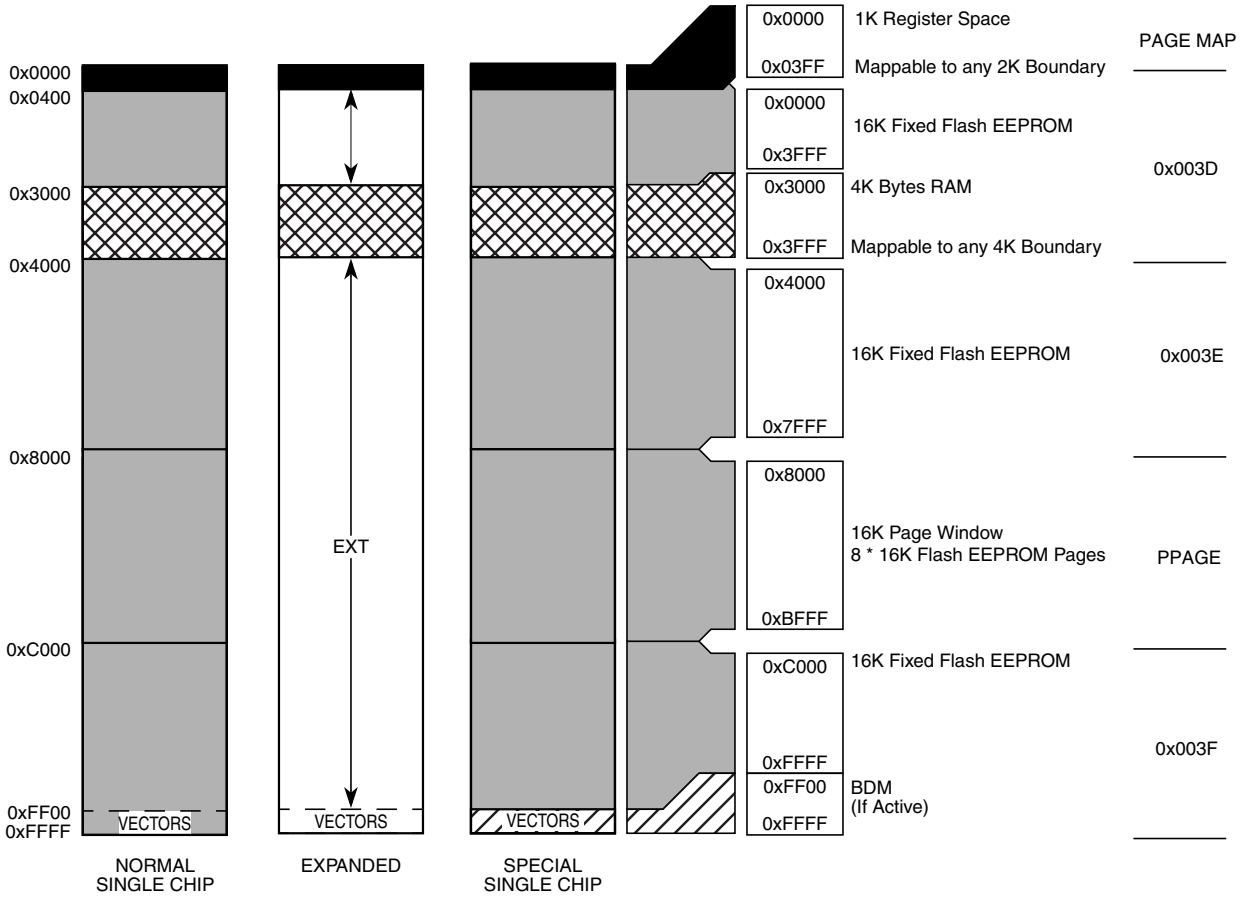
1.2.1 Device Memory Map

Table 1-1 shows the device register map after reset. Figure 1-2 through Figure 1-6 illustrate the full device memory map.

Table 1-1. Device Register Map Overview

Address	Module	Size
0x0000–0x0017	Core (ports A, B, E, modes, inits, test)	24
0x0018	Reserved	1
0x0019	Voltage regulator (VREG)	1
0x001A–0x001B	Device ID register	2
0x001C–0x001F	Core (MEMSIZ, IRQ, HPRIO)	4
0x0020–0x002F	Core (DBG)	16
0x0030–0x0033	Core (PPAGE[1])	4
0x0034–0x003F	Clock and reset generator (CRG)	12
0x0040–0x006F	Standard timer module (TIM)	48
0x0070–0x007F	Reserved	16
0x0080–0x009F	Analog-to-digital converter (ATD)	32
0x00A0–0x00C7	Reserved	40
0x00C8–0x00CF	Serial communications interface (SCI)	8
0x00D0–0x00D7	Reserved	8
0x00D8–0x00DF	Serial peripheral interface (SPI)	8
0x00E0–0x00FF	Pulse width modulator (PWM)	32
0x0100–0x010F	Flash control register	16
0x0110–0x013F	Reserved	48
0x0140–0x017F	Scalable controller area network (MSCAN)[2]	64
0x0180–0x023F	Reserved	192
0x0240–0x027F	Port integration module (PIM)	64
0x0280–0x03FF	Reserved	384

1. External memory paging is not supported on this device (Section 1.7.1, "PPAGE").
2. Not available on MC9S12GC Family devices

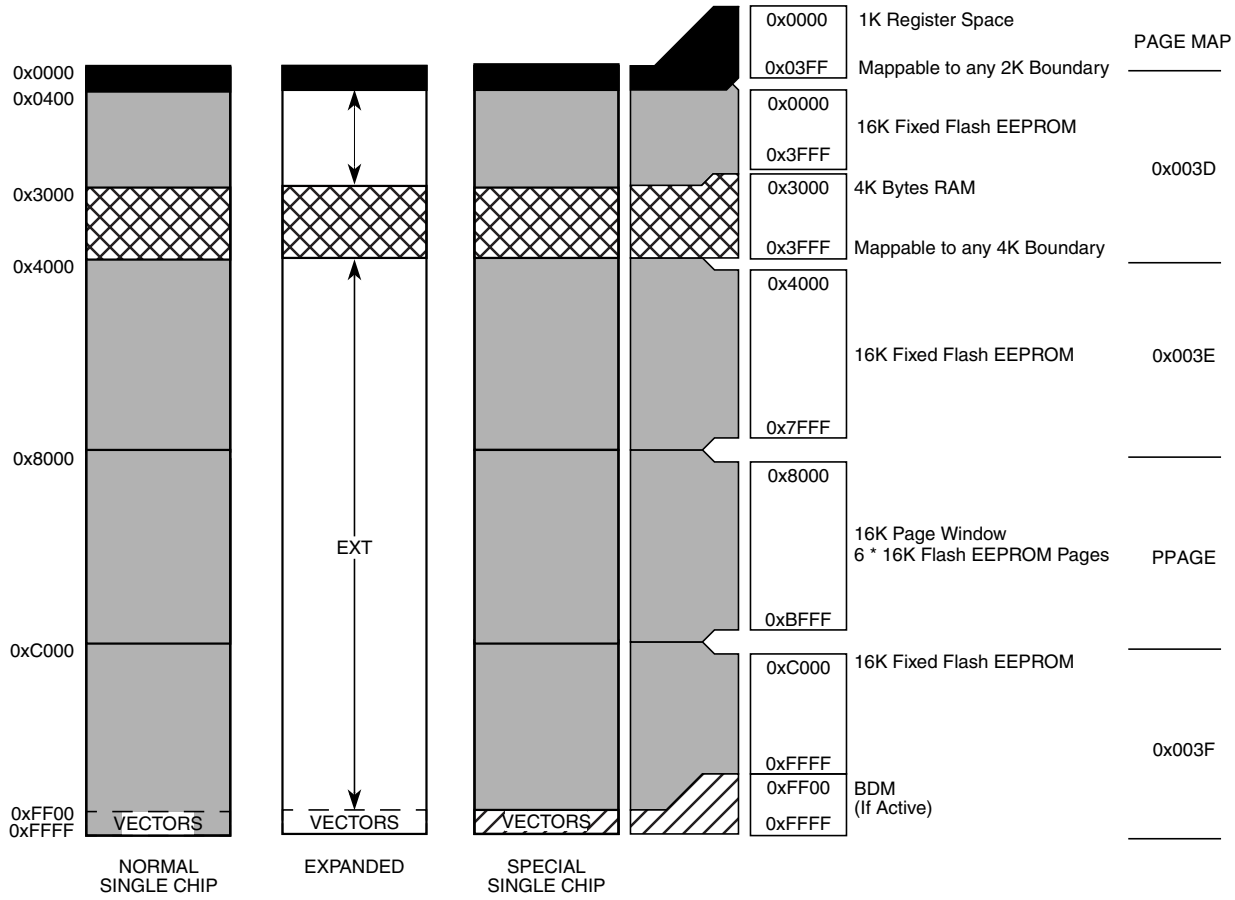


The figure shows a useful map, which is not the map out of reset. After reset the map is:

0x0000–0x03FF: Register Space
0x0000–0x0FFF: 4K RAM (only 3K visible 0x0400–0x0FFF)

Flash erase sector size is 1024 bytes

Figure 1-2. MC9S12C128 and MC9S12GC128 User Configurable Memory Map

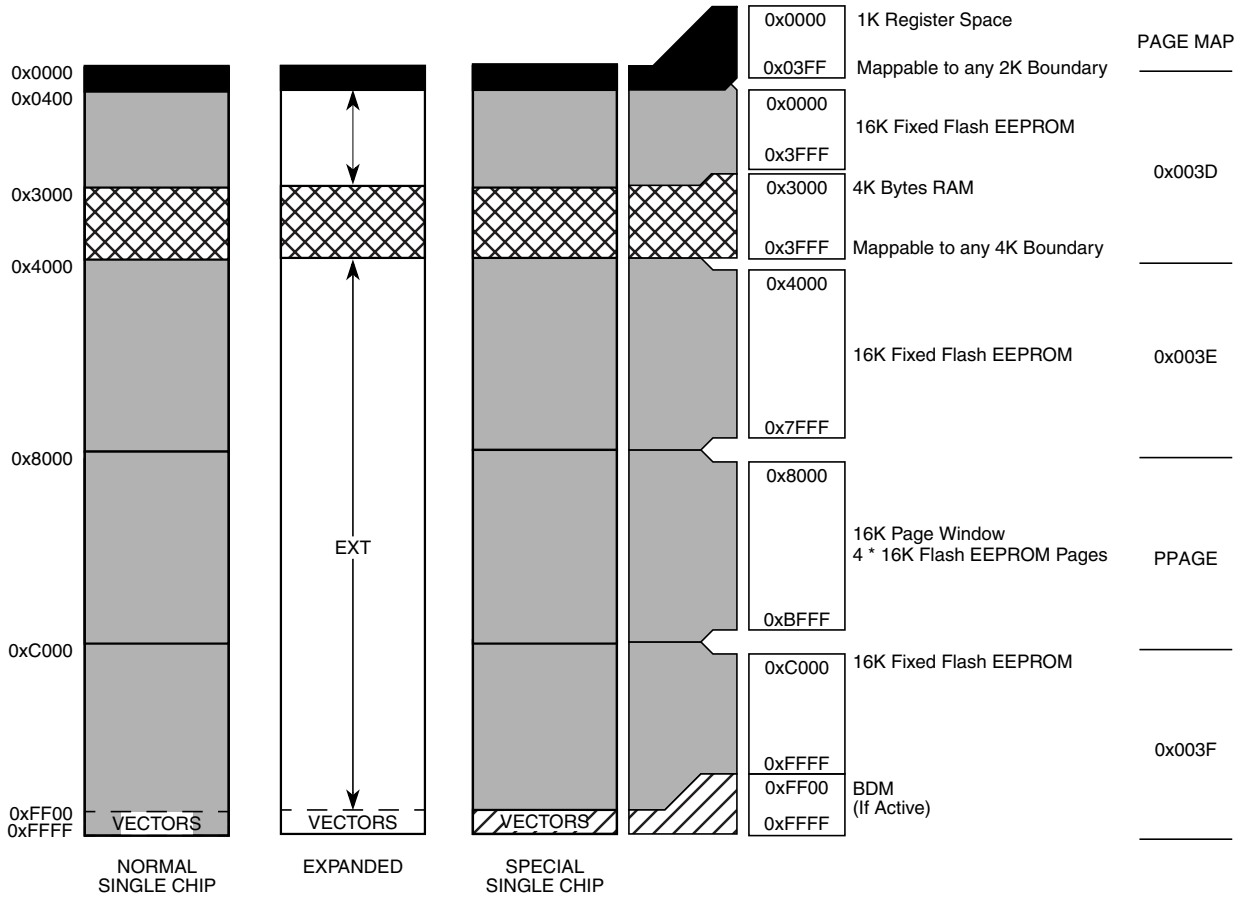


The figure shows a useful map, which is not the map out of reset. After reset the map is:

0x0000–0x03FF: Register Space
0x0000–0x0FFF: 4K RAM (only 3K visible 0x0400–0x0FFF)

Flash erase sector size is 1024 bytes

Figure 1-3. MC9S12C96 and MC9S12GC96 User Configurable Memory Map



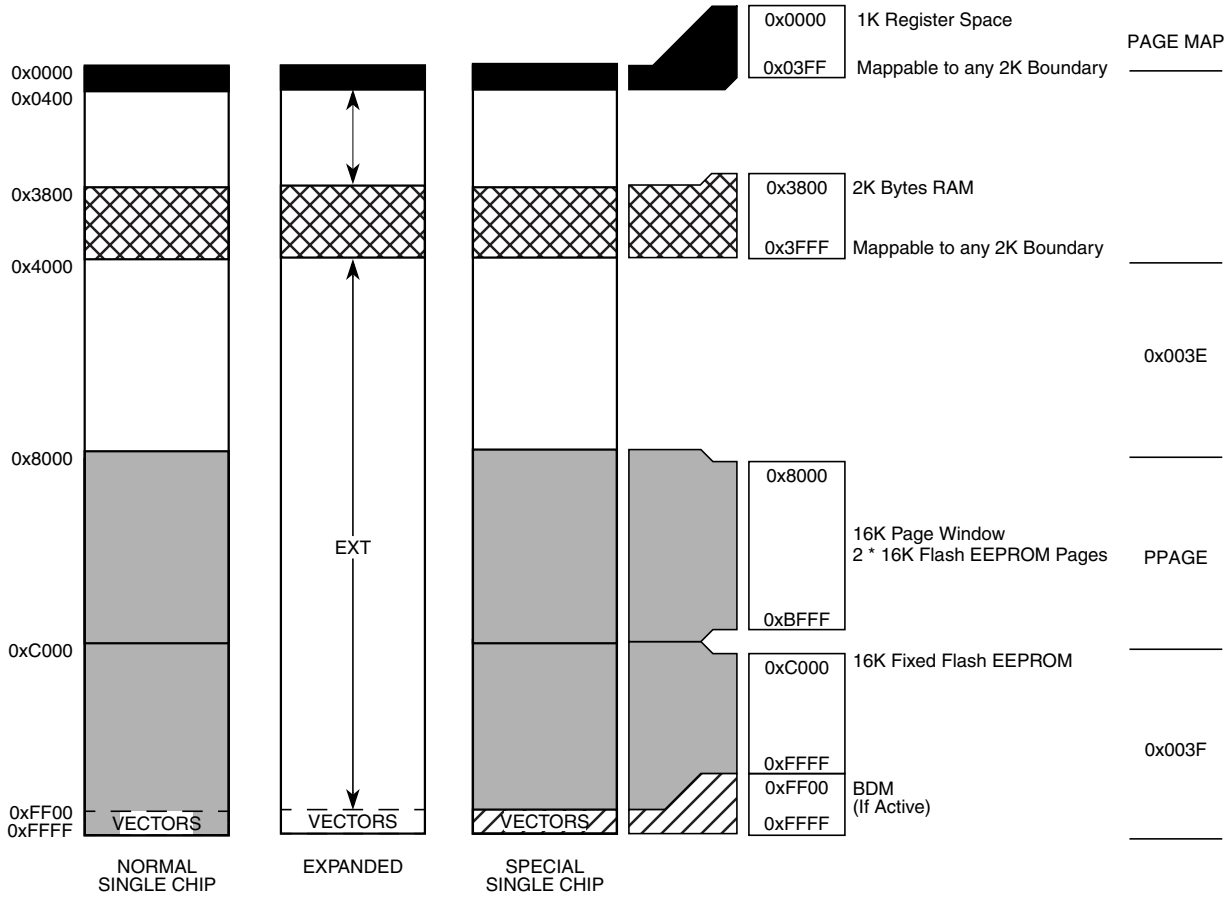
The figure shows a useful map, which is not the map out of reset. After reset the map is:

0x0000–0x03FF: Register space

0x0000–0x0FFF: 4K RAM (only 3K visible 0x0400–0x0FFF)

Flash erase sector size is 1024 Bytes

Figure 1-4. MC9S12C64 and MC9S12GC64 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

0x0000–0x03FF: Register space
0x0800–0x0FFF: 2K RAM

Flash erase sector size is 512 bytes

The flash page 0x003E is visible at 0x4000–0x7FFF in the memory map if ROMHM = 0.

In the figure ROMHM = 1 removing page 0x003E from 0x4000–0x7FFF.

Figure 1-5. MC9S12C32 and MC9S12GC32 User Configurable Memory Map