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MC9S12DT128

Device User Guide

Covers MC9S12DT128E, MC9S12DG128E, MC9S12DJ128E, MC9S12DG128, MC9S12DJ128, MC9S12DB128, MC9S12A128, SC515846, SC515847, SC515848, SC515849, SC101161DT, SC101161DG, SC101161DJ, SC102202, SC102203, SC102204, SC102205

HCS12
Microcontrollers

9S12DT128DGV2/D
V02.17
03 Jun 2010

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	18 Jun 2001	18 June 2001		Initial version (parent doc v2.03 dug for dp256).
V01.01	23 July 2001	23 July 2001		Updated version after review
V01.02	23 Sep 2001	23 Sep 2001		Changed Partname, added pierce mode, updated electrical characteristics some minor corrections
V01.03	12 Oct 2001	12 Oct 2001		Replaced Star12 by HCS12
V01.04	27 Feb 2002	27 Feb 2002		Updated electrical spec after MC-Qualification (IOL/IOH), Data for Pierce, NVM reliability New document numbering. Corrected Typos
V01.05	4 Mar 2002	4 Mar 2002		Increased VDD to 2.35V, removed min. oscillator startup Removed Document order number except from Cover Sheet
V01.06	8 July 2002	22 July 2002		Added: Pull-up columns to signal table, example for PLL Filter calculation, Thermal values for junction to board and package, BGND pin pull-up Part Order Information Global Register Table Chip Configuration Summary Modified: Reduced Wait and Run IDD values Mode of Operation chapter changed leakage current for ADC inputs down to +-1uA Corrected: Interrupt vector table enable register inconsistencies PCB layout for 80QFP VREGEN position
V02.00	11 Jan 2002	11 Jan 2002		NEW MASKSET Changed part number from DTB128 to DT128 Functional Changes: ROMCTL changes in Emulation Mode 80 Pin Byteflight package Option available Flash with 2 Bit Backdoor Key Enable Additional CAN0 routing to PJ7,6 Improved BDM with sync and acknowledge capabilities New Part ID number Improvements: Significantly improved NVM reliability data Corrections: Interrupt vector Table
V02.01	01 Feb 2002	01 Feb 2002		Updated Block User Guide versions in preface Updated Appendix A Electrical Characteristics

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.02	08 Mar 2002	08 Mar 2002		Changed XCLKS to PE7 in Table 2-2 Updated device part numbers in Figure 2-1 Updated BDM clock in Figure 3-1 Removed SIM description in overview & n_{UPOSC} spec in Table A-15 Updated electrical spec of VDD & VDDPLL (Table A-4), IOL/IOH (Table A-6), C_{INS} (Table A-9), C_{IN} (Table A-6 & A-15), Updated interrupt pulse timing variables in Table A-6 Updated device part numbers in Figure 2-1 Added document numbers on cover page and Table 0-2
V02.03	14 Mar 2002	14 Mar 2002		Cleaned up Fig. 1-1, 2-1 Updated Section 1.5 descriptions Corrected PE assignment in Table 2-2, Fig. 2-5,6,7. Corrected NVM sizes in Sections 16, 17 Added I_{REF} spec for 1ATD in Table A-8 Added Blank Check in A.3.1.5 and Table A-11 Updated CRG spec in Table A-15
V02.04	16 Aug 2002	16 Aug 2002		Added: Pull-up columns to signal table, Example for PLL Filter calculation, Thermal values for junction to board and package, BGND pin pull-up Part Order Information Global Register Table Chip Configuration Summary Device specific info on CRG Modified: Reduced Wait and Run IDD values Mode of Operation chapter Changed leakage current for ADC inputs down to +-1uA Minor modification of PLL frequency/ voltage gain values Corrected: Pin names/functions on 80 pin packages Interrupt vector table enable register inconsistencies PCB layout for 80QFP VREGEN position
V02.05	12 Sep 2002	12 Sep 2002		Corrected: Register address mismatches in 1.5.1
V02.06	06 Nov 2002	06 Nov 2002		Removed document order no. from Revision History pages Renamed "Preface" section to "Derivative Differences and Document references". Added details for derivatives missing CAN0/1/4, BDLC, IIC and/or Byteflight Added 2L40K mask set in section 1.6 Added OSC User Guide in Preface, “Document References” Added oscillator clock connection to BDM in S12_CORE in fig 3-1 Corrected several register and bit names in “Local Enable” column of Table 5.1 Interrupt Vector Locations Section HCS12 Core Block Description: mentioned alternate clock of BDM to be equivalent to oscillator clock Added new section: “Oscillator (OSC) Block Description” Corrected in footnote of Table "PLL Characteristics": fOSC = 4MHz

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.07	29 Jan 2003	29 Jan 2003		Added 3L40K mask set in section 1.6 Corrected register entries in section 1.5.1 “Detailed Memory Map” Updated description for ROMCTL in section 2.3.31 Updated section 4.3.3 “Unsecuring the Microcontroller” Corrected and updated device-specific information for OSC (section 8.1) & Byteflight (section 15.1) Updated footnote in Table A-4 “Operating Conditions” Changed reference of VDDM to VDDR in section A.1.8 Removed footnote on input leakage current in Table A-6 “5V I/O Characteristics”
V02.08	26 Feb 2003	26 Feb 2003		Added part numbers MC9S12DT128E, MC9S12DG128E, and MC9S12DJ128E in “Preface” and related part number references Removed mask sets 0L40K and 2L40K from Table 1-3
V02.09	15 Oct 2003	15 Oct 2003		Replaced references to HCS12 Core Guide by the individual HCS12 Block guides in Table 0-2, section 1.5.1, and section 6; updated Fig.3-1 “Clock Connections” to show the individual HCS12 blocks Corrected PIM module name and document order number in Table 0-2 “Document References” Corrected ECT pulse accumulators description in section 1.2 “Features” Corrected KWP5 pin name in Fig 2-1 112LQFP pin assignments Corrected pull resistor CTRL/reset states for PE7 and PE4-PE0 in Table 2.1 “Signal Properties” Mentioned “S12LRAE” bootloader in Flash section 17 Corrected footnote on clamp of TEST pin under Table A-1 “Absolute Maximum Ratings” Corrected minimum bus frequency to 0.25MHz in Table A-4 “Operating Conditions” Replaced “burst programming” by “row programming” in A.3 “NVM, Flash and EEPROM” Corrected blank check time for EEPROM in Table A-11 “NVM Timing Characteristics” Corrected operating frequency in Table A-18 “SPI Master/Slave Mode Timing Characteristics
V02.10	6 Feb 2004	6 Feb 2004		Added A128 information in “Derivative Differences”, 2.1 “Device Pinout”, 2.2 “Signal Properties Summary”, Fig 23-2 & Fig 23-4 Added lead-free package option (PVE) in Table 0-2 “Derivative Differences for MC9S12DB128” and Fig 0-1 “Order Partnumber Example” Added an “AEC qualified” row in the “Derivative Differences” tables 0-1 & 0-2.
V02.11	3 May 2004	3 May 2004		Added part numbers SC515846, SC515847, SC515848, and SC515849 in “Derivative Differences” tables 0-1 & 0-2, section 2, and section 23. Corrected and added maskset 4L40K in tables 0-1 & 0-2 and section 1.6. Corrected BDLC module availability in DB128 80QFP part in “Derivative Differences” table 0-2.

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.12	06 Dec 2004	06 Dec 2004		Added maskset 0L94R Added items $V_{IH,EXTAL}$, $V_{IL,EXTAL}$, & $V_{HYS,EXTAL}$ in table A-15 “Oscillator characteristics” Removed item “Oscillator” from table A-4 “Operating Conditions” as it is already covered in table “Oscillator Characteristics”
V02.13	04 Mar 2005	04 Mar 2005		Amended feature list of A128 in Table 0-1 “Derivative Differences”
V02.14	28 Apr 2005	28 Apr 2005		Updated cover page Added part numbers SC101161DT, SC101161DG, SC101161DJ, SC102202, SC102203, SC102204, & SC102205 Added masksets 5L40K &1L59W Changed T_{Javg} to 85°C in table A-12 “NVM Reliability” & added footnote concerning data retention
V02.15	05 Oct 2005	05 Oct 2005		Updated “NVM Reliability” table A-12 format with added data. Added figure A-2 “Typical Endurance vs Temperature”
V02.16	12 Apr 2008	12 Apr 2008		Added maskset 2L94R
V02.17	3 Jun 2010	3 Jun 2010		Added maskset 1L59W for MC9S12A128

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Derivative Differences and Document References

Derivative Differences

(Table 0-1) and **(Table 0-2)** show the availability of peripheral modules on the various derivatives. For details about the compatibility within the MC9S12D-Family refer also to engineering bulletin EB386.

Table 0-1 Derivative Differences[1]

Modules	MC9S12DT128E[3] MC9S12DT128 SC515849[4] SC101161DT[5] SC102205[6]	MC9S12DG128E[3] MC9S12DG128 SC515847[4] SC101161DG[5] SC102203[6]	MC9S12DJ128E[3] MC9S12DJ128 SC515848[4] SC101161DJ[5] SC102204[6]	MC9S12A128
# of CANs	3	2	2	0
CAN4	✓	✓	✓	×
CAN1	✓	×	×	×
CAN0	✓	✓	✓	×
J1850/BDLC	×	×	✓	×
IIC	✓	✓	✓	✓
Byteflight	×	×	×	×
Package	112 LQFP	112 LQFP/80 QFP[2]	112 LQFP/80 QFP[2]	112 LQFP/80 QFP[2]
Package Code	PV	PV/FU	PV/FU	PV/FU
Mask set	1L40K[3], 3L40K, 0L94R, 4L40K[4], 1L59W[5], 5L40K[6], 2L94R	1L40K[3], 3L40K, 0L94R, 4L40K[4], 1L59W[5], 5L40K[6], 2L94R	1L40K[3], 3L40K, 0L94R, 4L40K[4], 1L59W[5], 5L40K[6], 2L94R	3L40K, 0L94R, 2L94R, 1L59W
Temp Options	M, V, C	M, V, C	M, V, C	C
AEC qualified	Yes	Yes	Yes	No
Notes	An errata exists contact Sales Office	An errata exists contact Sales Office	An errata exists contact Sales Office	An errata exists contact Sales Office

Table 0-2 Derivative Differences for MC9S12DB128[1]

Modules	MC9S12DB128 SC515846[4] SC102202[6]	MC9S12DB128 SC515846[4] SC102202[6]
# of CANs	2	0
CAN4	✓	×
CAN1	×	×
CAN0	✓	×
J1850/BDLC	×	×
IIC	×	×
Byteflight	✓	✓
Package	112 LQFP	80 QFP[2]

Modules	MC9S12DB128 SC515846[4] SC102202[6]	MC9S12DB128 SC515846[4] SC102202[6]
Package Code	PV/PVE	FU
Mask set	3L40K, 0L94R, 4L40K[4], 5L40K[6], 2L94R	3L40K, 0L94R, 4L40K[4], 5L40K[6], 2L94R
Temp Options	M, V, C/M, V	M, V, C
AEC qualified	Yes	Yes
Notes	An errata exists contact Sales Office	An errata exists contact Sales Office

NOTE:
1. ✓: Available for this device, ×: Not available for this device.
2. 80 Pin bond-out for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204 is the same; MC9S12DB128, SC515846, and SC102202 have a different bond-out.
3. Part numbers MC9S12DT128E, MC9S12DG128E, and MC9S12DJ128E are associated with the mask set 1L40K.
4. Part numbers SC515846, SC515847, SC515848, and SC515849 are associated with the mask set 4L40K.
5. Part numbers SC101161DT, SC101161DG, SC101161DJ are associated with the mask set 1L59W.
6. Part numbers SC102202, SC102203, SC102204, and SC102205 are associated with the mask set 5L40K which is not for volume production.

The following figure provides an ordering number example for the MC9S12D128 devices.

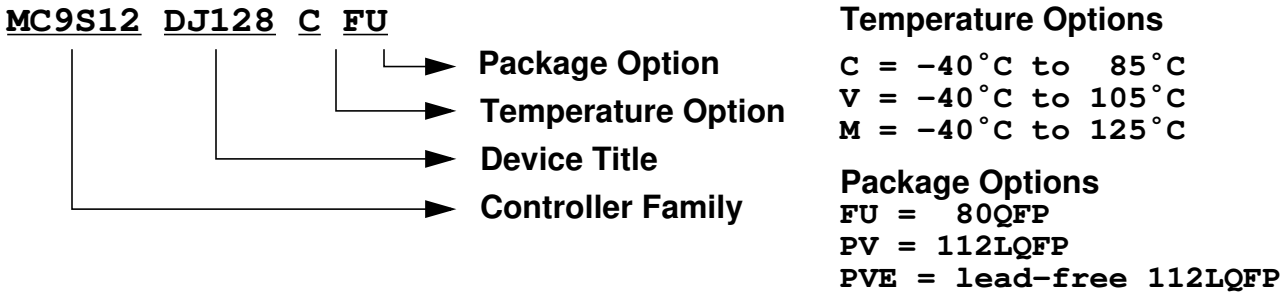

Figure 0-1 Order Partnumber Example

The following items should be considered when using a derivative.

- **Registers**
  - Do not write or read CAN0 registers (after reset: address range $0140 - $017F), if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write or read CAN1 registers (after reset: address range $0180 - $01BF), if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write or read CAN4 registers (after reset: address range $0280 - $02BF), if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write or read BDLC registers (after reset: address range $00E8 - $00EF), if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write or read IIC registers (after reset: address range $00E0 - $00E7), if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).

- Do not write or read Byteflight registers (after reset: address range $0300 - $035F), if using a derivative without Byteflight registers (see **(Table 0-1)** and **(Table 0-2)**).

- **Interrupts**
  - Fill the four CAN0 interrupt vectors ($FFB0 - $FFB7) according to your coding policies for unused interrupts, if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four CAN1 interrupt vectors ($FFA8 - $FFAF) according to your coding policies for unused interrupts, if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four CAN4 interrupt vectors ($FF90 - $FF97) according to your coding policies for unused interrupts, if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the BDLC interrupt vector ($FFC2, $FFC3) according to your coding policies for unused interrupts, if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the IIC interrupt vector ($FFC0, $FFC1) according to your coding policies for unused interrupts, if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).
  - Fill the four Byteflight interrupt vectors ($FFA0 - $FFA7) according to your coding policies for unused interrupts, if using a derivative without Byteflight (see **(Table 0-1)** and **(Table 0-2)**).

- **Ports**
  - The CAN0 pin functionality (TXCAN0, RXCAN0) is not available on port PJ7, PJ6, PM5, PM4, PM3, PM2, PM1 and PM0, if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - The CAN1 pin functionality (TXCAN1, RXCAN1) is not available on port PM3 and PM2, if using a derivative without CAN1 (see **(Table 0-1)** and **(Table 0-2)**).
  - The CAN4 pin functionality (TXCAN4, RXCAN4) is not available on port PJ7, PJ6, PM7, PM6, PM5 and PM4, if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).
  - The BDLC pin functionality (TXB, RXB) is not available on port PM1 and PM0, if using a derivative without BDLC (see **(Table 0-1)** and **(Table 0-2)**).
  - The IIC pin functionality (SCL, SCA) is not available on port PJ7 and PJ6, if using a derivative without IIC (see **(Table 0-1)** and **(Table 0-2)**).
  - The Byteflight pin functionality (BF_PSLM, BF_PERR, BF_PROK, BF_PSYN, TX_BF, RX_BF) is not available on port PM7, PM6, PM5, PM4, PM3 and PM2, if using a derivative without Byteflight (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write MODRR1 and MODRR0 Bit of Module Routing Register (PIM_9DTB128 Block User Guide), if using a derivative without CAN0 (see **(Table 0-1)** and **(Table 0-2)**).
  - Do not write MODRR3 and MODRR2 Bit of Module Routing Register (PIM_9DTB128 Block User Guide), if using a derivative without CAN4 (see **(Table 0-1)** and **(Table 0-2)**).

- **Pins not available in 80 pin QFP package for MC9S12DG128E, MC9S12DG128, MC9S12DJ128E, MC9S12DJ128, MC9S12A128, SC515847, SC515848, SC101161DG, SC101161DJ, SC102203, and SC102204**

- **Port H**
  In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+$0262) to $FF, or enabling the pull resistors by writing a $FF to the pull enable register (PERH at Base+$0264).
- **Port J[1:0]**
  Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[1:0] by clearing the bits PERJ1 and PERJ0 at Base+$026C.
- **Port K**
  Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+$000C. Therefore care must be taken not to clear this bit.
- **Port M[7:6]**
  PM7:6 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
- **Port P6**
  PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.
- **Port S[7:4]**
  PS7:4 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
- **PAD[15:8] (ATD1 channels)**
  Out of reset the ATD1 is disabled preventing current flows in the pins. Do not modify the ATD1 registers!

- **Pins not available in 80 pin QFP package for MC9S12DB128, SC515846, and SC102202**
  - **Port H**
    In order to avoid floating nodes the ports should be either configured as outputs by setting the data direction register (DDRH at Base+$0262) to $FF, or enabling the pull resistors by writing a $FF to the pull enable register (PERH at Base+$0264).
  - **Port J[7:6, 1:0]**
    Port J pull-up resistors are enabled out of reset on all four pins (7:6 and 1:0). Therefore care must be taken not to disable the pull enables on PJ[7:6, 1:0] by clearing the bits PERJ7, PERJ6, PERJ1 and PERJ0 at Base+$026C.
  - **Port K**
    Port K pull-up resistors are enabled out of reset, i.e. Bit 7 = PUKE = 1 in the register PUCR at Base+$000C. Therefore care must be taken not to clear this bit.
  - **Port M[1:0]**
    PM1:0 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.
  - **Port P6**
    PP6 must be configured as output or its pull resistor must be enabled to avoid a floating input.

– **Port S[3:2]**
PS3:2 must be configured as outputs or their pull resistors must be enabled to avoid floating inputs.

– **PAD[15:8] (ATD1 channels)**
Out of reset the ATD1 is disabled preventing current flows in the pins. Do not modify the ATD1 registers!

Document References

The Device User Guide provides information about the MC9S12DT128 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes all the individual Block User Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block User Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-3** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-3 Document References

User Guide	Version	Document Order Number
HCS12 CPU Reference Manual	V02	S12CPUV2/D
HCS12 Module Mapping Control (MMC) Block Guide	V04	S12MMCV4/D
HCS12 Multiplexed External Bus Interface (MEBI) Block Guide	V03	S12MEBIV3/D
HCS12 Interrupt (INT) Block Guide	V01	S12INTV1/D
HCS12 Background Debug Module (BDM) Block Guide	V04	S12BDMV4/D
HCS12 Breakpoint (BKP) Block Guide	V01	S12BKPV1/D
Clock and Reset Generator (CRG) Block User Guide	V04	S12CRGV4/D
Oscillator (OSC) Block User Guide	V02	S12OSCV2/D
Enhanced Capture Timer 16 Bit 8 Channel (ECT_16B8C) Block User Guide	V01	S12ECT16B8CV1/D
Analog to Digital Converter 10 Bit 8 Channel (ATD_10B8C) Block User Guide	V02	S12ATD10B8CV2/D
Inter IC Bus (IIC) Block User Guide	V02	S12IICV2/D
Asynchronous Serial Interface (SCI) Block User Guide	V02	S12SCIV2/D
Serial Peripheral Interface (SPI) Block User Guide	V02	S12SPIV2/D
Pulse Width Modulator 8 Bit 8 Channel (PWM_8B8C) Block User Guide	V01	S12PWM8B8CV1/D
128K Byte Flash (FTS128K) Block User Guide	V02	S12FTS128KV2/D
2K Byte EEPROM (EETS2K) Block User Guide	V01	S12EETS2KV1/D
Byte Level Data Link Controller -J1850 (BDLC) Block User Guide	V01	S12BDLCV1/D
Motorola Scalable CAN (MSCAN) Block User Guide	V02	S12MSCANV2/D
Voltage Regulator (VREG) Block User Guide	V01	S12VREGV1/D
Port Integration Module (PIM_9DTB128) Block User Guide	V02	S12DTB128PIMV2/D
Byteflight (BF) Block User Guide	V01	S12BFV1/D

Section 1 Introduction

1.1 Overview

The MC9S12DT128 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 128K bytes of Flash EEPROM, 8K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), two serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wakeup capability, three CAN 2.0 A, B software compatible modules (MSCAN12), a Byteflight module and an Inter-IC Bus. The MC9S12DT128 has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer's model identical to M68HC11
    iii. 20-bit ALU
    iv. Instruction queue
    v. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)
  - BDM (Background Debug Module)
- CRG (Clock and Reset Generator)
  - Choice of low current Colpitts oscillator or standard Pierce Oscillator
  - PLL
  - COP watchdog
  - real time interrupt
  - clock monitor
- 8-bit and 4-bit ports with interrupt functionality