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9S12DP256BDGV2/D

MC9S12DP256B
Device User Guide
V02.14

Covers also

MC9S12DT256C, MC9S12DJ256C, MC9S12DG256C, MC9S12DT256B, MC9S12DJ256B, MC9S12DG256B MC9S12A256B

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	29 MAR 2001	29 MAR 2001		Initial version.
V01.01	8 MAY 2001	8 MAY 2001		VDD5 spec change 4.5V . . 5.25V Current Injection on single pin +- 2.5mA added DC bias level on EXTAL pin minor cosmetics and corrected typos
V02.00	16 May 2001	16 May 2001		changed ATD Electrical Characteristics seperate coupling ratio for positive and negative bulk current injection added pinout for 80QFP corrected SPI timing
V02.01	5 June 2001			corrected Expanded Bus Timing Characteristics
V02.02	14 June 2001			Some corrections on pin usage after review
V02.03	18 June 2001			Minor corrections with respect to format and wording Added SRAM data retention disclaimer
V02.04	26 June 2001			Changed Oscillator Characteristics t_{CQOUT} max 2.5s and replaced Clock Monitor Time-out by Clock Monitor Failure Assert Frequency Changed Self Clock Mode Frequency min 1MHz and max 5.5MHz Changed I_{DDPS} (RTI and COP disabled) to 400uA
V02.05	11 July 2001			Corrected f_{ref} and REFDV/SYNR Settings for PLL Stabilization Delay Measurements, added t_{EXTR} and t_{EXTF} to Oscillator Characteristics, Corrected t_{EXTL} and t_{EXTH} values
V02.06	17 July 2001			Added thermal resistance for LQFP 80, added PCB layout proposal for power and ground connections
V02.07	24 July 2001			Added Document Names Variable definitions and Names have been hidden Added Maskset 1K79X Modified description in chapter A.5.2 Oscillator

Version Number	Revision Date	Effective Date	Author	Description of Changes
V02.08	24 August 2001			Corrected local enable bits in interrupt vector table Corrected #33 - #36 in table A-20 A.4 Voltage Regulator characteristics was removed A.1 to A.7 major rework according to feedback from PE
V02.09	12 Nov 2001			Changed document name and title to MC9.. Added table containing other devices covered by this document Added NVM Blank check specificaiton Added external ADC trigger to pin description Updated A-7 Supply Current Characteristics Updated Table0-1 Derivative Differences Added Item8 to Table A-8
V02.10	28 Feb 2002			IOL/IOH reduced to 10mA/2mA for full/reduced drive Changed ATD characteristic Cins max to 22pF Changed VDD min VDDPLL min to 2.35V Removed Oscillator startup time from POR or STOP changed input capacitance for standard i/o pin to 6pF
V02.11	26 Mar 2002			Corrected NVM reliability spec
V02.12	12Aug 2002			added derivative differences for part number MC9S12D256C added partID and maskset number for MC9S12D256D added table with fixed defects on 2K79X added table for HCS12 core configuration Added detailed register map Added pull device description to signal table
V02.13	25Sep 2002			corrected tables 0-1 and 0-2 Derivative Differences added 80QFP DG256 pin assignment diagram
V02.14	28Feb 2003			added A256B parts to table 0-1 Derivative Differences

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Section 4 Modes of Operation

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Section 6 HCS12 Core Block Description

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Preface

The Device User Guide provides information about the MC9S12DP256B device made up of standard HCS12 blocks and the HCS12 processor core.

Table 0-1 and **Table 0-2** show the availability of peripheral modules on the various derivatives. For details about the compatibility within the MC9S12D-Family refer also to engineering bulletin EB386.

Table 0-1 Drivative Differences MC9S12D256B

Generic device	MC9S12DP256B	MC9S12DT256B	MC9S12DJ256B	MC9S12DG256B	MC9S12A256B
# of CANs	5	3	2	2	0
CAN0	✓	✓	✓	✓	
CAN1	✓	✓			
CAN2	✓				
CAN3	✓				
CAN4	✓	✓	✓	✓	
J1850/BDLC	✓		✓		
Package	112 LQFP	112 LQFP	112 LQFP/80 QFP	112 LQFP/80 QFP	112 LQFP/80 QFP
Mask set	0/1K79X	0/1K79X	0/1K79X	0/1K79X	0/1K79X
Temp Options	M, V, C	M, V, C	M, V, C	M, V, C	C
package Code	PV	PV	PV/FU	PV	PV/FU
Notes	An errata exists conntact Sales office	An errata exists conntact Sales office	An errata exists conntact Sales office	An errata exists conntact Sales office	An errata exists conntact Sales office

Table 0-2 Derivative Differences MC9S12D256C

Generic device	MC9S12DP256C	MC9S12DT256C	MC9S12DJ256C	MC9S12DG256C
# of CANs	5	3	2	2
CAN0	✓	✓	✓	✓
CAN1	✓	✓		
CAN2	✓			
CAN3	✓			
CAN4	✓	✓	✓	✓
J1850/BDLC	✓		✓	
Package	112 LQFP	112 LQFP	112 LQFP/80 QFP	112 LQFP/80 QFP
Mask set	2K79X	2K79X	2K79X	2K79X
Temp Options	M, V, C	M, V, C	M, V, C	M, V, C
package Code	PV	PV	PV/FU	PV
Notes	An errata exists conntact Sales office	An errata exists conntact Sales office	An errata exists conntact Sales office	An errata exists conntact Sales office

Table 0-3 shows the defects fixed on maskset 2K79X (MC9S12DP256C)

Table 0-3 Defects fixed on Maskset 2K79X

Defect	Headline
MUCts00510	SCI interrupt asserts only if odd number of interrupts active
MUCts00604	Security in Normal Single Chip mode
MUCts00603	Security in Normal Single Chip mode

This document is part of the customer documentation. A complete set of device manuals also includes the HCS12 Core User Guide and all the individual Block User Guides of the implemented modules. In a effort to reduce redundancy all module specific information is located only in the respective Block User Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

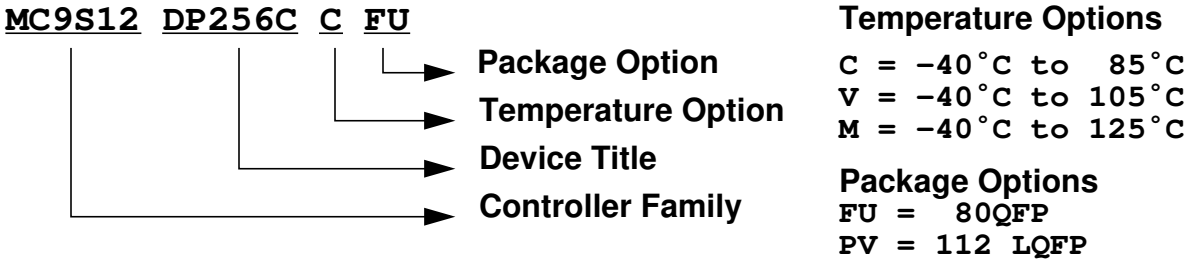


Figure 0-1 Order Part Number Example

See **Table 0-4** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-4 Document References

User Guide	Version	Document Order Number
HCS12 V1.5 Core User Guide	1.2	HCS12COREUG
CRG Block User Guide	V02	S12CRGV2/D
ECT_16B8C Block User Guide	V01	S12ECT16B8CV1/D
ATD_10B8C Block User Guide	V02	S12ATD10B8CV2/D
IIC Block User Guide	V02	S12IICV2/D
SCI Block User Guide	V02	S12SCIV2/D
SPI Block User Guide	V02	S12SPIV2/D
PWM_8B8C Block User Guide	V01	S12PWM8B8CV1/D
FTS256K Block User Guide	V02	S12FTS256KV2/D
EETS4K Block User Guide	V02	S12EETS4KV2/D
BDLC Block User Guide	V01	S12BDLCV1/D
MSCAN Block User Guide	V02	S12MSCANV2/D
VREG Block User Guide	V01	S12VREGV1/D
PIM_9DP256 Block User Guide	V02	S12PIM9DP256V2/D

Section 1 Introduction

1.1 Overview

The MC9S12DP256 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 256K bytes of Flash EEPROM, 12K bytes of RAM, 4K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), three serial peripheral interfaces (SPI), an 8-channel IC/OC enhanced capture timer, two 8-channel, 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), a digital Byte Data Link Controller (BDLC), 29 discrete digital I/O channels (Port A, Port B, Port K and Port E), 20 discrete digital I/O lines with interrupt and wakeup capability, five CAN 2.0 A, B software compatible modules (MSCAN12), and an Inter-IC Bus. The MC9S12DP256 has full 16-bit data paths throughout. However, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer's model identical to M68HC11
    iii. Instruction queue
    iv. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)
  - BDM (Background Debug Mode)
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- 8-bit and 4-bit ports with interrupt functionality
  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 256K Flash EEPROM
  - 4K byte EEPROM
  - 12K byte RAM

- Two 8-channel Analog-to-Digital Converters
  - 10-bit resolution
  - External conversion trigger capability
- Five 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Enhanced Capture Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 8 PWM channels
  - Programmable period and duty cycle
  - 8-bit 8-channel or 16-bit 4-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
  - Usable as interrupt inputs
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Three Synchronous Serial Peripheral Interface (SPI)
- Byte Data Link Controller (BDLC)
  - SAE J1850 Class B Data Communications Network Interface Compatible and ISO Compatible for Low-Speed (<125 Kbps) Serial Data Communications in Automotive Applications
- Inter-IC Bus (IIC)
  - Compatible with I2C Bus standard
  - Multi-master operation
  - Software programmable for one of 256 different serial clock frequencies
- 112-Pin LQFP package
  - I/O lines with 5V input and drive capability

- 5V A/D converter inputs
- Operation at 50MHz equivalent to 25MHz Bus Speed
- Development support
- Single-wire background debug™ mode (BDM)
- On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Motorola use only**)
  - Special Peripheral Mode (**Motorola use only**)

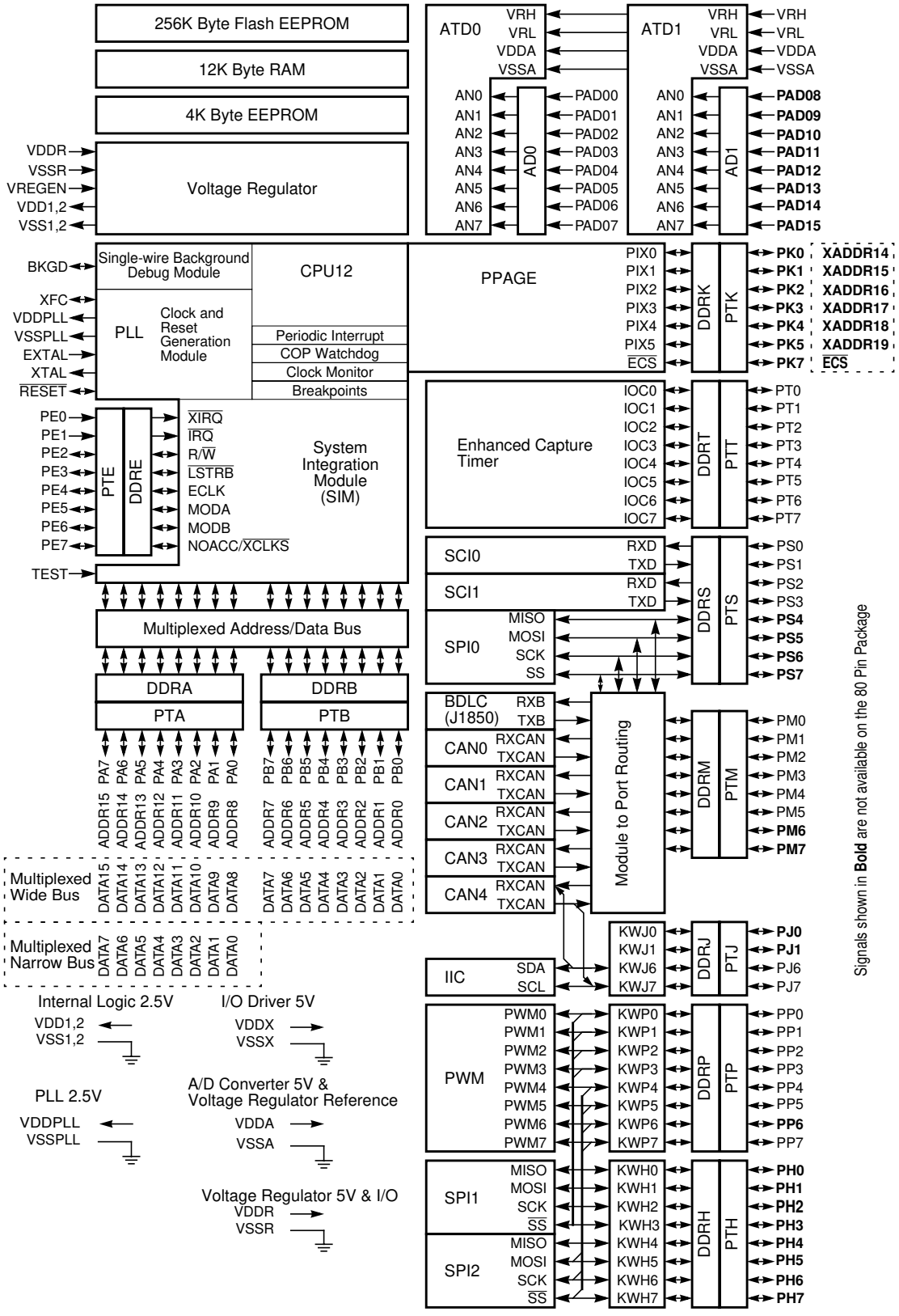
Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12DP256B device.

Figure 1-1 MC9S12DP256B Block Diagram



1.5 Device Memory Map

Table 1-1 and **Figure 1-2** show the device memory map of the MC9S12DP256B after reset. Note that after reset the bottom 1k of the EEPROM ($0000 - $03FF) are hidden by the register space.

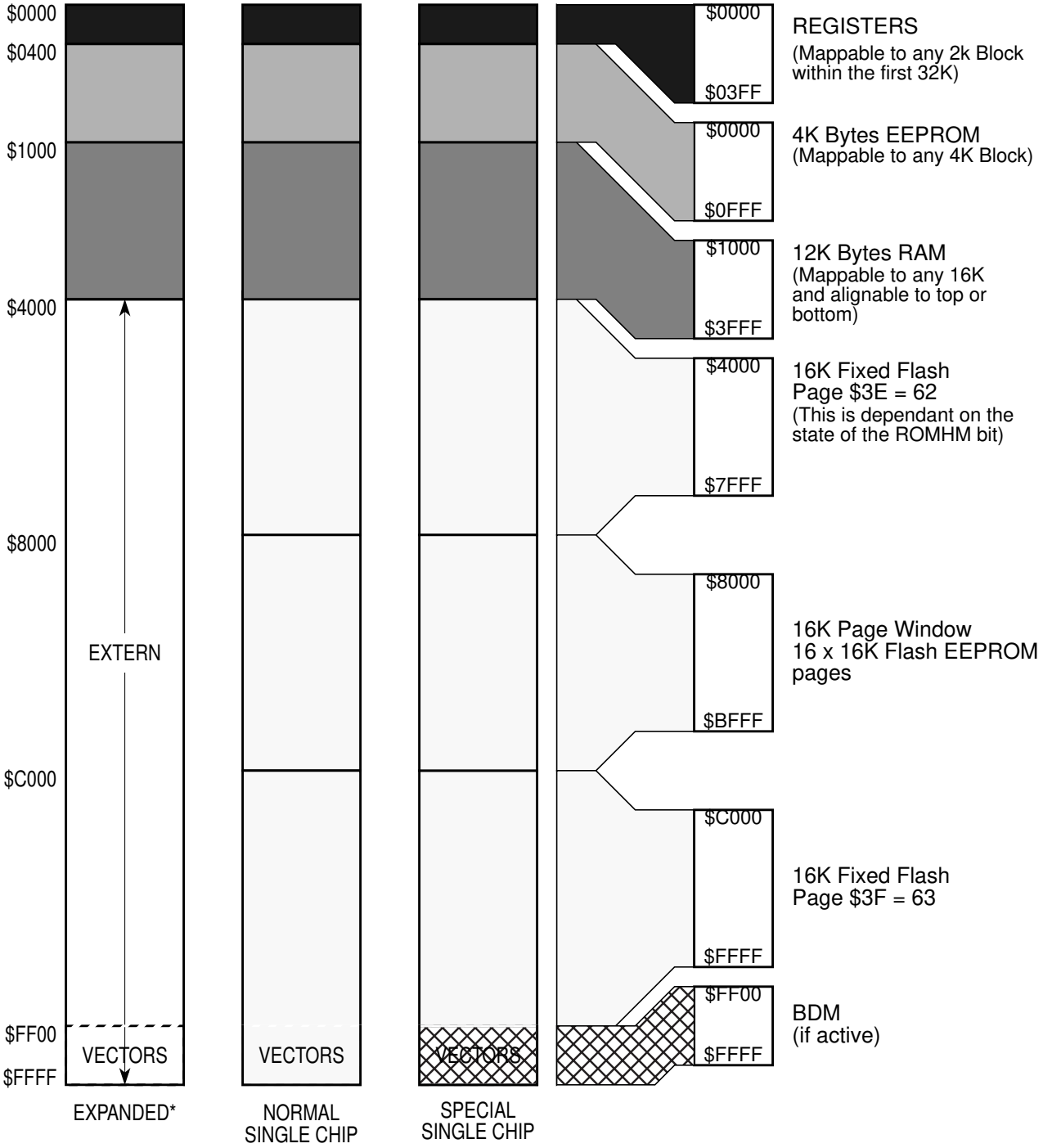
Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$0000 - $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 - $0019	Reserved	2
$001A - $001B	Device ID register (PARTID)	2
$001C - $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 - $0027	Reserved	8
$0028 - $002F	CORE (Background Debug Mode)	8
$0030 - $0033	CORE (PPAGE, Port K)	4
$0034 - $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 - $007F	Enhanced Capture Timer 16-bit 8 channels	64
$0080 - $009F	Analog to Digital Converter 10-bit 8 channels (ATD0)	32
$00A0 - $00C7	Pulse Width Modulator 8-bit 8 channels (PWM)	40
$00C8 - $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 - $00D7	Serial Communications Interface 0 (SCI1)	8
$00D8 - $00DF	Serial Peripheral Interface (SPI0)	8
$00E0 - $00E7	Inter IC Bus	8
$00E8 - $00EF	Byte Data Link Controller (BDLC)	8
$00F0 - $00F7	Serial Peripheral Interface (SPI1)	8
$00F8 - $00FF	Serial Peripheral Interface (SPI2)	8
$0100- $010F	Flash Control Register	16
$0110 - $011B	EEPROM Control Register	12
$011C - $011F	Reserved	4
$0120 - $013F	Analog to Digital Converter 10-bit 8 channels (ATD1)	32
$0140 - $017F	Motorola Scalable Can (CAN0)	64
$0180 - $01BF	Motorola Scalable Can (CAN1)	64
$01C0 - $01FF	Motorola Scalable Can (CAN2)	64
$0200 - $023F	Motorola Scalable Can (CAN3)	64
$0240 - $027F	Port Integration Module (PIM)	64
$0280 - $02BF	Motorola Scalable Can (CAN4)	64
$02C0 - $03FF	Reserved	320
$0000 - $0FFF	EEPROM array	4096
$1000 - $3FFF	RAM array	12288
$4000 - $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 - $BFFF	Flash EEPROM Page Window	16384

Table 1-1 Device Memory Map

Address	Module	Size (Bytes)
$C000 - $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 - $FFFF	16384

Figure 1-2 MC9S12DP256B Memory Map



* Assuming that a '0' was driven onto port K bit 7 during MCU is reset into normal expanded wide or narrow mode.

1.6 Detailed Register Map

The following tables show the detailed register map of the MC9S12DP256B.

$0000 - $000F MEBI map 1 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	PORTA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0001	PORTB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0002	DDRA	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0003	DDRB	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0008	PORTE	Read:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		Write:								
$0009	DDRE	Read:	Bit 7	6	5	4	3	Bit 2	0	0
		Write:								
$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
$000B	MODE	Read:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		Write:								
$000C	PUCR	Read:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		Write:								
$000D	RDRIV	Read:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		Write:								
$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0010 - $0014 MMC map 1 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0010	INITRM	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		Write:								
$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								