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**MC9S12E128**  
**MC9S12E64**  
**MC9S12E32**  
Data Sheet

*HCS12*  
*Microcontrollers*

MC9S12E128V1  
Rev. 1.07  
10/2005

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# MC9S12E128 Data Sheet

**covers**

**MC9S12E64 & MC9S12E32**

MC9S12E128V1  
Rev. 1.07  
10/2005

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## Appendix C Ordering Information



# Chapter 1

## MC9S12E128 Device Overview (MC9S12E128DGV1)

### 1.1 Introduction

The MC9S12E128 is a 112/80/64 pin low cost general purpose MCU comprised of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), up to 128K bytes of Flash EEPROM, up to 8K bytes of RAM, three asynchronous serial communications interface modules (SCI), a serial peripheral interface (SPI), an Inter-IC Bus (IIC), three 4-channel 16-bit timer modules (TIM), a 6-channel 15-bit Pulse Modulator with Fault protection module (PMF), a 6-channel 8-bit Pulse Width Modulator (PWM), a 16-channel 10-bit analog-to-digital converter (ADC), and two 1-channel 8-bit digital-to-analog converters (DAC). The MC9S12E128 has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available on each module, 16 dedicated I/O port bits are available with Wake-Up capability from STOP or WAIT mode. Furthermore, an on chip bandgap based voltage regulator (VREG) generates the internal digital supply voltage of 2.5V (VDD) from a 3.135V to 5.5V external supply range.

#### 1.1.1 Features

- 16-bit HCS12 CORE
  - HCS12 CPU
    - i. Upward compatible with M68HC11 instruction set
    - ii. Interrupt stacking and programmer's model identical to M68HC11
    - iii. Instruction queue
    - iv. Enhanced indexed addressing
  - Module Mapping Control (MMC)
  - Interrupt control (INT)
  - Background Debug Module (BDM)
  - Debugger (DBG12) including breakpoints and change-of-flow trace buffer
  - Multiplexed External Bus Interface (MEBI)
- Wake-Up interrupt inputs
  - Up to 16 port bits available for wake up interrupt function with digital filtering
- Memory Options
  - 32K, 64K or 128K Byte Flash EEPROM
  - 2K, 4K or 8K Byte RAM

- Two 1-channel Digital-to-Analog Converters (DAC)
  - 8-bit resolution
- Analog-to-Digital Converter (ADC)
  - 16-channel module with 10-bit resolution
  - External conversion trigger capability
- Three 4-channel Timers (TIM)
  - Programmable input capture or output compare channels
  - Simple PWM mode
  - Counter modulo reset
  - External event counting
  - Gated time accumulation
- 6 PWM channels (PWM)
  - Programmable period and duty cycle
  - 8-bit 6-channel or 16-bit 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- 6-channel Pulse width Modulator with Fault protection (PMF)
  - Three independent 15-bit counters with synchronous mode
  - Complementary channel operation
  - Edge and center aligned PWM signals
  - Programmable dead time insertion
  - Integral reload rates from 1 to 16
  - Four fault protection shut down input pins
  - Three current sense input pins
- Serial interfaces
  - Three asynchronous serial communication interfaces (SCI)
  - Synchronous serial peripheral interface (SPI)
  - Inter-IC Bus (IIC)
- Clock and Reset Generator (CRG)
  - Windowed COP watchdog
  - Real Time interrupt
  - Clock Monitor
  - Pierce or low current Colpitts oscillator
  - Phase-locked loop clock frequency multiplier
  - Self Clock mode in absence of external clock
  - Low power 0.5 to 16Mhz crystal oscillator reference clock

- Operating frequency
  - 50MHz equivalent to 25MHz Bus Speed
- Internal 2.5V Regulator
  - Input voltage range from 3.135V to 5.5V
  - Low power mode capability
  - Includes low voltage reset (LVR) circuitry
  - Includes low voltage interrupt (LVI) circuitry
- 112-Pin LQFP or 80-Pin QFP or 64-Pin QFN package
  - Up to 90 I/O lines with 5V input and drive capability (112 pin package)
  - Up to two dedicated 5V input only lines (IRQ and XIRQ)
  - Sixteen 3.3V/5V A/D converter inputs
- Development Support.
  - Single-wire background debug™ mode
  - On-chip hardware breakpoints
  - Enhanced debug features

## 1.1.2 Modes of Operation

User modes (**Expanded modes are only available in the 112-pin package version**)

- Normal modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Freescale use only**)
  - Special Peripheral Mode (**Freescale use only**)
- Low power modes
  - Stop Mode
  - Pseudo Stop Mode
  - Wait Mode



### 1.1.3 Block Diagram

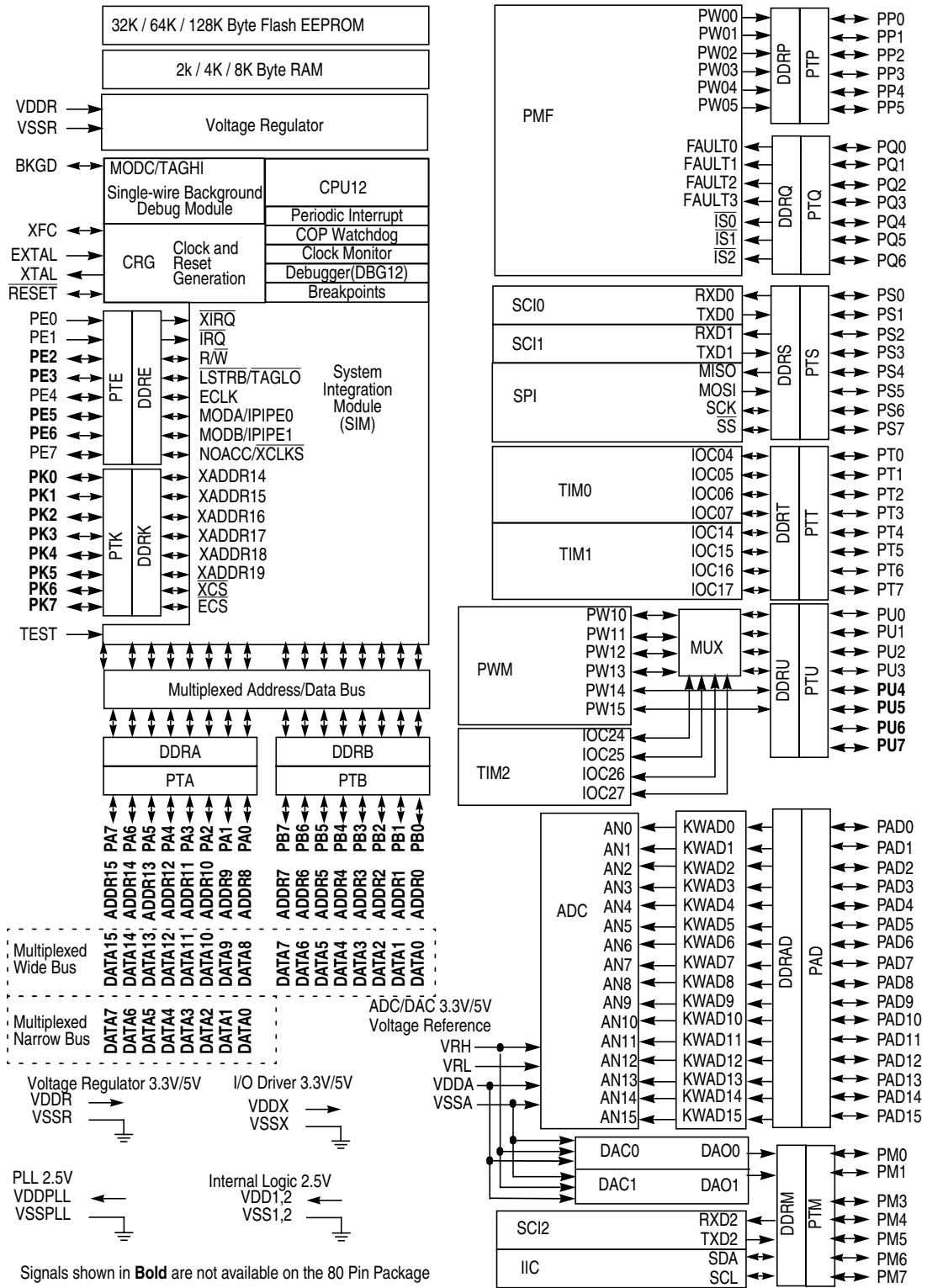


Figure 1-1. MC9S12E128 Block Diagram

## 1.2 Device Memory Map

Table 1-1 shows the device register map of the MC9S12E128 after reset. Figure 1-2, Figure 1-3 and Figure 1-4 illustrate the device memory map with Flash and RAM.

**Table 1-1. Device Register Map Overview**

Address	Module	Size
0x0000–0x0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
0x0018	Reserved	1
0x0019	Voltage Regulator (VREG)	1
0x001A–0x001B	Device ID register (PARTID)	2
0x001C–0x001F	CORE (MEMSIZ, IRQ, HPRI0)	4
0x0020–0x002F	CORE (DBG)	16
0x0030–0x0033	CORE (PPAGE, Port K)	4
0x0034–0x003F	Clock and Reset Generator (PLL, RTI, COP)	12
0x0040–0x006F	Standard Timer 16-bit 4 channels (TIM0)	48
0x0070–0x007F	Reserved	16
0x0080–0x00AF	Analog to Digital Converter 10-bit 16 channels (ATD)	48
0x00B0–0x00C7	Reserved	24
0x00C8–0x00CF	Serial Communications Interface 0 (SCI0)	8
0x00D0–0x00D7	Serial Communications Interface 1 (SCI1)	8
0x00D8–0x00DF	Serial Peripheral Interface (SPI)	8
0x00E0–0x00E7	Inter IC Bus	8
0x00E8–0x00EF	Serial Communications Interface 2 (SCI2)	8
0x00F0–0x00F3	Digital to Analog Converter 8-bit 1-channel (DAC0)	4
0x00F4–0x00F7	Digital to Analog Converter 8-bit 1-channel (DAC1)	4
0x00F8–0x00FF	Reserved	8
0x0100–0x010F	Flash Control Register	16
0x0110–0x013F	Reserved	48
0x0140–0x016F	Standard Timer 16-bit 4 channels (TIM1)	48
0x0170–0x017F	Reserved	16
0x0180–0x01AF	Standard Timer 16-bit 4 channels (TIM2)	48
0x01B0–0x01DF	Reserved	48
0x01E0–0x01FF	Pulse Width Modulator 8-bit 6 channels (PWM)	32
0x0200–0x023F	Pulse Width Modulator with Fault 15-bit 6 channels (PMF)	64
0x0240–0x027F	Port Integration Module (PIM)	64
0x0280–0x03FF	Reserved	384