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MC9S12H256
Device User Guide
V01.20
Covers also MC9S12H128

Original Release Date: 29 SEP 2000
Revised: 28 JUL 2008

Freescale Semiconductor Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	07 MAR 2001	03 APR 2001		Initial version.
V01.01	10 MAI 2001	10 MAY 2001		- Minor formal corrections - Changed ATD coupling ratio to10^{-2} - Changed V_{DD5} to 4.5V
V01.02	14 MAY 2001	14 MAY 2001		- Removed 112-pin package references - Changed ATD Electrical Characteristics separate coupling ratio for positive and negative bulk current injection
V01.03	30 MAY 2001	30 MAY 2001		- Reinserted 112-pin package information.
V01.04	11 JUN 2001	11 JUN 2001		- Removed SRSv2 comment from preface - Corrected RESET pin to active low in table 2-1
V01.05	18 JUN 2001	18 JUN 2001		- Adapted style and wording to 9DP256 device user guide - Minor format and wording improvements - Added SRAM data retention disclaimer
V01.06	28 JUN 2001	28 JUN 2001		- Changed Oscillator Characteristics t_{CQOUT} max 2.5s and replaced Clock Monitor Time-out by Clock Monitor Failure Assert Frequency - Changed Self Clock Mode Frequency min 1MHz and max 5.5MHz - Changed I_{DDPS} (RTI and COP disabled) to 400µA - Corrected typo in Figure 2-1 pin 76: PK3 -> PK2
V01.07	12 JUL 2001	12 JUL 2001		- Added t_{EXTR} and t_{EXTF} to Oscillator Characteristics - Added typ value for t_{UPOSC} - Corrected t_{EXTL} and t_{EXTH} values - Updated thermal resistances as per Thermal Simulation Report, July 10, 2001
V01.08	16 JUL 2001	16 JUL 2001		- updated EEPROM size - added DC cutoff capacitor into layout proposals
V01.09	03 AUG 2001	03 AUG 2001		- minor updates
V01.10	29 AUG 2001	29 AUG 2001		- updated electrical spec

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.11	11 OCT 2001	11 OCT 2001		- Replaced references w.r.t. new family name HCS12. - Corrected XCLKS reference in CRG electrical spec.
V01.12	07 NOV 2001	07 NOV 2001		- added ‘powered by’ column in pin list table
V01.13	08 MAR 2002	08 MAR 2002		- new document numbering - removed document order number except from cover sheet - updated min VDD, VDDPLL - updated currents on V_{OH},V_{OL} for standard pins - updated C_{IN}, I_{DDS}, I_{REF}, C_{INS}, T_{EXTL}, T_{EXTH} - included missing lcd electrical spec - updated NVM spec
V01.14	16 DEC 2002	16 DEC 2002		- updated input leakage - updated slew rate spec on PU,PV, PW - updated supply currents - included 1K78X - added detailed register map
V01.15	31 MAR 2003	31 MAR 2003		- added K_1 max value - added chragepump current min/max values
V01.16	05 NOV 2003	05 NOV 2003		- corrected pinout problem in LQFP112 layout proposal
V01.17	04 AUG 2004	04 AUG 2004		- added MC9S12H128
V01.18	13 AUG 2004	13 AUG 2004		- added Internal Pull Resistor columns to signal properties table
V01.19	05 NOV 2004	05 NOV 2004		- changed SPI0 to SPI, ATD0 to ATD
V01.20	28 JUL 2008	28 JUL 2008		- changed PU,PV,PW rise/fall times in EPP package at cold.

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Preface

The Device User Guide provides information about the MC9S12H256 and MC9S12H128 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes the HCS12 Core User Guide and all the individual Block User Guides of the implemented modules. In an effort to reduce redundancy all module specific information is located only in the respective Block User Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-1** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-1 Document References

User Guide	Version	Document Order Number
HCS12 V1.5 Core User Guide	1.2	HCS12COREUG
CRG Block User Guide	V02	S12CRGV2/D
TIM_16B8C Block User Guide	V01	S12TIM16B8CV1/D
ATD_10B16C Block User Guide	V02	S12ATD10B16CV2/D
IIC Block User Guide	V02	S12IICV2/D
SCI Block User Guide	V02	S12SCIV2/D
SPI Block User Guide	V02	S12SPIV2/D
PWM_8B6C Block User Guide	V01	S12PWM8B6CV1/D
FTS256K Block User Guide	V02	S12FTS256KV2/D
EETS4K Block User Guide	V02	S12EETS4KV2/D
LCD_32F4B Block User Guide	V01	S12LCD32F4BV1/D
MSCAN Block User Guide	V02	S12MSCANV2/D
MC_10B12C Block User Guide	V02	S12MC10B12CV2/D
PIM_9H256 Block User Guide	V01	S12PIMH256V1/D
VREG Block User Guide	V01	S12VREGV1/D

Section 1 Introduction

1.1 Overview

The MC9S12H256 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 256K bytes of Flash EEPROM, 12K bytes of RAM, 4K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), a serial peripheral interface (SPI), an IIC-bus interface (IIC), an 8-channel 16-bit timer (TIM), a 16-channel, 10-bit analog-to-digital converter (ATD), a six-channel pulse width modulator (PWM), and two CAN 2.0 A, B software compatible modules (MSCAN).

The MC9S12H128 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 128K bytes of Flash EEPROM, 6K bytes of RAM, 2K bytes of EEPROM, one asynchronous serial communications interface (SCI), a serial peripheral interface (SPI), an IIC-bus interface (IIC), an 8-channel 16-bit timer (TIM), a 8-channel, 10-bit analog-to-digital converter (ATD), a two-channel pulse width modulator (PWM), and two CAN 2.0 A, B software compatible modules (MSCAN).

In addition, it features a 32x4 liquid crystal display (LCD) controller/driver and a motor pulse width modulator (MC) consisting of 24 high current outputs suited to drive up to 6 stepper motors. System resource mapping, clock generation, interrupt control, and bus interfacing are managed by the HCS12 Core.

The MC9S12H256 has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, 12 general purpose I/O pins are available with interrupt and wake-up capability from STOP or WAIT mode.

1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer's model identical to M68HC11
    iii. 20-bit ALU
    iv. Instruction queue
    v. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)

  - BDM (Background Debug Mode)
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- 8-bit and 4-bit ports with interrupt functionality
  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 128K, 256K Flash EEPROM
  - 2K, 4K byte EEPROM
  - 6K, 12K byte RAM
- Analog-to-Digital Converter
  - 8, 16 channels, 10-bit resolution
  - External conversion trigger capability
- Two 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 2, 6 PWM channels
  - Programmable period and duty cycle
  - 8-bit 2, 6-channel or 16-bit 1, 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Synchronous Serial Peripheral Interface (SPI)

  - Inter-Integrated Circuit interface (IIC)
- Liquid Crystal Display driver with variable input voltage
  - Configurable for up to 32 frontplanes and 4 backplanes or general purpose input or output
  - 5 modes of operation allow for different display sizes to meet application requirements
  - Unused frontplane and backplane pins can be used as general purpose I/O
- 16, 24 high current drivers suited for PWM motor control
  - Each PWM channel switchable between two drivers in an H-bridge configuration
  - Left, right and center aligned outputs
  - Support for sine and cosine drive
  - Dithering
  - Output slew rate control
- 144-Pin or 112-Pin LQFP package
  - I/O lines with 5V input and drive capability
  - 5V A/D converter inputs
  - Operation at 32MHz equivalent to 16MHz Bus Speed
  - Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Freescale Use Only**)
  - Special Peripheral Mode (**Freescale Use Only**)

Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 is a block diagram of the MC9S12H256 device.

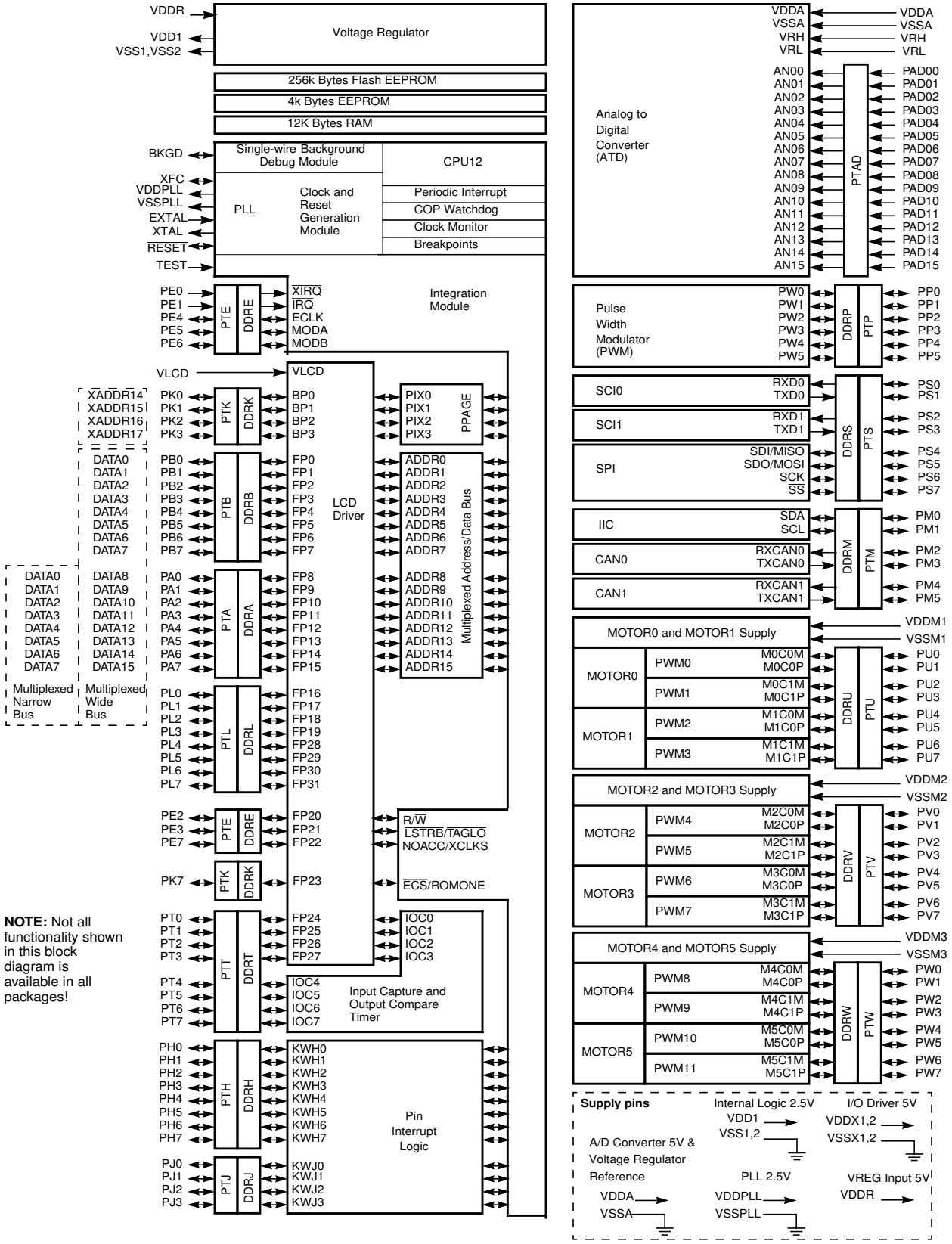

Figure 1-1 MC9S12H256 Block Diagram

Figure 1-2 is a block diagram of the MC9S12H128 device.

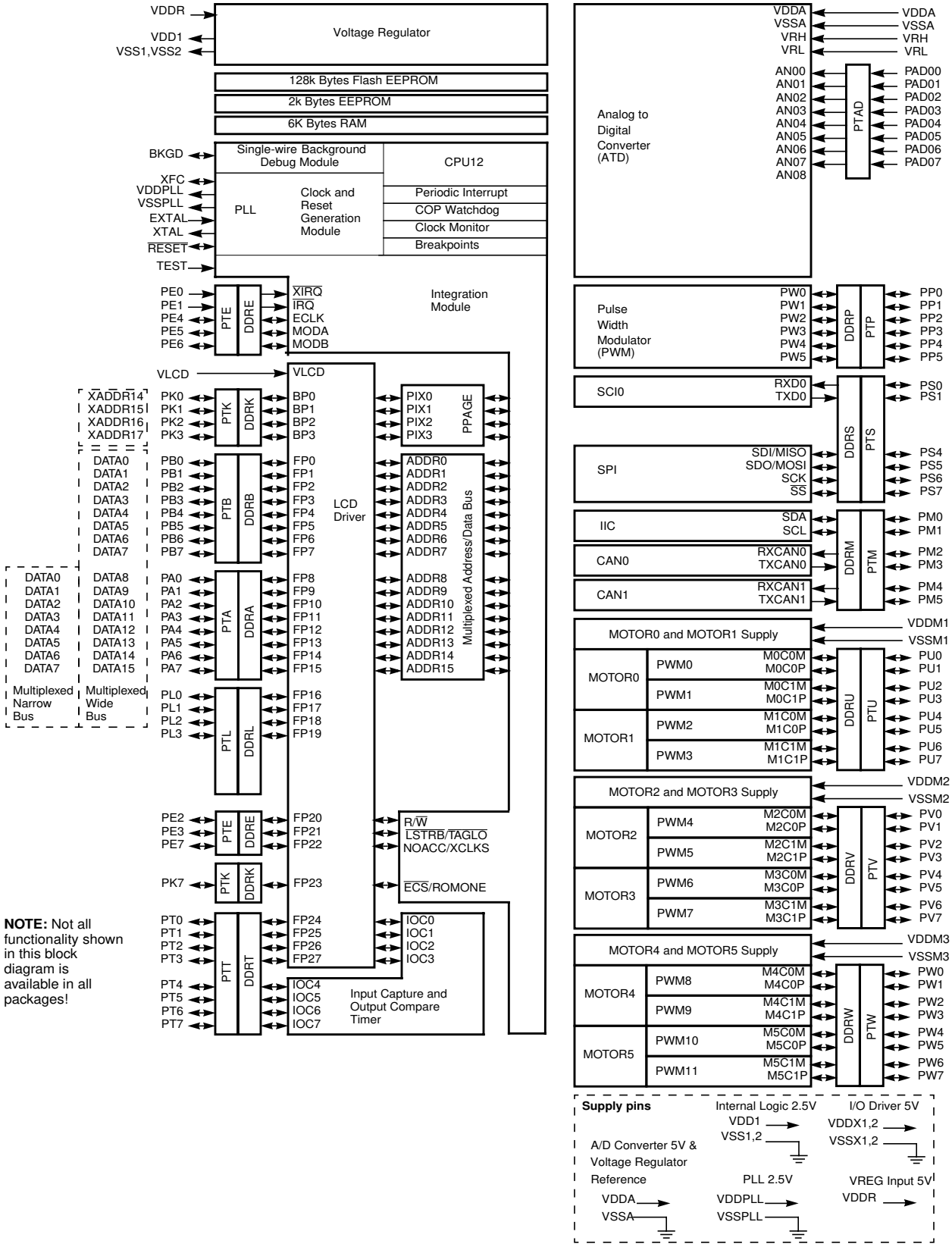

Figure 1-2 MC9S12H128 Block Diagram

1.5 Device Memory Map