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MC9S12HZ256

Data Sheet

Covers
MC9S12HZ128, MC9S12HZ64, MC9S12HN64
MC3S12HZ256, MC3S12HZ128, MC3S12HZ64,
MC3S12HN64, MC3S12HZ32 & MC3S12HN32

HCS12
Microcontrollers

MC9S12HZ256V2
Rev. 2.05
04/2008

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MC9S12HZ256 Data Sheet

MC9S12HZ256V2
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This document contains information for all constituent modules, with the exception of the S12 CPU. For S12 CPU information please refer to the CPU S12 Reference Manual.

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The following revision history table summarizes changes contained in this document.

Revision History

Date	Revision Level	Description
October 10, 2005	02.01	New Data Sheet
April 20, 2006	02.02	Corrected Table 4-1 Port U and Port V descriptions Added 80QFP to PCB layout guidelines Added derivative differences to appendix D Updated ordering information on appendix E
October 5, 2006	02.03	Added ROM to memory options Updated memory map figures and added tables for RAM mapping options Added ROM derivatives to appendix D Added ROM description to appendices (appendix E)
October 31, 2006	02.04	Added MC3S12HZ64 mask set Updated Table A-5 Thermal Package Characteristics Updated Table A-17 PLL Characteristics
April 25, 2008	02.05	Added MC3S12HZ64 Pinout. Figure 1-7 Corrected register map typo.

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MC9S12HZ256 Device Overview

Chapter 2
256 Kbyte Flash Module (FTS256K2V1)

Chapter 3
2 Kbyte EEPROM Module (EETS2KV1)

Chapter 4
Port Integration Module (PIM9HZ256V2)

Chapter 5
Clocks and Reset Generator (CRGV4)

Chapter 6
Oscillator (OSCV2)

Chapter 7
Analog-to-Digital Converter (ATD10B16CV4)

Chapter 8
Liquid Crystal Display (LCD32F4BV1)

Chapter 9
Motor Controller (MC10B8CV1)

Chapter 10
Stepper Stall Detector (SSDV1)

Chapter 11
Inter-Integrated Circuit (IICV2)

Chapter 12
Freescale's Scalable Controller Area Network (MSCANV2)

Chapter 13
Serial Communication Interface (SCIV4)

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Electrical Characteristics

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Chapter 1
MC9S12HZ256 Device Overview

1.1 Introduction

The MC9S12HZ256 microcontroller units (MCU) are 16-bit devices composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), up to 256K bytes of Flash EEPROM or ROM, up to 12K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), a serial peripheral interface (SPI), an IIC-bus interface (IIC), an 8-channel 16-bit timer (TIM), a 16-channel, 10-bit analog-to-digital converter (ATD), a six-channel pulse width modulator (PWM), and two CAN 2.0 A, B software compatible modules (MSCAN). In addition, they feature a 32x4 liquid crystal display (LCD) controller/driver, a pulse width modulator motor controller (MC) consisting of 16 high current outputs suited to drive up to four stepper motors, and four stepper stall detectors (SSD) to simultaneously calibrate the pointer position of each motor. System resource mapping, clock generation, interrupt control, and external bus interfacing are managed by the HCS12 Core. The MC9S12HZ256 have full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, 8 general-purpose I/O pins are available with interrupt and wake-up capability from stop or wait mode.

For information regarding the HCS12 CPU instruction set, please see the *HCS12 CPU Reference Manual*, Freescale document order number S12CPUV2.

1.1.1 Features

- HCS12 core
  - 16-bit HCS12 CPU
    - Upward compatible with M68HC11 instruction set
    - Interrupt stacking and programmer's model identical to M68HC11
    - 16-bit ALU
    - Instruction queue
    - Enhanced indexed addressing
  - MEBI (multiplexed external bus interface)
  - MMC (module mapping control)
  - INT (interrupt control)
  - DBG (debugger and breakpoints)
  - BDM (background debug mode)

- Memory
  - 256K, 128K, 64K, 32K Flash EEPROM or ROM
  - 2K, 1K byte EEPROM
  - 12K, 6K, 4K, 2K byte RAM
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- Analog-to-digital converter
  - 16 channels, 10-bit resolution
  - External conversion trigger capability
- Two 1-Mbps, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 6 PWM channels
  - Programmable period and duty cycle
  - 8-bit 6-channel or 16-bit 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Serial interfaces
  - Two asynchronous serial communications interfaces (SCI)
  - Synchronous serial peripheral interface (SPI)
  - Inter-integrated circuit interface (IIC)
- Liquid crystal display (LCD) driver with variable input voltage
  - Configurable for up to 32 frontplanes and 4 backplanes or general-purpose input or output
  - 5 modes of operation allow for different display sizes to meet application requirements
  - Unused frontplane and backplane pins can be used as general-purpose I/O
- PWM motor controller (MC) with 16 high current drivers
  - Each PWM channel switchable between two drivers in an H-bridge configuration
  - Left, right and center aligned outputs
  - Support for sine and cosine drive
  - Dithering
  - Output slew rate control

- Four stepper stall detectors (SSD)
  - Full step control during return to zero
  - Voltage detector and integrator / sigma delta converter circuit
  - 16-bit accumulator register
  - 16-bit modulus down counter
- 112-pin LQFP and 80-pin QFP packages
  - 85 I/O lines with 5-V input and drive capability
  - 5-V A/D converter inputs
  - 8 key wake up interrupts with digital filtering and programmable rising/falling edge trigger
- Operation at 50 MHz equivalent to 25-MHz bus speed
- Development support
  - Single-wire background debug™ mode (BDM)
  - Debugger and on-chip hardware breakpoints

1.1.2 Modes of Operation

User modes

- Normal and emulation operating modes
  - Normal single-chip mode
  - Normal expanded wide mode
  - Normal expanded narrow mode
  - Emulation expanded wide mode
  - Emulation expanded narrow mode
- Special operating mode
  - Special single-chip mode with active background debug mode

Low-power modes

- Stop mode
- Pseudo stop mode
- Wait mode

1.1.3 Block Diagram

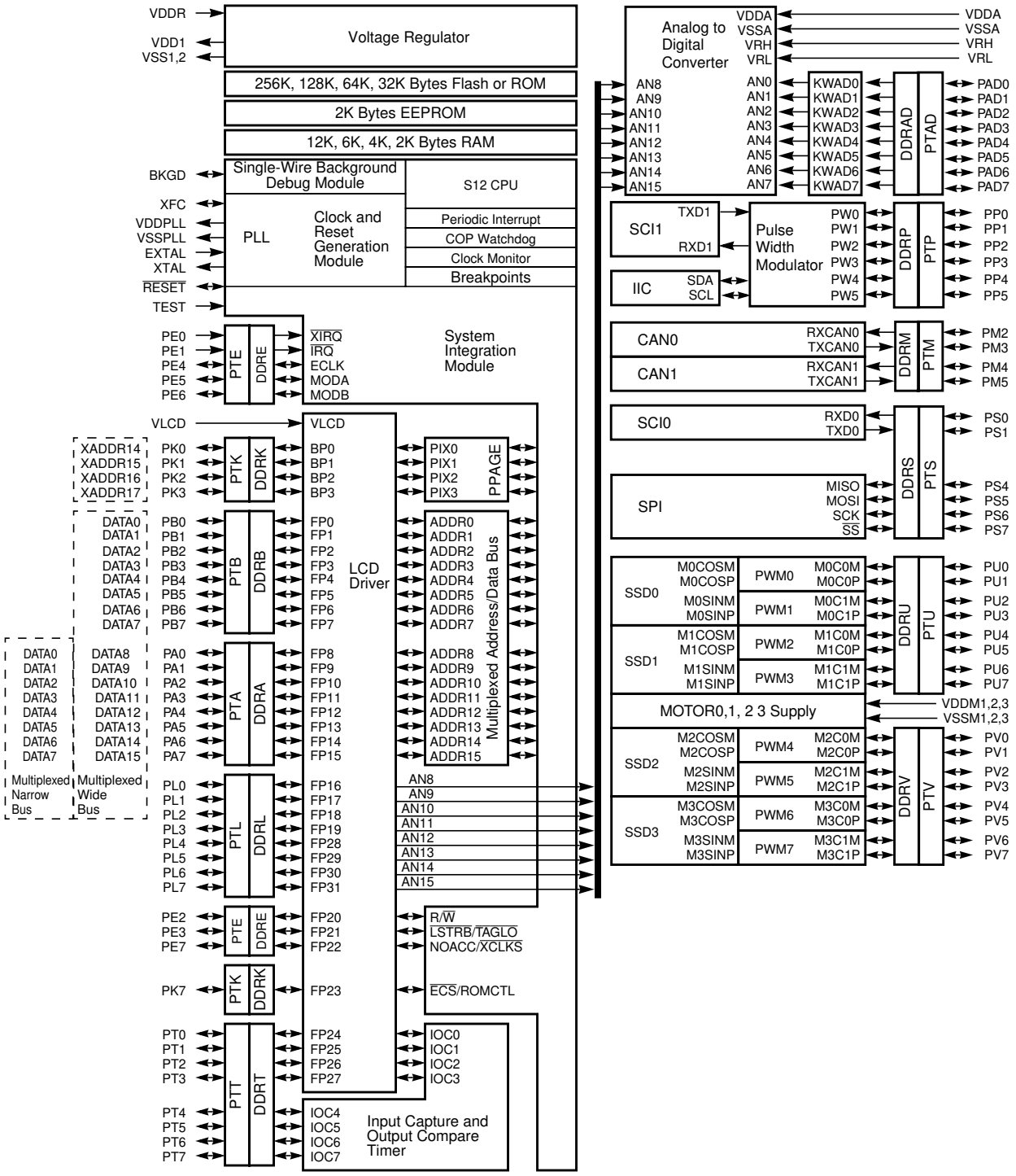

Figure 1-1. MC9S12HZ256 Block Diagram

1.2 Device Memory Map

Table 1-1 shows the device memory map for the MC9S12HZ256 out of reset.

Table 1-1. Device Register Map Overview

Address Offset	Module	Size (Bytes)
0x0000–0x0017	HCS12 Core (Ports A, B, E, Modes, Inits, Test)	24
0x0018–0x0019	Reserved	2
0x001A–0x001B	Device ID register (PARTID)	2
0x001C–0x001F	HCS12 Core (MEMSIZ, IRQ, HPRIO)	4
0x0020–0x0027	Reserved	8
0x0028–0x002F	HCS12 Core (Background Debug Mode)	8
0x0030–0x0033	HCS12 Core (PPAGE, Port K)	4
0x0034–0x003F	Clock and Reset Generator (PLL, RTI, COP)	12
0x0040–0x006F	Standard Timer Module 16-bit 8 channels (TIM)	48
0x0070–0x007F	Reserved	16
0x0080–0x00AF	Analog-to-Digital Converter 10-bit 16 channels (ATD)	48
0x00B0–0x00BF	Reserved	16
0x00C0–0x00C7	Inter Integrated Circuit (IIC)	8
0x00C8–0x00CF	Serial Communications Interface 0 (SCI0)	8
0x00D0–0x00D7	Serial Communications Interface 1 (SCI1)	8
0x00D8–0x00DF	Serial Peripheral Interface (SPI)	8
0x00E0–0x00FF	Pulse Width Modulator 8-bit 6 channels (PWM)	32
0x0100–0x010F	Flash control registers	16
0x0110–0x011B	EEPROM control registers	12
0x011C–0x011F	Reserved	4
0x0120–0x0137	Liquid Crystal Display Driver 32x4 (LCD)	24
0x0140–0x017F	Scalable Controller Area Network 0 (MSCAN0)	64
0x0180–0x01BF	Scalable Controller Area Network 1 (MSCAN1)	64
0x01C0–0x01FF	Motor Control Module (MC)	64
0x0200–0x027F	Port Integration Module (PIM)	128
0x0280–0x0287	Reserved	8
0x0288–0x028F	Stepper Stall Detector 0 (SSD0)	8
0x0290–0x0297	Stepper Stall Detector 1 (SSD1)	8
0x0298–0x029F	Stepper Stall Detector 2 (SSD2)	8
0x02A0–0x02A7	Stepper Stall Detector 3 (SSD3)	8
0x02A8–0x03FF	Reserved	344