



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



MC9S12KT256

Data Sheet

***HCS12
Microcontrollers***

MC9S12KT256
Rev. 1.16
06/2010

freescale.com



To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

A full list of family members and options is included in the appendices.

The following revision history table summarizes changes contained in this document.

This document contains information for all constituent modules, with the exception of the CPU. For CPU information please refer to **CPU12-1** in the **CPU12 & CPU12X Reference Manual**.

Revision History

Date	Revision Level	Description
June, 2010	1.16	Change SCI from V1 to V2, Chagne ATD from V2 to V3. Update TIM block guide. Update mask set Table 1-7 Add S12FTS256K2ECC_V1 for the xL33V mask set

Chapter 1	MC9S12KT256 Device Overview (MC9S12KT256V1)	17
Chapter 2	256 Kbyte ECC Flash Module (S12FTS256K2ECCV1)	73
Chapter 3	256 Kbyte ECC Flash Module (S12FTS256K2ECCV2)	117
Chapter 4	4 Kbyte EEPROM Module (S12EETS4KV2)	161
Chapter 5	Port Integration Module (PIM9KT256V1)	181
Chapter 6	Clocks and Reset Generator (CRGV4)	221
Chapter 7	Pierce Oscillator (S12OSCLCPV1)	257
Chapter 8	Analog-to-Digital Converter (S12ATD10B8CV3)	263
Chapter 9	Inter-Integrated Circuit (IICV2)	291
Chapter 10	Freescale’s Scalable Controller Area Network (S12MSCANV2)	315
Chapter 11	Serial Communications Interface (S12SCIV2)	371
Chapter 12	Serial Peripheral Interface (SPIV3)	401
Chapter 13	Pulse-Width Modulator (S12PWM8B8CV1)	423
Chapter 14	Timer Module (TIM16B8CV1)	455
Chapter 15	Dual Output Voltage Regulator (VREG3V3V2)	487
Chapter 16	Background Debug Module (BDMV4)	495
Chapter 17	Debug Module (DBGV1)	521
Chapter 18	Interrupt (INTV1)	555
Chapter 19	Multiplexed External Bus Interface (MEBIV3)	563
Chapter 20	Module Mapping Control (MMCV4)	593
Appendix A	Electrical Characteristics	613
Appendix B	Recommended PCB Layout	647
Appendix C	Package Information	650

Chapter 1

MC9S12KT256 Device Overview (MC9S12KT256V1)

1.1	Introduction	17
1.1.1	Features	17
1.1.2	Modes of Operation	19
1.1.3	MC9S12KT256 Block Diagram	21
1.2	Signal Description	22
1.2.1	Signal Properties Summary	24
1.2.2	Detailed Signal Descriptions	27
1.2.3	Power Supply Pins	36
1.3	Memory Map and Register Definition	38
1.3.1	Device Memory Map	38
1.3.2	Detailed Register Map	40
1.3.3	Part ID Assignments	64
1.4	System Clock Description	65
1.5	Modes of Operation	65
1.5.1	Chip Configuration Summary	65
1.5.2	Security	67
1.5.3	Low Power Modes	68
1.6	Resets and Interrupts	68
1.6.1	Vectors	68
1.6.2	Resets	71

Chapter 2

256 Kbyte ECC Flash Module (S12FTS256K2ECCV1)

2.1	Introduction	73
2.1.1	Glossary	74
2.1.2	Features	74
2.1.3	Modes of Operation	74
2.1.4	Block Diagram	74
2.2	External Signal Description	75
2.3	Memory Map and Register Definition	76
2.3.1	Module Memory Map	76
2.3.2	Register Descriptions	80
2.4	Functional Description	95
2.4.1	Flash Command Operations	95
2.5	Operating Modes	111
2.5.1	Wait Mode	111
2.5.2	Stop Mode	111
2.5.3	Background Debug Mode	111
2.6	Flash Module Security	112
2.6.1	Unsecuring the MCU using Backdoor Key Access	112
2.6.2	Unsecuring the Flash Module in Special Single-Chip Mode using BDM	113
2.7	Resets	113

2.7.1	Flash Reset Sequence	113
2.7.2	Reset While Flash Command Active	114
2.8	Interrupts	114
2.8.1	Description of Flash Interrupt Operation	114

Chapter 3

256 Kbyte ECC Flash Module (S12FTS256K2ECCV2)

3.1	Introduction	117
3.1.1	Glossary	118
3.1.2	Features	118
3.1.3	Modes of Operation	118
3.1.4	Block Diagram	118
3.2	External Signal Description	119
3.3	Memory Map and Register Definition	120
3.3.1	Module Memory Map	120
3.3.2	Register Descriptions	124
3.4	Functional Description	139
3.4.1	Flash Command Operations (NVM User Mode)	139
3.5	Operating Modes	155
3.5.1	Wait Mode	155
3.5.2	Stop Mode	155
3.5.3	Background Debug Mode	155
3.6	Flash Module Security	156
3.6.1	Unsecuring the MCU using Backdoor Key Access	156
3.6.2	Unsecuring the Flash Module in Special Single-Chip Mode using BDM	157
3.7	Resets	157
3.7.1	Flash Reset Sequence	157
3.7.2	Reset While Flash Command Active	158
3.8	Interrupts	158
3.8.1	Description of Flash Interrupt Operation	158

Chapter 4

4 Kbyte EEPROM Module (S12EETS4KV2)

4.1	Introduction	161
4.1.1	Glossary	161
4.1.2	Features	161
4.1.3	Modes of Operation	162
4.1.4	Block Diagram	162
4.2	External Signal Description	162
4.3	Memory Map and Register Definition	162
4.3.1	Module Memory Map	162
4.3.2	Register Descriptions	165
4.4	Functional Description	173
4.4.1	Program and Erase Operation	173

4.5	Operating Modes	179
4.5.1	Wait Mode	179
4.5.2	Stop Mode	179
4.5.3	Background Debug Mode	180
4.6	Resets	180
4.7	Interrupts	180

Chapter 5 Port Integration Module (PIM9KT256V1)

5.1	Introduction	181
5.1.1	Features	181
5.1.2	Block Diagram	182
5.2	External Signal Description	183
5.2.1	Signal Properties	183
5.3	Memory Map and Register Definition	187
5.3.1	Port T Registers	189
5.3.2	Port S Registers	192
5.3.3	Port M Registers	196
5.3.4	Port P Registers	202
5.3.5	Port H Registers	207
5.3.6	Port J Registers	211
5.4	Functional Description	215
5.4.1	I/O Register	215
5.4.2	Input Register	215
5.4.3	Data Direction Register	216
5.4.4	Reduced Drive Register	216
5.4.5	Pull Device Enable Register	217
5.4.6	Polarity Select Register	217
5.4.7	Pin Configuration Summary	217
5.5	Resets	218
5.5.1	Reset Initialization	218
5.6	Interrupts	218
5.6.1	General	218
5.6.2	Interrupt Sources	220
5.6.3	Operation in Stop Mode	220

Chapter 6 Clocks and Reset Generator (CRGV4) Block Description

6.1	Introduction	221
6.1.1	Features	221
6.1.2	Modes of Operation	222
6.1.3	Block Diagram	222
6.2	External Signal Description	223
6.2.1	V_{DDPLL} , V_{SSPLL} — PLL Operating Voltage, PLL Ground	223

6.2.2	XFC — PLL Loop Filter Pin	223
6.2.3	$\overline{\text{RESET}}$ — Reset Pin	224
6.3	Memory Map and Register Definition	224
6.3.1	Module Memory Map	224
6.3.2	Register Descriptions	225
6.4	Functional Description	236
6.4.1	Phase Locked Loop (PLL)	236
6.4.2	System Clocks Generator	239
6.4.3	Clock Monitor (CM)	240
6.4.4	Clock Quality Checker	240
6.4.5	Computer Operating Properly Watchdog (COP)	242
6.4.6	Real-Time Interrupt (RTI)	243
6.4.7	Modes of Operation	243
6.4.8	Low-Power Operation in Run Mode	244
6.4.9	Low-Power Operation in Wait Mode	244
6.4.10	Low-Power Operation in Stop Mode	248
6.5	Resets	252
6.5.1	Clock Monitor Reset	254
6.5.2	Computer Operating Properly Watchdog (COP) Reset	254
6.5.3	Power-On Reset, Low Voltage Reset	255
6.6	Interrupts	256
6.6.1	Real-Time Interrupt	256
6.6.2	PLL Lock Interrupt	256
6.6.3	Self-Clock Mode Interrupt	256

Chapter 7

Pierce Oscillator (S12OSCLCPV1)

7.1	Introduction	257
7.1.1	Features	257
7.1.2	Modes of Operation	257
7.1.3	Block Diagram	258
7.2	External Signal Description	258
7.2.1	V_{DDPLL} and V_{SSPLL} — Operating and Ground Voltage Pins	258
7.2.2	EXTAL and XTAL — Input and Output Pins	258
7.2.3	XCLKS — Input Signal	260
7.3	Memory Map and Register Definition	260
7.4	Functional Description	260
7.4.1	Gain Control	260
7.4.2	Clock Monitor	260
7.4.3	Wait Mode Operation	261
7.4.4	Stop Mode Operation	261

Chapter 8

Analog-to-Digital Converter (S12ATD10B8CV3)

8.1	Introduction	263
	8.1.1 Features	263
	8.1.2 Modes of Operation	263
	8.1.3 Block Diagram	264
8.2	External Signal Description	264
	8.2.1 AN _x (x = 7, 6, 5, 4, 3, 2, 1, 0) — Analog Input Pin	264
	8.2.2 ETRIG3, ETRIG2, ETRIG1, and ETRIG0 — External Trigger Pins	264
	8.2.3 V _{RH} and V _{RL} — High and Low Reference Voltage Pins	264
	8.2.4 V _{DDA} and V _{SSA} — Power Supply Pins	264
8.3	Memory Map and Register Definition	266
	8.3.1 Module Memory Map	266
	8.3.2 Register Descriptions	266
8.4	Functional Description	285
	8.4.1 Analog Sub-Block	285
	8.4.2 Digital Sub-Block	286
8.5	Initialization/Application Information	288
	8.5.1 Setting up and starting an A/D conversion	288
	8.5.2 Aborting an A/D conversion	289
8.6	Resets	289
8.7	Interrupts	289

Chapter 9

Inter-Integrated Circuit (IICV2) Block Description

9.1	Introduction	291
	9.1.1 Features	291
	9.1.2 Modes of Operation	293
	9.1.3 Block Diagram	293
9.2	External Signal Description	294
	9.2.1 IIC_SCL — Serial Clock Line Pin	294
	9.2.2 IIC_SDA — Serial Data Line Pin	294
9.3	Memory Map and Register Definition	294
	9.3.1 Module Memory Map	294
	9.3.2 Register Descriptions	295
9.4	Functional Description	306
	9.4.1 I-Bus Protocol	306
	9.4.2 Operation in Run Mode	310
	9.4.3 Operation in Wait Mode	310
	9.4.4 Operation in Stop Mode	310
9.5	Resets	310
9.6	Interrupts	310
9.7	Initialization/Application Information	311
	9.7.1 IIC Programming Examples	311

Chapter 10

Freescale's Scalable Controller Area Network (S12MSCANV2)

10.1	Introduction	315
10.1.1	Glossary	315
10.1.2	Block Diagram	316
10.1.3	Features	316
10.1.4	Modes of Operation	317
10.2	External Signal Description	317
10.2.1	RXCAN — CAN Receiver Input Pin	317
10.2.2	TXCAN — CAN Transmitter Output Pin	317
10.2.3	CAN System	317
10.3	Memory Map and Register Definition	318
10.3.1	Module Memory Map	318
10.3.2	Register Descriptions	320
10.3.3	Programmer's Model of Message Storage	342
10.4	Functional Description	351
10.4.1	General	351
10.4.2	Message Storage	352
10.4.3	Identifier Acceptance Filter	355
10.4.4	Modes of Operation	361
10.4.5	Low-Power Options	362
10.4.6	Reset Initialization	367
10.4.7	Interrupts	367
10.5	Initialization/Application Information	369
10.5.1	MSCAN initialization	369

Chapter 11

Serial Communications Interface (S12SCIV2)

Block Description

11.1	Introduction	371
11.1.1	Glossary	371
11.1.2	Features	372
11.1.3	Modes of Operation	372
11.1.4	Block Diagram	373
11.2	External Signal Description	374
11.2.1	TXD-SCI Transmit Pin	374
11.2.2	RXD-SCI Receive Pin	374
11.3	Memory Map and Registers	375
11.3.1	Module Memory Map	375
11.3.2	Register Descriptions	375
11.4	Functional Description	383
11.4.1	Data Format	384
11.4.2	Baud Rate Generation	385
11.4.3	Transmitter	386

11.4.4 Receiver	389
11.4.5 Single-Wire Operation	398
11.4.6 Loop Operation	398
11.5 Initialization Information	398
11.5.1 Reset Initialization	398
11.5.2 Interrupt Operation	399
11.5.3 Recovery from Wait Mode	400

Chapter 12

Serial Peripheral Interface (SPIV3) Block Description

12.1 Introduction	401
12.1.1 Features	401
12.1.2 Modes of Operation	401
12.1.3 Block Diagram	402
12.2 External Signal Description	402
12.2.1 MOSI — Master Out/Slave In Pin	402
12.2.2 MISO — Master In/Slave Out Pin	403
12.2.3 \overline{SS} — Slave Select Pin	403
12.2.4 SCK — Serial Clock Pin	403
12.3 Memory Map and Register Definition	403
12.3.1 Module Memory Map	403
12.3.2 Register Descriptions	404
12.4 Functional Description	411
12.4.1 Master Mode	412
12.4.2 Slave Mode	413
12.4.3 Transmission Formats	414
12.4.4 SPI Baud Rate Generation	417
12.4.5 Special Features	418
12.4.6 Error Conditions	419
12.4.7 Operation in Run Mode	420
12.4.8 Operation in Wait Mode	420
12.4.9 Operation in Stop Mode	420
12.5 Reset	421
12.6 Interrupts	421
12.6.1 MODF	421
12.6.2 SPIF	421
12.6.3 SPTEF	421

Chapter 13

Pulse-Width Modulator (S12PWM8B8CV1)

13.1 Introduction	423
13.1.1 Features	423
13.1.2 Modes of Operation	423
13.1.3 Block Diagram	424

13.2	External Signal Description	424
13.2.1	PWM7 — PWM Channel 7	424
13.2.2	PWM6 — PWM Channel 6	424
13.2.3	PWM5 — PWM Channel 5	425
13.2.4	PWM4 — PWM Channel 4	425
13.2.5	PWM3 — PWM Channel 3	425
13.2.6	PWM3 — PWM Channel 2	425
13.2.7	PWM3 — PWM Channel 1	425
13.2.8	PWM3 — PWM Channel 0	425
13.3	Memory Map and Register Definition	425
13.3.1	Module Memory Map	425
13.3.2	Register Descriptions	426
13.4	Functional Description	441
13.4.1	PWM Clock Select	441
13.4.2	PWM Channel Timers	444
13.5	Resets	452
13.6	Interrupts	453

Chapter 14

Timer Module (TIM16B8CV1) Block Description

14.1	Introduction	455
14.1.1	Features	455
14.1.2	Modes of Operation	455
14.1.3	Block Diagrams	456
14.2	External Signal Description	458
14.2.1	IOC7 — Input Capture and Output Compare Channel 7 Pin	458
14.2.2	IOC6 — Input Capture and Output Compare Channel 6 Pin	458
14.2.3	IOC5 — Input Capture and Output Compare Channel 5 Pin	458
14.2.4	IOC4 — Input Capture and Output Compare Channel 4 Pin	458
14.2.5	IOC3 — Input Capture and Output Compare Channel 3 Pin	458
14.2.6	IOC2 — Input Capture and Output Compare Channel 2 Pin	459
14.2.7	IOC1 — Input Capture and Output Compare Channel 1 Pin	459
14.2.8	IOC0 — Input Capture and Output Compare Channel 0 Pin	459
14.3	Memory Map and Register Definition	459
14.3.1	Module Memory Map	459
14.3.2	Register Descriptions	461
14.4	Functional Description	477
14.4.1	Prescaler	478
14.4.2	Input Capture	479
14.4.3	Output Compare	479
14.4.4	Pulse Accumulator	480
14.4.5	Event Counter Mode	480
14.4.6	Gated Time Accumulation Mode	481
14.5	Resets	481
14.6	Interrupts	481

14.6.1	Channel [7:0] Interrupt (C[7:0]F)	481
14.6.2	Pulse Accumulator Input Interrupt (PAOVI)	482
14.6.3	Pulse Accumulator Overflow Interrupt (PAOVF)	482
14.6.4	Timer Overflow Interrupt (TOF)	482

Chapter 15

Dual Output Voltage Regulator (VREG3V3V2)

Block Description

15.1	Introduction	487
15.1.1	Features	487
15.1.2	Modes of Operation	487
15.1.3	Block Diagram	488
15.2	External Signal Description	489
15.2.1	V_{DDR} — Regulator Power Input	489
15.2.2	V_{DDA} , V_{SSA} — Regulator Reference Supply	489
15.2.3	V_{DD} , V_{SS} — Regulator Output1 (Core Logic)	490
15.2.4	V_{DDPLL} , V_{SSPLL} — Regulator Output2 (PLL)	490
15.2.5	V_{REGEN} — Optional Regulator Enable	490
15.3	Memory Map and Register Definition	490
15.3.1	Module Memory Map	490
15.3.2	Register Descriptions	491
15.4	Functional Description	491
15.4.1	REG — Regulator Core	492
15.4.2	Full-Performance Mode	492
15.4.3	Reduced-Power Mode	492
15.4.4	LVD — Low-Voltage Detect	492
15.4.5	POR — Power-On Reset	492
15.4.6	LVR — Low-Voltage Reset	492
15.4.7	CTRL — Regulator Control	492
15.5	Resets	493
15.5.1	Power-On Reset	493
15.5.2	Low-Voltage Reset	493
15.6	Interrupts	493
15.6.1	LVI — Low-Voltage Interrupt	493

Chapter 16

Background Debug Module (BDMV4) Block Description

16.1	Introduction	495
16.1.1	Features	495
16.1.2	Modes of Operation	496
16.2	External Signal Description	496
16.2.1	BKGD — Background Interface Pin	497
16.2.2	$\overline{\text{TAGHI}}$ — High Byte Instruction Tagging Pin	497
16.2.3	$\overline{\text{TAGLO}}$ — Low Byte Instruction Tagging Pin	497

16.3	Memory Map and Register Definition	498
16.3.1	Module Memory Map	498
16.3.2	Register Descriptions	499
16.4	Functional Description	504
16.4.1	Security	504
16.4.2	Enabling and Activating BDM	504
16.4.3	BDM Hardware Commands	505
16.4.4	Standard BDM Firmware Commands	506
16.4.5	BDM Command Structure	507
16.4.6	BDM Serial Interface	509
16.4.7	Serial Interface Hardware Handshake Protocol	512
16.4.8	Hardware Handshake Abort Procedure	514
16.4.9	SYNC — Request Timed Reference Pulse	517
16.4.10	Instruction Tracing	517
16.4.11	Instruction Tagging	518
16.4.12	Serial Communication Time-Out	518
16.4.13	Operation in Wait Mode	519
16.4.14	Operation in Stop Mode	519

Chapter 17

Debug Module (DBGV1) Block Description

17.1	Introduction	521
17.1.1	Features	521
17.1.2	Modes of Operation	523
17.1.3	Block Diagram	523
17.2	External Signal Description	525
17.3	Memory Map and Register Definition	526
17.3.1	Module Memory Map	526
17.3.2	Register Descriptions	526
17.4	Functional Description	542
17.4.1	DBG Operating in BKP Mode	542
17.4.2	DBG Operating in DBG Mode	544
17.4.3	Breakpoints	551
17.5	Resets	552
17.6	Interrupts	552

Chapter 18

Interrupt (INTV1) Block Description

18.1	Introduction	555
18.1.1	Features	556
18.1.2	Modes of Operation	556
18.2	External Signal Description	557
18.3	Memory Map and Register Definition	557
18.3.1	Module Memory Map	557

18.3.2 Register Descriptions	557
18.4 Functional Description	559
18.4.1 Low-Power Modes	560
18.5 Resets	560
18.6 Interrupts	560
18.6.1 Interrupt Registers	560
18.6.2 Highest Priority I-Bit Maskable Interrupt	560
18.6.3 Interrupt Priority Decoder	561
18.7 Exception Priority	561

Chapter 19

Multiplexed External Bus Interface (MEBIV3)

19.1 Introduction	563
19.1.1 Features	563
19.1.2 Modes of Operation	565
19.2 External Signal Description	565
19.3 Memory Map and Register Definition	567
19.3.1 Module Memory Map	568
19.3.2 Register Descriptions	568
19.4 Functional Description	585
19.4.1 Detecting Access Type from External Signals	585
19.4.2 Stretched Bus Cycles	586
19.4.3 Modes of Operation	586
19.4.4 Internal Visibility	591
19.4.5 Low-Power Options	591

Chapter 20

Module Mapping Control (MMCV4) Block Description

20.1 Introduction	593
20.1.1 Features	594
20.1.2 Modes of Operation	594
20.2 External Signal Description	594
20.3 Memory Map and Register Definition	594
20.3.1 Module Memory Map	594
20.3.2 Register Descriptions	596
20.4 Functional Description	606
20.4.1 Bus Control	606
20.4.2 Address Decoding	606
20.4.3 Memory Expansion	608

Appendix A

Electrical Characteristics

A.1 General	613
A.1.1 Parameter Classification	613

A.1.2	Power Supply	613
A.1.3	Pins	614
A.1.4	Current Injection	615
A.1.5	Absolute Maximum Ratings	615
A.1.6	ESD Protection and Latch-up Immunity	616
A.1.7	Operating Conditions	617
A.1.8	Power Dissipation and Thermal Characteristics	618
A.1.9	I/O Characteristics	620
A.1.10	Supply Currents	622
A.2	Voltage Regulator	624
A.3	Chip Power-up and LVI/LVR Graphical Explanation	625
A.4	Output Loads	626
A.4.1	Resistive Loads	626
A.4.2	Capacitive Loads	626
A.5	ATD Characteristics	627
A.5.1	ATD Operating Characteristics	627
A.5.2	Factors Influencing Accuracy	628
A.5.3	ATD Accuracy	629
A.6	NVM, Flash and EEPROM	632
A.6.1	NVM Timing	632
A.6.2	NVM Reliability	634
A.7	Reset, Oscillator and PLL	635
A.7.1	Startup	635
A.7.2	Oscillator	636
A.7.3	Phase Locked Loop	637
A.8	MSCAN	641
A.9	SPI	641
A.9.1	Master Mode	641
A.9.2	Slave Mode	643
A.10	External Bus Timing	644
A.10.1	General Muxed Bus Timing	644

Appendix B Recommended PCB Layout

Appendix C Package Information

C.1	112-Pin LQFP Package	651
C.2	80-Pin QFP Package	652

Chapter 1

MC9S12KT256 Device Overview (MC9S12KT256V1)

1.1 Introduction

The MC9S12KT256 is a 112/80 pin 16-bit Flash-based microcontroller family targeted for high reliability systems. The MC9S12KT256 has an increased performance in reliability over the life of the product due to a built-in Error Checking and Correction Code (ECC) in the Flash memory. The program and erase operations automatically generate six parity bits per word making ECC transparent to the user.

The MC9S12KT256 is comprised of standard on-chip peripherals including a 16-bit central processing unit (CPU12), 256K bytes of Flash EEPROM, 4K bytes of EEPROM, 12K bytes of RAM, two asynchronous serial communications interface (SCI), three serial peripheral interface (SPI), IIC-bus, an 8-channel IC/OC timer, two 8-channel 10-bit analog-to-digital converters (ADC), an 8-channel pulse-width modulator (PWM), three CAN 2.0 A, B software compatible modules, 29 discrete digital I/O channels (Port A, Port B, Port E and Port K), and 20 discrete digital I/O lines with interrupt and wakeup capability. The MC9S12KT256 has full 16-bit data paths throughout, however, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

1.1.1 Features

- HCS12 Core
 - 16-bit HCS12 CPU
 - Upward compatible with M68HC11 instruction set
 - Interrupt stacking and programmer’s model identical to M68HC11
 - Instruction queue
 - Enhanced indexed addressing
 - MEBI (Multiplexed External Bus Interface)
 - MMC (Memory Map and Interface)
 - INT (Interrupt Controller)
 - DBG (Debugger)
 - BDM (Background Debug Mode)
- Oscillator
 - 4MHz to 16MHz frequency range
 - Pierce with amplitude loop control
 - Clock monitor

- Clock and Reset Generator (CRG)
 - Phase-locked loop clock frequency multiplier
 - Self Clock mode in absence of external clock
 - COP watchdog
 - Real Time interrupt (RTI)
- Memory
 - 256K Byte Flash EEPROM
 - Internal program/erase voltage generation
 - Security and Block Protect bits
 - Hamming Error Correction Coding (ECC)
 - 4K Byte EEPROM
 - 12K Byte static RAM
 - Single-cycle misaligned word accesses without wait states
- Analog-to-Digital Converters (ADC)
 - Two 8-channel modules with 10-bit resolution
 - External conversion trigger capability
- 8-channel Timer (TIM)
 - Programmable input capture or output compare channels
 - Simple PWM mode
 - Counter Modulo Reset
 - External Event Counting
 - Gated Time Accumulation
- 8-channel Pulse Width Modulator (PWM)
 - Programmable period and duty cycle per channel
 - 8-bit 8-channel or 16-bit 4-channel
 - Edge and center aligned PWM signals
 - Emergency shutdown input
- Three 1M bit per second, CAN 2.0 A, B software compatible modules
 - Five receive and three transmit buffers
 - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
 - Four separate interrupt channels for Rx, Tx, error and wake-up
 - Low-pass filter wake-up function
 - Loop-back for self test operation
- Serial interfaces
 - Two asynchronous serial communication interface (SCI)
 - Three synchronous serial peripheral interface (SPI)
 - Inter-IC Bus (IIC)
- Internal 2.5V Regulator
 - Input voltage range from 3.15V to 5.5V

- Low power mode capability
- Low Voltage Reset (LVR) and Low Voltage Interrupt (LVI)
- 20 key wake up inputs
 - Rising or falling edge triggered interrupt capability
 - Digital filter to prevent short pulses from triggering interrupts
 - Programmable pull ups and pull downs
- Operating frequency for ambient temperatures (T_A -40°C to 125°C)
 - 50MHz equivalent to 25MHz Bus Speed
- 112-Pin LQFP or 80-Pin QFP package
 - I/O lines with 3.3V/5V input and drive capability
 - 3.3V/5V A/D converter inputs

1.1.2 Modes of Operation

- Normal modes
 - Normal Single-Chip Mode
 - Normal Expanded Wide Mode
 - Normal Expanded Narrow Mode
 - Emulation Expanded Wide Mode
 - Emulation Expanded Narrow Mode
- Special Operating Modes
 - Special Single-Chip Mode with active Background Debug Mode
 - Special Test Mode (Freescale use only)
 - Special Peripheral Mode (Freescale use only)
- Each of the above modes of operation can be configured for three Low power submodes
 - Stop Mode
 - Pseudo Stop Mode
 - Wait Mode
- Secure operation, preventing the unauthorized read and write of the memory contents.

Table 1-1 shows a feature overview of the MC9S12KT256 members.

Table 1-1. List of MC9S12KT256 members

Device	Temp Options ¹	Flash	RAM	EEPROM	Package	CAN	SCI	SPI	IIC	A/D ²	PWM ²	TIM ²	I/O ³
MC9S12KT256	C, V, M	256K	12K	4K	112 LQFP	3	2	3	1	16	8	8	91
MC9S12KG256	C, V, M	256K	12K	4K	112 LQFP	2	2	3	1	16	8	8	91
					80 QFP	2	2	3	1	8	7	8	59

¹ C: TA = 85°C, f = 25MHz. V: TA=105°C, f = 25MHz. M: TA= 125°C, f = 25MHz

² Number of channels

³ I/O is the sum of ports capable to act as digital input or output.

Figure 1-1 shows the part number coding based on the package and temperature options for the MC9S12KT256.

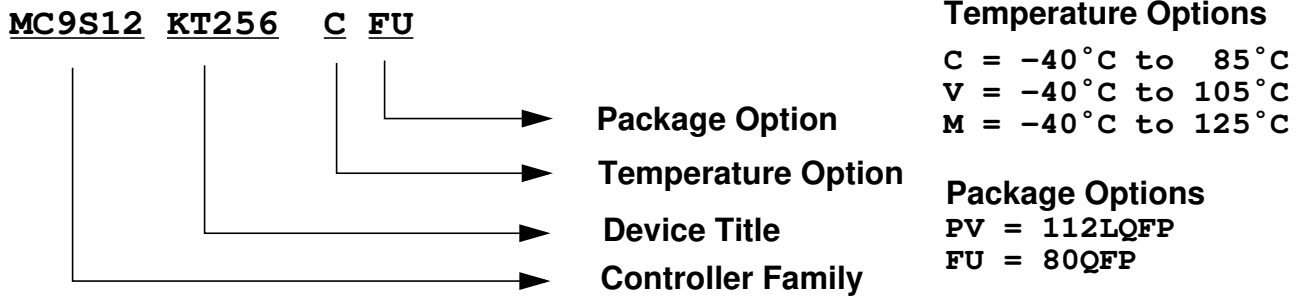
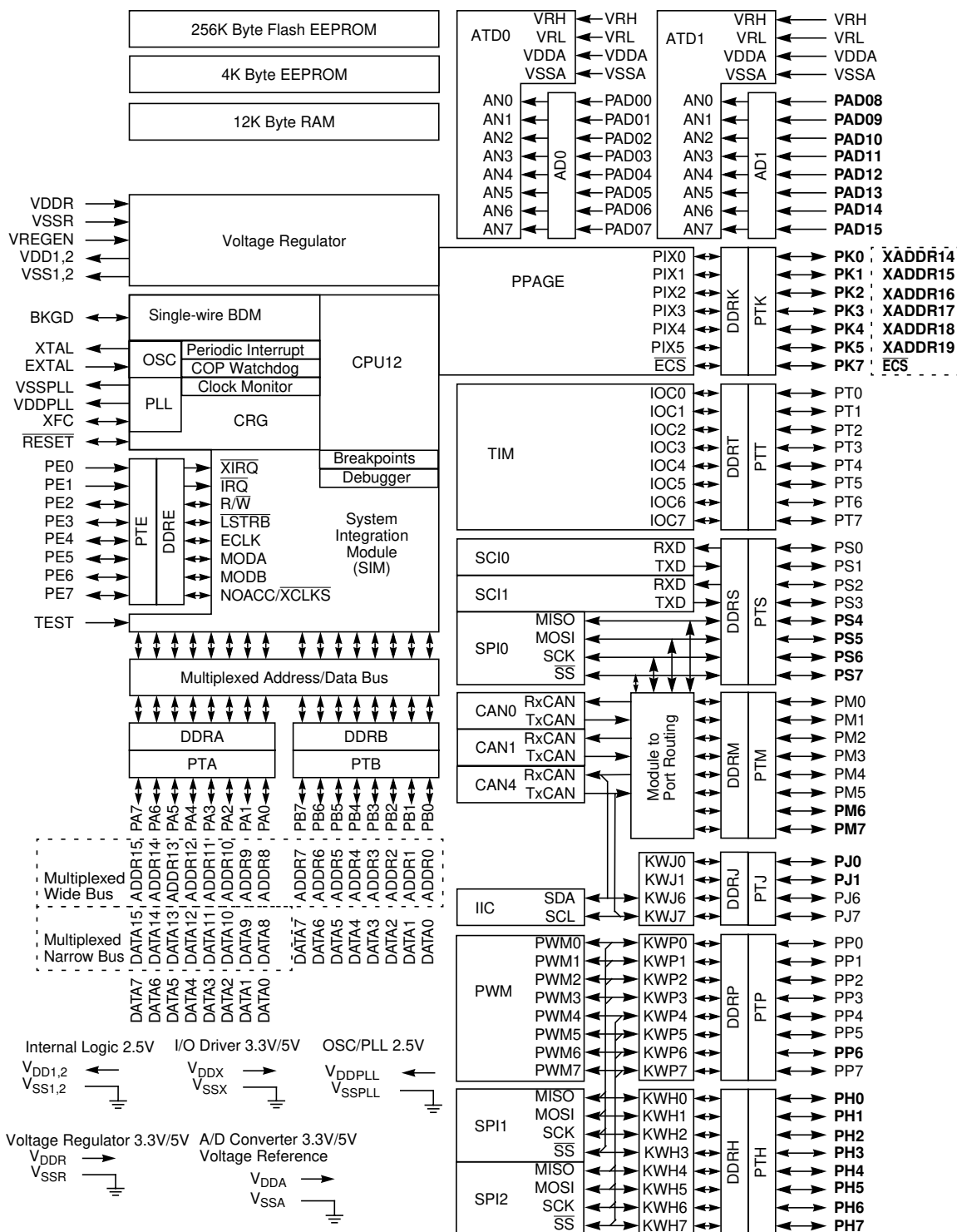


Figure 1-1. Order Part number Coding

1.1.3 MC9S12KT256 Block Diagram

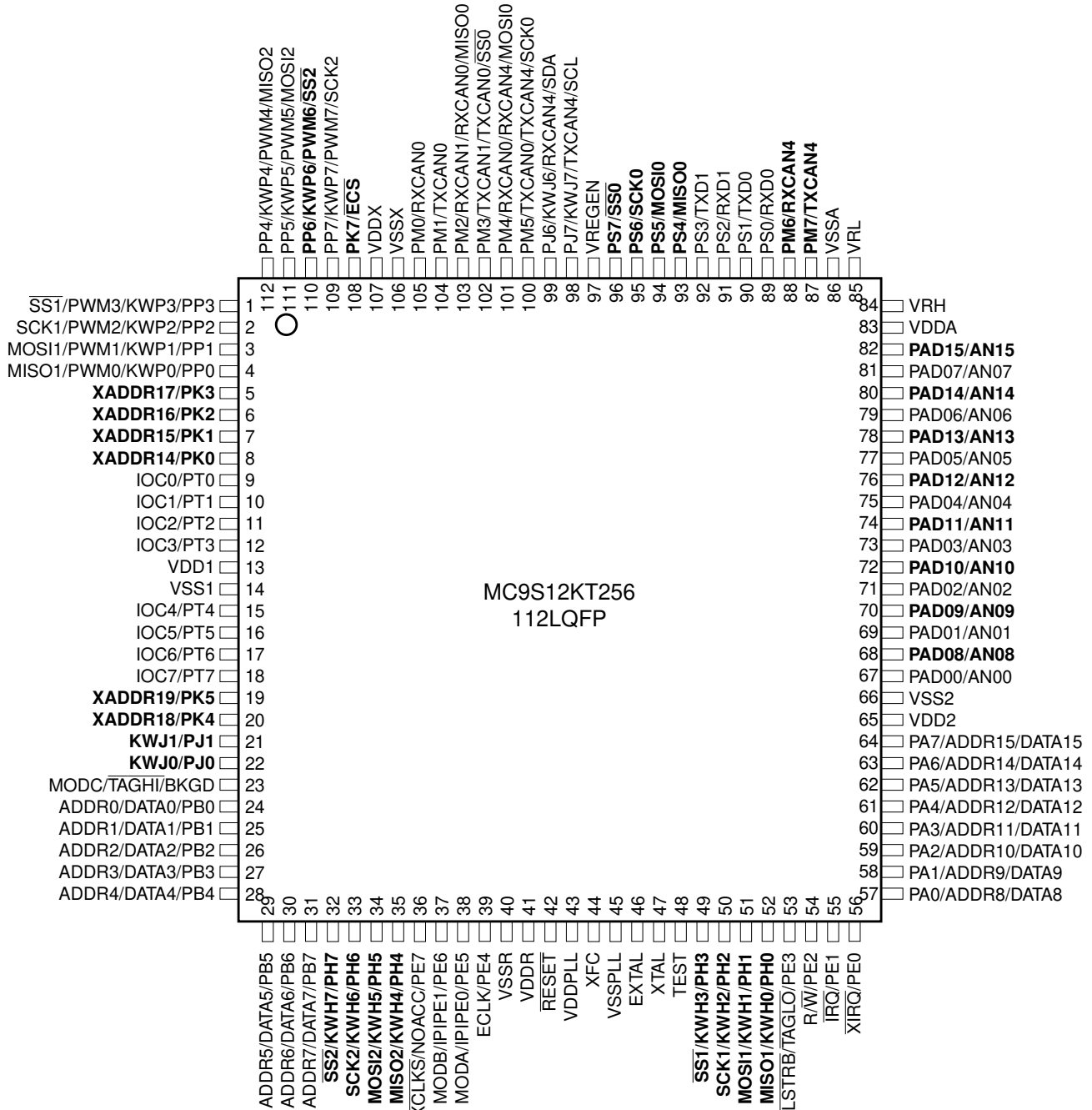


Signals shown in **Bold** are not available on the 80-Pin Package

Figure 1-2. MC9S12KT256 Block Diagram

1.2 Signal Description

The MC9S12KT256 is available in a 112-pin low profile quad flat pack (LQFP) and a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in Section 1.2.1, “Signal Properties Summary”. Figure 1-3 and Figure 1-4 show the pin assignments for different packages.



Signals shown in **Bold** are not available on the 80-pin package

Figure 1-3. Pin Assignments for 112 LQFP

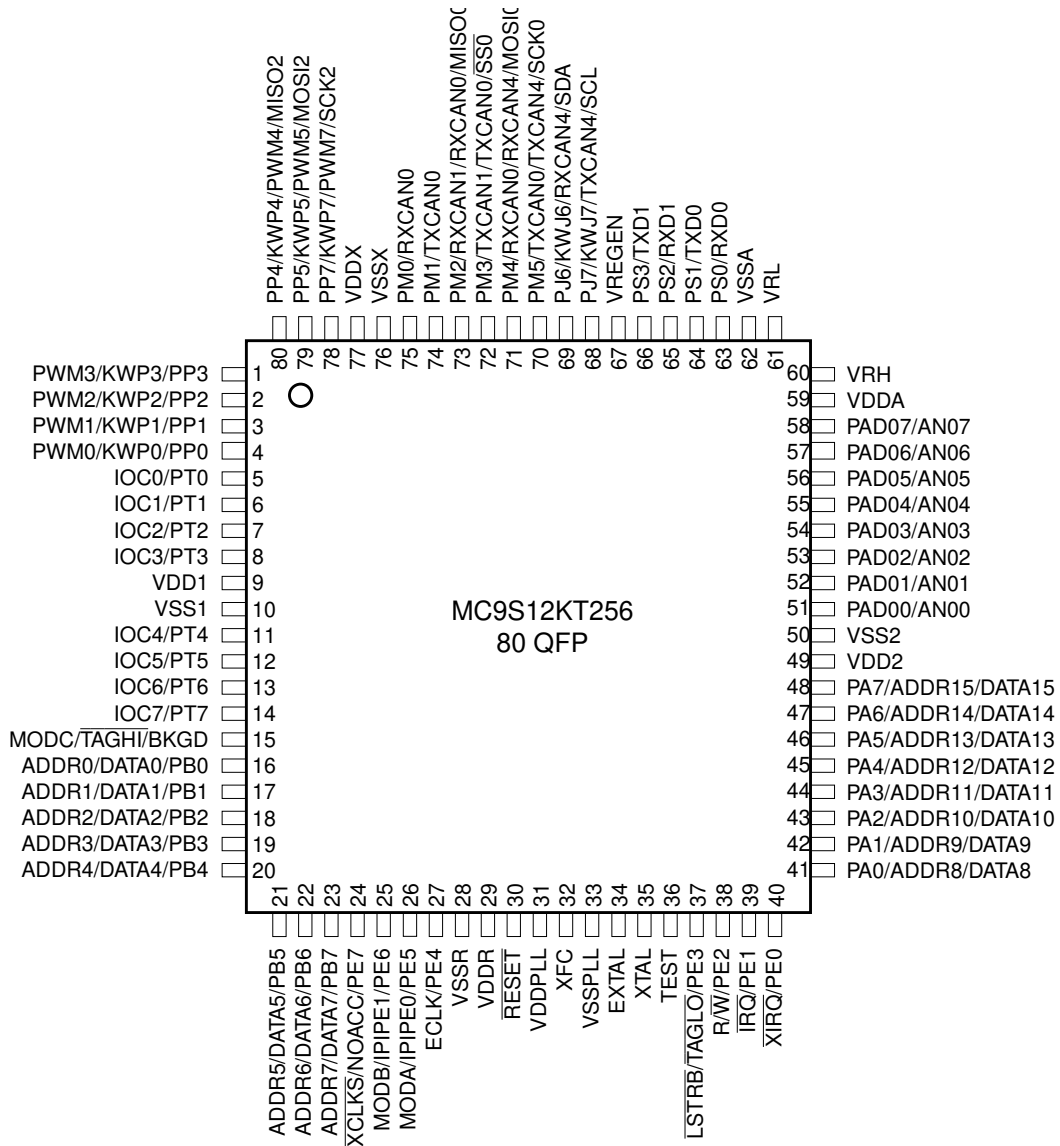


Figure 1-4. Pin Assignments for 80 QFP

1.2.1 Signal Properties Summary

Table 1-2 summarizes the pin functionality. Signals shown in **bold** are not available in the 80-pin package. Table 1-3 summarizes the power and ground pins.

Table 1-2. Signal Properties (Sheet 1 of 3)

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
EXTAL	—	—	—	VDDPLL	NA	NA	Oscillator Pins
XTAL	—	—	—	VDDPLL	NA	NA	
RESET	—	—	—	VDDR	None	None	External Reset
TEST	—	—	—	NA	NA	NA	Test Input
VREGEN	—	—	—	VDDX	NA	NA	Voltage Regulator Enable Input
XFC	—	—	—	VDDPLL	NA	NA	PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	VDDR	Always Up	Up	Background Debug, Tag High, Mode Input
PAD[15:8]	AN1[7:0]	—	—	VDDA	None	None	Port AD Input, Analog Inputs of ATD1
PAD[7:0]	AN0[7:0]	—	—	VDDA	None	None	Port AD Input, Analog Inputs of ATD0
PA[7:0]	ADDR[15:8]/ DATA[15:8]	—	—	VDDR	PUCR	Disabled	Port A I/O, Multiplexed Address/Data
PB[7:0]	ADDR[7:0]/ DATA[7:0]	—	—	VDDR	PUCR	Disabled	Port B I/O, Multiplexed Address/Data
PE7	NOACC	XCLKS	—	VDDR	PUCR	Up	Port E I/O, Access, Clock Select
PE6	IPIPE1	MODB	—	VDDR	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—	VDDR	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—	VDDR	PUCR	Up	Port E I/O, Bus Clock Output
PE3	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	—	VDDR	PUCR	Up	Port E I/O, Byte Strobe, Tag Low
PE2	R/W	—	—	VDDR	PUCR	Up	Port E I/O, R/W in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—	VDDR	PUCR	Up	Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—	VDDR	PUCR	Up	Port E Input, Non Maskable Interrupt
PH7	KWH7	SS2	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, $\overline{\text{SS}}$ of SPI2
PH6	KWH6	SCK2	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, SCK of SPI2
PH5	KWH5	MOSI2	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MOSI of SPI2

Table 1-2. Signal Properties (Sheet 2 of 3)

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
PH4	KWH4	MISO2	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MISO of SPI2
PH3	KWH3	$\overline{SS1}$	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, \overline{SS} of SPI1
PH2	KWH2	SCK1	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, SCK of SPI1
PH1	KWH1	MOSI1	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MOSI of SPI1
PH0	KWH0	MISO1	—	VDDR	PERH/ PPSH	Disabled	Port H I/O, Interrupt, MISO of SPI1
PJ7	KWJ7	TXCAN4	SCL	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, TX of CAN4, SCL of IIC
PJ6	KWJ6	RXCAN4	SDA	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupt, RX of CAN4, SDA of IIC
PJ[1:0]	KWJ[1:0]	—	—	VDDX	PERJ/ PPSJ	Up	Port J I/O, Interrupts
PK7	\overline{ECS}	ROMCTL	—	VDDX	PUCR	Up	Port K I/O, Emulation Chip Select, ROM On Enable
PK[5:0]	XADDR[19:14]	—	—	VDDX	PUCR	Up	Port K I/O, Extended Addresses
PM7	TXCAN4	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN4 TX
PM6	RXCAN4	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN4 RX
PM5	TXCAN0	TXCAN4	SCK0	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 TX, CAN4 TX, SPI0 SCK
PM4	RXCAN0	RXCAN4	MOSI0	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 RX, CAN4 RX, SPI0 MOSI
PM3	TXCAN1	TXCAN0	$\overline{SS0}$	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN1 TX, CAN0 TX, SPI0 \overline{SS}
PM2	RXCAN1	RXCAN0	MISO0	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN1 RX, CAN0 RX, SPI0 MISO
PM1	TXCAN0	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 TX
PM0	RXCAN0	—	—	VDDX	PERM/ PPSM	Disabled	Port M I/O, CAN0 RX
PP7	KWP7	PWM7	SCK2	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, PWM Channel 7, SCK of SPI2
PP6	KWP6	PWM6	$\overline{SS2}$	VDDX	PERP/ PPSP	Disabled	Port P I/O, Interrupt, PWM Channel 6, SPI2 \overline{SS}