Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MC9S12P128
Reference Manual

Covers also MC9S12P-Family
MC9S12P96
MC9S12P64
MC9S12P32

S12
Microcontrollers

MC9S12P128RMV1

Rev. 1.13

23 April 2010

freescale.com

freescale™
semiconductor

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

A full list of family members and options is included in the appendices.

The following revision history table summarizes changes contained in this document.

This document contains information for all constituent modules, with the exception of the CPU. For CPU information please refer to **CPU12-1** in the **CPU12 & CPU12X Reference Manual**.

Revision History

Date	Revision Level	Description
April 2008	1.07	PRELIMINARY
July 2008	1.08	Minor Corrections Added typ. I_{DD} values
December 2008	1.09	Completed Electricals Minor Corrections
March 2009	1.10	Final Electricals
June 2009	1.11	Corrected section 1.11.3.4 Memory Corrected 1.7.3.16 - 1.7.3.19 SPI pin description Removed reference to MMCCTL1 register from Table 13-5 Removed item 4b from Table A-6 and A-7 Changed Version ID in Table 1-5 from $FF to $00
October 2009	1.12	Added Register Summary Appendix D Updated FTMRC Blockguide . See Revision History Chapter 13 Updated CPMU Blockguide . See Revision History Chapter 7
April 2010	1.13	Updated S12PMMCV1 Blockguide. See Revision History Chapter 3 Updated S12CPMU Blockguide. See Revision History Chapter 7

Chapter 1Device Overview MC9S12P-Family

Chapter 2
Port Integration Module (S12PPIMV1)

Chapter 3
Memory Map Control (S12PMMCV1)

Chapter 4
Interrupt Module (S12SINTV1)

Chapter 5
Background Debug Module (S12SBDMV1)

Chapter 6
S12S Debug Module (S12SDBGV2)

Chapter 7
S12 Clock, Reset and Power Management Unit (S12CPMU)

Chapter 8
Freescale's Scalable Controller Area Network (S12MSCANV3)

Chapter 9
Analog-to-Digital Converter (ADC12B10C)

Chapter 10
Pulse-Width Modulator (PWM8B6CV1) Block Description

Chapter 11
Serial Communication Interface (S12SCIV5)

Chapter 12
Serial Peripheral Interface (S12SPIV5)

Chapter 13
128 KByte Flash Module (S12FTMRC128K1V1)

Chapter 14
Timer Module (TIM16B8CV2) Block Description

Appendix A
Electrical Characteristics

Appendix B
Ordering Information

Appendix C
Package Information

Appendix D
Detailed Register Address Map

Chapter 1 Device Overview MC9S12P-Family

1.1 Introduction

The MC9S12P family is an optimized, automotive, 16-bit microcontroller product line focused on low-cost, high-performance, and low pin-count. This family is intended to bridge between high-end 8-bit microcontrollers and high-performance 16-bit microcontrollers, such as the MC9S12XS family. The MC9S12P family is targeted at generic automotive applications requiring CAN or LIN/J2602 communication. Typical examples of these applications include body controllers, occupant detection, door modules, seat controllers, RKE receivers, smart actuators, lighting modules, and smart junction boxes.

The MC9S12P family uses many of the same features found on the MC9S12XS family, including error correction code (ECC) on flash memory, a separate data-flash module for diagnostic or data storage, a fast analog-to-digital converter (ATD) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance.

The MC9S12P family deliver all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of Freescale's existing 8-bit and 16-bit MCU families. Like the MC9S12XS family, the MC9S12P family run 16-bit wide accesses without wait states for all peripherals and memories. The MC9S12P family is available in 80-pin QFP, 64-pin LQFP, and 48-pin QFN package options and aims to maximize pin compatibility with the MC9S12XS family. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

1.2 Features

This section describes the key features of the MC9S12P family.

1.2.1 MC9S12P Family Comparison

Table 1 provides a summary of different members of the MC9S12P family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

Table 1. MC9S12P Family

Feature	MC9S12P32	MC9S12P64	MC9S12P96	MC9S12P128
CPU	CPU12-V1			
Flash memory (ECC)	32 Kbytes	64 Kbytes	96 Kbytes	128 Kbytes
Data flash (ECC)	4 Kbytes			
RAM	2 Kbytes	4 Kbytes	6 Kbytes	
MSCAN	1			
SCI	1			
SPI	1			
Timer	8 ch x 16-bit			
PWM	6 ch x 8-bit			
ADC	10 ch x 12-bit			
Frequency modulated PLL	Yes			
External oscillator (4 – 16 MHz Pierce with loop control)	Yes			
Internal 1 MHz RC oscillator	Yes			
Supply voltage	3.15 V – 5.5 V			
Execution speed	Static(1) – 32 MHz			
Package	80 QFP, 64 LQFP, 48 QFN			

1. P or D Flash erasing or programming requires a minimum bus frequency of 1MHz

1.2.2 Chip-Level Features

On-chip modules available within the family include the following features:

- S12 CPU core
- Up to 128 Kbyte on-chip flash with ECC
- 4 Kbyte data flash with ECC
- Up to 6 Kbyte on-chip SRAM
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 4–16 MHz amplitude controlled Pierce oscillator
- 1 MHz internal RC oscillator
- Timer module (TIM) supporting input/output channels that provide a range of 16-bit input capture, output compare, counter, and pulse accumulator functions

- Pulse width modulation (PWM) module with 6 x 8-bit channels
- 10-channel, 12-bit resolution successive approximation analog-to-digital converter (ATD)
- One serial peripheral interface (SPI) module
- One serial communication interface (SCI) module supporting LIN communications
- One multi-scalable controller area network (MSCAN) module (supporting CAN protocol 2.0A/B)
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- Autonomous periodic interrupt (API)

1.3 Module Features

The following sections provide more details of the modules implemented on the MC9S12P family.

1.3.1 S12 16-Bit Central Processor Unit (CPU)

S12 CPU is a high-speed 16-bit processing unit:

- Full 16-bit data paths supports efficient arithmetic operation and high-speed math execution
- Includes many single-byte instructions. This allows much more efficient use of ROM space.
- Extensive set of indexed addressing capabilities, including:
  - Using the stack pointer as an indexing register in all indexed operations
  - Using the program counter as an indexing register in all but auto increment/decrement mode
  - Accumulator offsets using A, B, or D accumulators
  - Automatic index predecrement, preincrement, postdecrement, and postincrement (by –8 to +8)

1.3.2 On-Chip Flash with ECC

On-chip flash memory on the MC9S12P features the following:

- Up to 128 Kbyte of program flash memory
  - 32 data bits plus 7 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 512 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads
  - Protection scheme to prevent accidental program or erase
- 4 Kbyte data flash space
  - 16 data bits plus 6 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 256 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads

1.3.3 On-Chip SRAM

- Up to 6 Kbytes of general-purpose RAM

1.3.4 Main External Oscillator (XOSC)

- Loop control Pierce oscillator using a 4 MHz to 16 MHz crystal
  - Current gain control on amplitude output
  - Signal with low harmonic distortion
  - Low power
  - Good noise immunity
  - Eliminates need for external current limiting resistor
  - Transconductance sized for optimum start-up margin for typical crystals

1.3.5 Internal RC Oscillator (IRC)

- Trimmable internal reference clock.
  - Frequency: 1 MHz
  - Trimmed accuracy over –40˚C to +125˚C ambient temperature range: ±1.5%

1.3.6 Internal Phase-Locked Loop (IPLL)

- Phase-locked-loop clock frequency multiplier
  - No external components required
  - Reference divider and multiplier allow large variety of clock rates
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
  - Reference clock sources:
    - External 4–16 MHz resonator/crystal (XOSC)
    - Internal 1 MHz RC oscillator (IRC)

1.3.7 System Integrity Support

- Power-on reset (POR)
- System reset generation
- Illegal address detection with reset
- Low-voltage detection with interrupt or reset
- Real time interrupt (RTI)
- Computer operating properly (COP) watchdog
  - Configurable as window COP for enhanced failure detection

  - Initialized out of reset using option bits located in flash memory
- Clock monitor supervising the correct function of the oscillator

1.3.8 Timer (TIM)

- 8 x 16-bit channels for input capture or output compare
- 16-bit free-running counter with 7-bit precision prescaler
- 1 x 16-bit pulse accumulator

1.3.9 Pulse Width Modulation Module (PWM)

- 6 channel x 8-bit or 3 channel x 16-bit pulse width modulator
  - Programmable period and duty cycle per channel
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies

1.3.10 Controller Area Network Module (MSCAN)

- 1 Mbit per second, CAN 2.0 A, B software compatible
  - Standard and extended data frames
  - 0–8 bytes data length
  - Programmable bit rate up to 1 Mbps
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization
- Flexible identifier acceptance filter programmable as:
  - 2 x 32-bit
  - 4 x 16-bit
  - 8 x 8-bit
- Wakeup with integrated low pass filter option
- Loop back for self test
- Listen-only mode to monitor CAN bus
- Bus-off recovery by software intervention or automatically
- 16-bit time stamp of transmitted/received messages

1.3.11 Serial Communication Interface Module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection

- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wakeup
- Break detect and transmit collision detect supporting LIN

1.3.12 Serial Peripheral Interface Module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.3.13 Analog-to-Digital Converter Module (ATD)

- 10-channel, 12-bit analog-to-digital converter
  - 3 us single conversion time
  - 8-/10-/12-bit resolution
  - Left or right justified result data
  - Internal oscillator for conversion in stop modes
  - Wakeup from low power modes on analog comparison > or <= match
  - Continuous conversion mode
  - Multiple channel scans
- Pins can also be used as digital I/O

1.3.14 On-Chip Voltage Regulator (VREG)

- Linear voltage regulator with bandgap reference
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR) circuit
- Low-voltage reset (LVR)
- High temperature sensor

1.3.15 Background Debug (BDM)

- Non-intrusive memory access commands
- Supports in-circuit programming of on-chip nonvolatile memory

1.3.16 Debugger (DBG)

- Trace buffer with depth of 64 entries
- Three comparators (A, B and C)
  - Comparators A compares the full address bus and full 16-bit data bus
  - Exact address or address range comparisons
- Two types of comparator matches
  - Tagged This matches just before a specific instruction begins execution
  - Force This is valid on the first instruction boundary after a match occurs
- Four trace modes
- Four stage state sequencer

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12P-Family devices

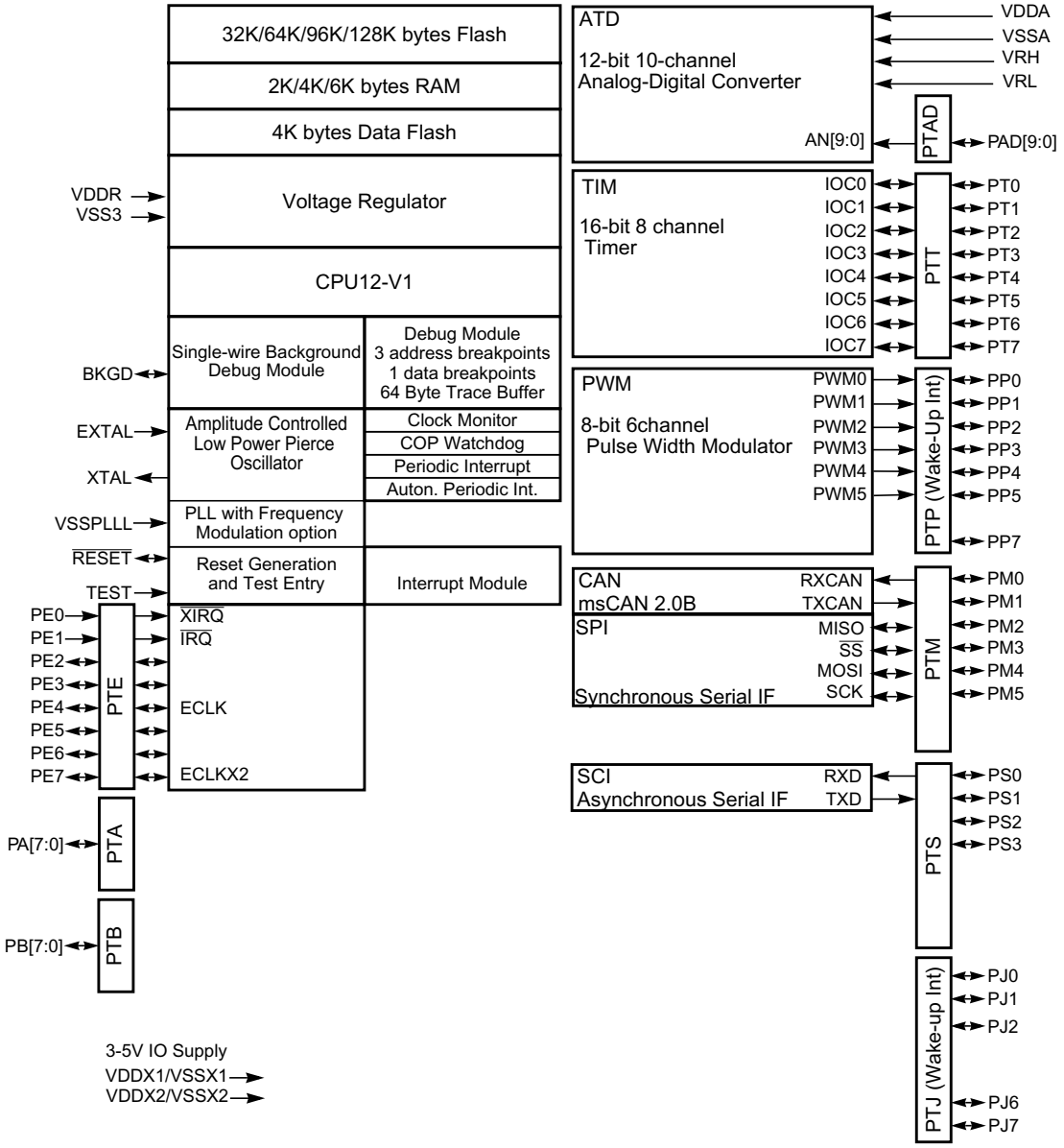

Figure 1-1. MC9S12P-Family Block Diagram

1.5 Device Memory Map

Table 1-2 shows the device register memory map.

Table 1-2. Device Register Memory Map

Address	Module	Size (Bytes)
0x0000–0x0009	PIM (port integration module)	10
0x000A–0x000B	MMC (memory map control)	2
0x000C–0x000D	PIM (port integration module)	2
0x000E–0x000F	Reserved	2
0x0010–0x0017	MMC (memory map control)	8
0x0018–0x0019	Reserved	2
0x001A–0x001B	Device ID register	2
0x001C–0x001F	PIM (port integration module)	4
0x0020–0x002F	DBG (debug module)	16
0x0030–0x0033	Reserved	4
0x0034–0x003F	CPMU (clock and power management)	12
0x0040–0x006F	TIM (timer module)	48
0x0070–0x009F	ATD (analog-to-digital converter 12 bit 10-channel)	48
0x00A0–0x00C7	PWM (pulse-width modulator 6 channels)	40
0x00C8–0x00CF	SCI (serial communications interface)	8
0x00D0–0x00D7	Reserved	8
0x00D8–0x00DF	SPI (serial peripheral interface)	8
0x00E0–0x00FF	Reserved	32
0x0100–0x0113	FTMRC control registers	20
0x0114–0x011F	Reserved	12
0x0120	INT (interrupt module)	1
0x0121–0x013F	Reserved	31
0x0140–0x017F	CAN	64
0x0180–0x023F	Reserved	192
0x0240–0x027F	PIM (port integration module)	64
0x0280–0x02BF	Reserved	64
0x02C0–0x02EF	Reserved	48
0x02F0–0x02FF	CPMU (clock and power management)	16
0x0300–0x03FF	Reserved	256