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# MC9S12XDP512

## Data Sheet

### Covers

### S12XD, S12XB & S12XA Families

***HCS12X  
Microcontrollers***

MC9S12XDP512RMV2  
Rev. 2.21  
October 2009

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# MC9S12XDP512RMV2 Data Sheet

MC9S12XDP512RMV2  
Rev. 2.21  
October 2009





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A full list of family members and options is included in the appendices.

Read page 29 first to understand the maskset specific chapters of this document

This document contains information for all constituent modules, with the exception of the S12X CPU. For S12X CPU information please refer to the CPU S12X Reference Manual.

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## Revision History

Date	Revision Level	Description
April, 2005	02.07	New Book
May, 2005	02.08	Minor corrections
May, 2005	02.09	removed ESD Machine Model from electrical characteristics added thermal characteristics added more details to run current measurement configurations VDDA supply voltage range 3.15V - 3.6V for ATD Operating Characteristics I/O Characteristics for all pins except EXTAL, XTAL .... corrected VREG electrical spec IDD wait max 95mA
May 2005	02.10	Improvements to NVM reliability spec, added part numbers
July 2005	02.11	Added ROM parts to App.
October 2005	02.12	Single Source S12XD Fam. Document, New Memory Map Figures,
May 2006	2.13	SPI electricals updated Voltage Regulator electricals updated Added Partnumbers and 1L15Y maskset Updated App. E 6SCI's on 112 pin DT/P512 and 3 SPI's on all D256 parts
June 2006	2.14	Data Sheet covers S12XD/B & A Family Included different pull device specification for different masksets
July 2006	2.15	Minor Corrections and Improvements
June 2007	2.16	Added 2M42E and 1M84E masksets
July 2007	2.17	Modified Appendix
April 2008	2.18	Better explanation of ATD0/1 for S12XD-Family see page 1305 S12XB256 ATD specification changed see Appendix E.6 added M23S maskset
August 2008	2.19	Corrected XGRAMSIZE of S12XD256 on page 44 Corrected 17.4.2.4 XGATE Memory Map Scheme Corrected 18.4.2.4 XGATE Memory Map Scheme
September 2009	2.20	Corrected Table E-6 , 30K flash memory available for XGATE on B256
October 2009	2.21	Corrected Footnote in Appendix E3 regarding Shared XGATE/CPU area





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