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# MC9S12XEP100 Reference Manual Covers MC9S12XE Family

***HCS12X  
Microcontrollers***

MC9S12XEP100RMV1

Rev. 1.25

02/2013

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This document contains information for the complete S12XE-Family and thus includes a set of separate FTM module sections to cover the whole family. A full list of family members and options is included in the appendices.

This document contains information for all constituent modules, with the exception of the S12X CPU. For S12X CPU information please refer to CPU12XV2 in the CPU12/CPU12X Reference Manual.

**Revision History. Refer to module section revision history tables for more information.**

<b>Date</b>	<b>Revision</b>	<b>Description</b>
Sep, 2008	1.18	Updated NVM timing parameter section for brownout case Specified time delay from RESET to start of CPU code execution Added NVM patch Part IDs Enhanced ECT GPIO / timer function transitioning description
Dec, 2008	1.19	Updated 208MAPBGA thermal parameters Revised TIM flag clearing procedure Corrected CRG register address Added maskset identifier suffix for ATMC fab Fixed typos
Aug, 2009	1.20	Added 208MAPBGA disclaimer Added VREAPI to PT5. Added LVR Note to electricals. Updates to TIM/ECT/XGATE/SCI/MSCAN (see embedded rev. history)
Apr, 2010	1.21	FTM section (see FTM revision history) PIM section (see PIM revision history)
May, 2010	1.22	ECT and TIM sections (see ECT, TIM revision history tables) BDM Alternate clock source defined in device overview
Sep, 2010	1.23	Added S12XEG256 option. Updated MSCAN section
Aug, 2012	1.24	Added bandgap voltage to electricals Added new maskset and Part ID numbers Minor updates to MSCAN,SCI and S12XINT sections Removed BGA disclaimer
Feb, 2013	1.25	Updated MSCAN section Formatting updates and minor corrections in PWM, CRG, BDM, DBG sections Updated Ordering Information

<b>Chapter 1</b>	<b>Device Overview MC9S12XE-Family. . . . .</b>	<b>27</b>
<b>Chapter 2</b>	<b>Port Integration Module (S12XEP100PIMV1) . . . . .</b>	<b>89</b>
<b>Chapter 3</b>	<b>Memory Mapping Control (S12XMMCV4). . . . .</b>	<b>187</b>
<b>Chapter 4</b>	<b>Memory Protection Unit (S12XMPUV1) . . . . .</b>	<b>227</b>
<b>Chapter 5</b>	<b>External Bus Interface (S12XEIV4). . . . .</b>	<b>241</b>
<b>Chapter 6</b>	<b>Interrupt (S12XINTV2) . . . . .</b>	<b>261</b>
<b>Chapter 7</b>	<b>Background Debug Module (S12XBDMV2) . . . . .</b>	<b>279</b>
<b>Chapter 8</b>	<b>S12X Debug (S12XDBGV3) Module . . . . .</b>	<b>305</b>
<b>Chapter 9</b>	<b>Security (S12XE9SECV2). . . . .</b>	<b>347</b>
<b>Chapter 10</b>	<b>XGATE (S12XGATEV3). . . . .</b>	<b>353</b>
<b>Chapter 11</b>	<b>S12XE Clocks and Reset Generator (S12XECRGV1) . . . . .</b>	<b>469</b>
<b>Chapter 12</b>	<b>Pierce Oscillator (S12XOSCLCPV2) . . . . .</b>	<b>499</b>
<b>Chapter 13</b>	<b>Analog-to-Digital Converter (ADC12B16CV1) . . . . .</b>	<b>503</b>
<b>Chapter 14</b>	<b>Enhanced Capture Timer (ECT16B8CV3). . . . .</b>	<b>527</b>
<b>Chapter 15</b>	<b>Inter-Integrated Circuit (IICV3) Block Description. . . . .</b>	<b>579</b>
<b>Chapter 16</b>	<b>Scalable Controller Area Network (S12MSCANV3). . . . .</b>	<b>605</b>
<b>Chapter 17</b>	<b>Periodic Interrupt Timer (S12PIT24B8CV2) . . . . .</b>	<b>659</b>
<b>Chapter 18</b>	<b>Periodic Interrupt Timer (S12PIT24B4CV2) . . . . .</b>	<b>677</b>
<b>Chapter 19</b>	<b>Pulse-Width Modulator (S12PWM8B8CV1) . . . . .</b>	<b>691</b>
<b>Chapter 20</b>	<b>Serial Communication Interface (S12SCIV5) . . . . .</b>	<b>723</b>
<b>Chapter 21</b>	<b>Serial Peripheral Interface (S12SPIV5). . . . .</b>	<b>761</b>
<b>Chapter 22</b>	<b>Timer Module (TIM16B8CV2) Block Description . . . . .</b>	<b>787</b>
<b>Chapter 23</b>	<b>Voltage Regulator (S12VREGL3V3V1) . . . . .</b>	<b>815</b>
<b>Chapter 24</b>	<b>128 KByte Flash Module (S12XFTM128K2V1) . . . . .</b>	<b>832</b>
<b>Chapter 25</b>	<b>256 KByte Flash Module (S12XFTM256K2V1) . . . . .</b>	<b>891</b>

<b>Chapter 26</b>	<b>384 KByte Flash Module (S12XFTM384K2V1) . . . . .</b>	<b>953</b>
<b>Chapter 27</b>	<b>512 KByte Flash Module (S12XFTM512K3V1) . . . . .</b>	<b>1016</b>
<b>Chapter 28</b>	<b>768 KByte Flash Module (S12XFTM768K4V2) . . . . .</b>	<b>1077</b>
<b>Chapter 29</b>	<b>1024 KByte Flash Module (S12XFTM1024K5V2) . . . . .</b>	<b>1140</b>
<b>Appendix A</b>	<b>Electrical Characteristics. . . . .</b>	<b>1201</b>
<b>Appendix B</b>	<b>Package Information . . . . .</b>	<b>1258</b>
<b>Appendix C</b>	<b>PCB Layout Guidelines . . . . .</b>	<b>1260</b>
<b>Appendix D</b>	<b>Derivative Differences . . . . .</b>	<b>1268</b>
<b>Appendix E</b>	<b>Detailed Register Address Map. . . . .</b>	<b>1271</b>
<b>Appendix F</b>	<b>Ordering Information . . . . .</b>	<b>1322</b>



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## Chapter 1 Device Overview MC9S12XE-Family

1.1	Introduction .....	27
1.1.1	Features .....	27
1.1.2	Modes of Operation .....	31
1.1.3	Block Diagram .....	32
1.1.4	Device Memory Map .....	33
1.1.5	Address Mapping .....	34
1.1.6	Detailed Register Map .....	40
1.1.7	Part ID Assignments .....	40
1.2	Signal Description .....	41
1.2.1	Device Pinout .....	42
1.2.2	Pin Assignment Overview .....	48
1.2.3	Detailed Signal Descriptions .....	62
1.2.4	Power Supply Pins .....	72
1.3	System Clock Description .....	75
1.4	Modes of Operation .....	76
1.4.1	Chip Configuration Summary .....	76
1.4.2	Power Modes .....	78
1.4.3	Freeze Mode .....	79
1.4.4	System States .....	79
1.5	Security .....	80
1.6	Resets and Interrupts .....	80
1.6.1	Resets .....	80
1.6.2	Vectors .....	80
1.6.3	Effects of Reset .....	84
1.7	ADC0 Configuration .....	86
1.7.1	External Trigger Input Connection .....	86
1.7.2	ADC0 Channel[17] Connection .....	86
1.8	ADC1 External Trigger Input Connection .....	86
1.9	MPU Configuration .....	87
1.10	VREG Configuration .....	87
1.10.1	Temperature Sensor Configuration .....	87
1.11	BDM Clock Configuration .....	87
1.12	S12XEPIM Configuration .....	87
1.13	Oscillator Configuration .....	88

## Chapter 2 Port Integration Module (S12XEPIMV1)

2.1	Introduction .....	89
-----	--------------------	----



2.1.1	Overview .....	89
2.1.2	Features .....	90
2.2	External Signal Description .....	90
2.3	Memory Map and Register Definition .....	98
2.3.1	Memory Map .....	99
2.3.2	Register Descriptions .....	106
2.3.3	Port A Data Register (PORTA) .....	108
2.3.4	Port B Data Register (PORTB) .....	108
2.3.5	Port A Data Direction Register (DDRA) .....	109
2.3.6	Port B Data Direction Register (DDRB) .....	109
2.3.7	Port C Data Register (PORTC) .....	110
2.3.8	Port D Data Register (PORTD) .....	111
2.3.9	Port C Data Direction Register (DDRC) .....	111
2.3.10	Port D Data Direction Register (DDRD) .....	112
2.3.11	Port E Data Register (PORTE) .....	113
2.3.12	Port E Data Direction Register (DDRE) .....	114
2.3.13	S12X_EBI ports, BKGD pin Pull-up Control Register (PUCR) .....	114
2.3.14	S12X_EBI ports Reduced Drive Register (RDRIV) .....	116
2.3.15	ECLK Control Register (ECLKCTL) .....	117
2.3.16	PIM Reserved Register .....	118
2.3.17	IRQ Control Register (IRQCR) .....	119
2.3.18	PIM Reserved Register .....	119
2.3.19	Port K Data Register (PORTK) .....	120
2.3.20	Port K Data Direction Register (DDRK) .....	120
2.3.21	Port T Data Register (PTT) .....	121
2.3.22	Port T Input Register (PTIT) .....	122
2.3.23	Port T Data Direction Register (DDRT) .....	122
2.3.24	Port T Reduced Drive Register (RDRT) .....	123
2.3.25	Port T Pull Device Enable Register (PERT) .....	123
2.3.26	Port T Polarity Select Register (PPST) .....	124
2.3.27	PIM Reserved Register .....	124
2.3.28	PIM Reserved Register .....	124
2.3.29	Port S Data Register (PTS) .....	125
2.3.30	Port S Input Register (PTIS) .....	126
2.3.31	Port S Data Direction Register (DDRS) .....	126
2.3.32	Port S Reduced Drive Register (RDRS) .....	127
2.3.33	Port S Pull Device Enable Register (PERS) .....	128
2.3.34	Port S Polarity Select Register (PPSS) .....	128
2.3.35	Port S Wired-Or Mode Register (WOMS) .....	129
2.3.36	PIM Reserved Register .....	129
2.3.37	Port M Data Register (PTM) .....	130
2.3.38	Port M Input Register (PTIM) .....	131
2.3.39	Port M Data Direction Register (DDRM) .....	132
2.3.40	Port M Reduced Drive Register (RDRM) .....	134
2.3.41	Port M Pull Device Enable Register (PERM) .....	134

2.3.42	Port M Polarity Select Register (PPSM)	135
2.3.43	Port M Wired-Or Mode Register (WOMM)	135
2.3.44	Module Routing Register (MODRR)	136
2.3.45	Port P Data Register (PTP)	137
2.3.46	Port P Input Register (PTIP)	138
2.3.47	Port P Data Direction Register (DDRP)	139
2.3.48	Port P Reduced Drive Register (RDRP)	140
2.3.49	Port P Pull Device Enable Register (PERP)	140
2.3.50	Port P Polarity Select Register (PPSP)	141
2.3.51	Port P Interrupt Enable Register (PIEP)	141
2.3.52	Port P Interrupt Flag Register (PIFP)	142
2.3.53	Port H Data Register (PTH)	142
2.3.54	Port H Input Register (PTIH)	144
2.3.55	Port H Data Direction Register (DDRH)	144
2.3.56	Port H Reduced Drive Register (RDRH)	146
2.3.57	Port H Pull Device Enable Register (PERH)	147
2.3.58	Port H Polarity Select Register (PPSH)	147
2.3.59	Port H Interrupt Enable Register (PIEH)	148
2.3.60	Port H Interrupt Flag Register (PIFH)	148
2.3.61	Port J Data Register (PTJ)	149
2.3.62	Port J Input Register (PTIJ)	150
2.3.63	Port J Data Direction Register (DDRJ)	150
2.3.64	Port J Reduced Drive Register (RDRJ)	152
2.3.65	Port J Pull Device Enable Register (PERJ)	153
2.3.66	Port J Polarity Select Register (PPSJ)	153
2.3.67	Port J Interrupt Enable Register (PIEJ)	154
2.3.68	Port J Interrupt Flag Register (PIFJ)	154
2.3.69	Port AD0 Data Register 0 (PT0AD0)	155
2.3.70	Port AD0 Data Register 1 (PT1AD0)	155
2.3.71	Port AD0 Data Direction Register 0 (DDR0AD0)	156
2.3.72	Port AD0 Data Direction Register 1 (DDR1AD0)	156
2.3.73	Port AD0 Reduced Drive Register 0 (RDR0AD0)	157
2.3.74	Port AD0 Reduced Drive Register 1 (RDR1AD0)	158
2.3.75	Port AD0 Pull Up Enable Register 0 (PER0AD0)	158
2.3.76	Port AD0 Pull Up Enable Register 1 (PER1AD0)	159
2.3.77	Port AD1 Data Register 0 (PT0AD1)	159
2.3.78	Port AD1 Data Register 1 (PT1AD1)	160
2.3.79	Port AD1 Data Direction Register 0 (DDR0AD1)	160
2.3.80	Port AD1 Data Direction Register 1 (DDR1AD1)	161
2.3.81	Port AD1 Reduced Drive Register 0 (RDR0AD1)	162
2.3.82	Port AD1 Reduced Drive Register 1 (RDR1AD1)	162
2.3.83	Port AD1 Pull Up Enable Register 0 (PER0AD1)	163
2.3.84	Port AD1 Pull Up Enable Register 1 (PER1AD1)	163
2.3.85	Port R Data Register (PTR)	164
2.3.86	Port R Input Register (PTIR)	164

2.3.87	Port R Data Direction Register (DDRR)	165
2.3.88	Port R Reduced Drive Register (RDRR)	165
2.3.89	Port R Pull Device Enable Register (PERR)	166
2.3.90	Port R Polarity Select Register (PPSR)	166
2.3.91	PIM Reserved Register	167
2.3.92	Port R Routing Register (PTRRR)	167
2.3.93	Port L Data Register (PTL)	168
2.3.94	Port L Input Register (PTIL)	170
2.3.95	Port L Data Direction Register (DDRL)	170
2.3.96	Port L Reduced Drive Register (RDRL)	171
2.3.97	Port L Pull Device Enable Register (PERL)	171
2.3.98	Port L Polarity Select Register (PPSL)	172
2.3.99	Port L Wired-Or Mode Register (WOML)	172
2.3.100	Port L Routing Register (PTLRR)	173
2.3.101	Port F Data Register (PTF)	173
2.3.102	Port F Input Register (PTIF)	175
2.3.103	Port F Data Direction Register (DDRF)	175
2.3.104	Port F Reduced Drive Register (RDRF)	176
2.3.105	Port F Pull Device Enable Register (PERF)	176
2.3.106	Port F Polarity Select Register (PPSF)	177
2.3.107	PIM Reserved Register	177
2.3.108	Port F Routing Register (PTFRR)	177
2.4	Functional Description	178
2.4.1	General	178
2.4.2	Registers	178
2.4.3	Pins and Ports	181
2.4.4	Pin interrupts	185
2.5	Initialization Information	186
2.5.1	Port Data and Data Direction Register writes	186

## Chapter 3

### Memory Mapping Control (S12XMMCV4)

3.1	Introduction	187
3.1.1	Terminology	188
3.1.2	Features	188
3.1.3	S12X Memory Mapping	189
3.1.4	Modes of Operation	189
3.1.5	Block Diagram	190
3.2	External Signal Description	190
3.3	Memory Map and Registers	192
3.3.1	Module Memory Map	192
3.3.2	Register Descriptions	193
3.4	Functional Description	204
3.4.1	MCU Operating Mode	204
3.4.2	Memory Map Scheme	205

3.4.3	Chip Access Restrictions	217
3.4.4	Chip Bus Control	217
3.5	Initialization/Application Information	218
3.5.1	CALL and RTC Instructions	218
3.5.2	Port Replacement Registers (PRRs)	220
3.5.3	On-Chip ROM Control	221

## Chapter 4 Memory Protection Unit (S12XMPUV1)

4.1	Introduction	227
4.1.1	Preface	227
4.1.2	Overview	227
4.1.3	Features	228
4.1.4	Modes of Operation	229
4.2	External Signal Description	229
4.3	Memory Map and Register Definition	229
4.3.1	Register Descriptions	230
4.4	Functional Description	237
4.4.1	Protection Descriptors	237
4.4.2	Interrupts	239
4.5	Initialization/Application Information	239
4.5.1	Initialization	239

## Chapter 5 External Bus Interface (S12XEIV4)

5.1	Introduction	241
5.1.1	Glossary or Terms	242
5.1.2	Features	242
5.1.3	Modes of Operation	242
5.1.4	Block Diagram	243
5.2	External Signal Description	243
5.3	Memory Map and Register Definition	245
5.3.1	Module Memory Map	245
5.3.2	Register Descriptions	245
5.4	Functional Description	248
5.4.1	Operating Modes and External Bus Properties	248
5.4.2	Internal Visibility	249
5.4.3	Accesses to Port Replacement Registers	253
5.4.4	Stretched External Bus Accesses	253
5.4.5	Data Select and Data Direction Signals	254
5.4.6	Low-Power Options	256
5.5	Initialization/Application Information	256
5.5.1	Normal Expanded Mode	256
5.5.2	Emulation Modes	257

## Chapter 6 Interrupt (S12XINTV2)

6.1	Introduction .....	261
	6.1.1 Glossary .....	262
	6.1.2 Features .....	262
	6.1.3 Modes of Operation .....	263
	6.1.4 Block Diagram .....	264
6.2	External Signal Description .....	264
6.3	Memory Map and Register Definition .....	265
	6.3.1 Module Memory Map .....	265
	6.3.2 Register Descriptions .....	266
6.4	Functional Description .....	271
	6.4.1 S12X Exception Requests .....	272
	6.4.2 Interrupt Prioritization .....	272
	6.4.3 XGATE Requests .....	273
	6.4.4 Priority Decoders .....	273
	6.4.5 Reset Exception Requests .....	274
	6.4.6 Exception Priority .....	274
6.5	Initialization/Application Information .....	275
	6.5.1 Initialization .....	275
	6.5.2 Interrupt Nesting .....	275
	6.5.3 Wake Up from Stop or Wait Mode .....	276

## Chapter 7 Background Debug Module (S12XBDMV2)

7.1	Introduction .....	279
	7.1.1 Features .....	279
	7.1.2 Modes of Operation .....	280
	7.1.3 Block Diagram .....	281
7.2	External Signal Description .....	281
7.3	Memory Map and Register Definition .....	282
	7.3.1 Module Memory Map .....	282
	7.3.2 Register Descriptions .....	282
	7.3.3 Family ID Assignment .....	287
7.4	Functional Description .....	287
	7.4.1 Security .....	288
	7.4.2 Enabling and Activating BDM .....	288
	7.4.3 BDM Hardware Commands .....	289
	7.4.4 Standard BDM Firmware Commands .....	290
	7.4.5 BDM Command Structure .....	291
	7.4.6 BDM Serial Interface .....	293
	7.4.7 Serial Interface Hardware Handshake Protocol .....	296
	7.4.8 Hardware Handshake Abort Procedure .....	298
	7.4.9 SYNC — Request Timed Reference Pulse .....	301

7.4.10	Instruction Tracing .....	302
7.4.11	Serial Communication Time Out .....	303

## Chapter 8

### S12X Debug (S12XDBGV3) Module

8.1	Introduction .....	305
8.1.1	Glossary .....	305
8.1.2	Overview .....	306
8.1.3	Features .....	306
8.1.4	Modes of Operation .....	307
8.1.5	Block Diagram .....	308
8.2	External Signal Description .....	308
8.3	Memory Map and Registers .....	308
8.3.1	Module Memory Map .....	308
8.3.2	Register Descriptions .....	310
8.4	Functional Description .....	326
8.4.1	S12XDBG Operation .....	327
8.4.2	Comparator Modes .....	327
8.4.3	Trigger Modes .....	331
8.4.4	State Sequence Control .....	332
8.4.5	Trace Buffer Operation .....	333
8.4.6	Tagging .....	341
8.4.7	Breakpoints .....	342

## Chapter 9

### Security (S12XE9SECV2)

9.1	Introduction .....	347
9.1.1	Features .....	347
9.1.2	Modes of Operation .....	348
9.1.3	Securing the Microcontroller .....	348
9.1.4	Operation of the Secured Microcontroller .....	349
9.1.5	Unsecuring the Microcontroller .....	350
9.1.6	Reprogramming the Security Bits .....	351
9.1.7	Complete Memory Erase (Special Modes) .....	351

## Chapter 10

### XGATE (S12XGATEV3)

10.1	Introduction .....	353
10.1.1	Glossary of Terms .....	353
10.1.2	Features .....	354
10.1.3	Modes of Operation .....	355
10.1.4	Block Diagram .....	355
10.2	External Signal Description .....	356
10.3	Memory Map and Register Definition .....	356

10.3.1	Register Descriptions .....	356
10.4	Functional Description .....	373
10.4.1	XGATE RISC Core .....	374
10.4.2	Programmer's Model .....	374
10.4.3	Memory Map .....	375
10.4.4	Semaphores .....	376
10.4.5	Software Error Detection .....	378
10.5	Interrupts .....	379
10.5.1	Incoming Interrupt Requests .....	379
10.5.2	Outgoing Interrupt Requests .....	379
10.6	Debug Mode .....	379
10.6.1	Debug Features .....	379
10.6.2	Leaving Debug Mode .....	381
10.7	Security .....	381
10.8	Instruction Set .....	382
10.8.1	Addressing Modes .....	382
10.8.2	Instruction Summary and Usage .....	385
10.8.3	Cycle Notation .....	387
10.8.4	Thread Execution .....	388
10.8.5	Instruction Glossary .....	388
10.8.6	Instruction Coding .....	461
10.9	Initialization and Application Information .....	463
10.9.1	Initialization .....	463
10.9.2	Code Example (Transmit "Hello World!" on SCI) .....	463
10.9.3	Stack Support .....	466

## Chapter 11

### S12XE Clocks and Reset Generator (S12XECRGV1)

11.1	Introduction .....	469
11.1.1	Features .....	469
11.1.2	Modes of Operation .....	470
11.1.3	Block Diagram .....	470
11.2	Signal Description .....	471
11.2.1	$V_{DDPLL}$ , $V_{SSPLL}$ .....	471
11.2.2	RESET .....	471
11.3	Memory Map and Registers .....	472
11.3.1	Module Memory Map .....	472
11.3.2	Register Descriptions .....	473
11.4	Functional Description .....	486
11.4.1	Functional Blocks .....	486
11.4.2	Operation Modes .....	491
11.4.3	Low Power Options .....	492
11.5	Resets .....	494
11.5.1	Description of Reset Operation .....	495
11.6	Interrupts .....	497

11.6.1 Description of Interrupt Operation .....	498
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## Chapter 12

### Pierce Oscillator (S12XOSCLCPV2)

12.1 Introduction .....	499
12.1.1 Features .....	499
12.1.2 Modes of Operation .....	499
12.1.3 Block Diagram .....	500
12.2 External Signal Description .....	500
12.2.1 $V_{DDPLL}$ and $V_{SSPLL}$ — Operating and Ground Voltage Pins .....	500
12.2.2 EXTAL and XTAL — Input and Output Pins .....	500
12.3 Memory Map and Register Definition .....	502
12.4 Functional Description .....	502
12.4.1 Gain Control .....	502
12.4.2 Clock Monitor .....	502
12.4.3 Wait Mode Operation .....	502
12.4.4 Stop Mode Operation .....	502

## Chapter 13

### Analog-to-Digital Converter (ADC12B16CV1)

13.1 Introduction .....	503
13.1.1 Features .....	503
13.1.2 Modes of Operation .....	504
13.1.3 Block Diagram .....	505
13.2 Signal Description .....	506
13.2.1 Detailed Signal Descriptions .....	506
13.3 Memory Map and Register Definition .....	506
13.3.1 Module Memory Map .....	506
13.3.2 Register Descriptions .....	508
13.4 Functional Description .....	523
13.4.1 Analog Sub-Block .....	523
13.4.2 Digital Sub-Block .....	524
13.5 Resets .....	525
13.6 Interrupts .....	525

## Chapter 14

### Enhanced Capture Timer (ECT16B8CV3)

14.1 Introduction .....	527
14.1.1 Features .....	527
14.1.2 Modes of Operation .....	528
14.1.3 Block Diagram .....	529
14.2 External Signal Description .....	529
14.2.1 IOC7 — Input Capture and Output Compare Channel 7 .....	529
14.2.2 IOC6 — Input Capture and Output Compare Channel 6 .....	529



14.2.3	IOC5 — Input Capture and Output Compare Channel 5	530
14.2.4	IOC4 — Input Capture and Output Compare Channel 4	530
14.2.5	IOC3 — Input Capture and Output Compare Channel 3	530
14.2.6	IOC2 — Input Capture and Output Compare Channel 2	530
14.2.7	IOC1 — Input Capture and Output Compare Channel 1	530
14.2.8	IOC0 — Input Capture and Output Compare Channel 0	530
14.3	Memory Map and Register Definition	530
14.3.1	Module Memory Map	530
14.3.2	Register Descriptions	530
14.4	Functional Description	566
14.4.1	Enhanced Capture Timer Modes of Operation	573
14.4.2	Reset	577
14.4.3	Interrupts	577

## Chapter 15

### Inter-Integrated Circuit (IICV3) Block Description

15.1	Introduction	579
15.1.1	Features	579
15.1.2	Modes of Operation	580
15.1.3	Block Diagram	580
15.2	External Signal Description	580
15.2.1	IIC_SCL — Serial Clock Line Pin	580
15.2.2	IIC_SDA — Serial Data Line Pin	580
15.3	Memory Map and Register Definition	581
15.3.1	Register Descriptions	581
15.4	Functional Description	593
15.4.1	I-Bus Protocol	593
15.4.2	Operation in Run Mode	598
15.4.3	Operation in Wait Mode	598
15.4.4	Operation in Stop Mode	598
15.5	Resets	598
15.6	Interrupts	598
15.7	Application Information	599
15.7.1	IIC Programming Examples	599

## Chapter 16

### Freescale's Scalable Controller Area Network (S12MSCANV3)

16.1	Introduction	605
16.1.1	Glossary	606
16.1.2	Block Diagram	606
16.1.3	Features	607
16.1.4	Modes of Operation	607
16.2	External Signal Description	608
16.2.1	RXCAN — CAN Receiver Input Pin	608

16.2.2	TXCAN — CAN Transmitter Output Pin	608
16.2.3	CAN System	608
16.3	Memory Map and Register Definition	609
16.3.1	Module Memory Map	609
16.3.2	Register Descriptions	611
16.3.3	Programmer’s Model of Message Storage	630
16.4	Functional Description	641
16.4.1	General	641
16.4.2	Message Storage	641
16.4.3	Identifier Acceptance Filter	644
16.4.4	Modes of Operation	650
16.4.5	Low-Power Options	652
16.4.6	Reset Initialization	656
16.4.7	Interrupts	656
16.5	Initialization/Application Information	658
16.5.1	MSCAN initialization	658
16.5.2	Bus-Off Recovery	658

## Chapter 17

### Periodic Interrupt Timer (S12PIT24B8CV2)

17.1	Introduction	659
17.1.1	Glossary	659
17.1.2	Features	659
17.1.3	Modes of Operation	659
17.1.4	Block Diagram	660
17.2	External Signal Description	660
17.3	Register Definition	661
17.4	Functional Description	671
17.4.1	Timer	672
17.4.2	Interrupt Interface	673
17.4.3	Hardware Trigger	673
17.5	Initialization	674
17.5.1	Startup	674
17.5.2	Shutdown	674
17.5.3	Flag Clearing	674
17.6	Application Information	674

## Chapter 18

### Periodic Interrupt Timer (S12PIT24B4CV2)

18.1	Introduction	677
18.1.1	Glossary	677
18.1.2	Features	677
18.1.3	Modes of Operation	677
18.1.4	Block Diagram	678

18.2	External Signal Description .....	678
18.3	Register Definition .....	678
18.4	Functional Description .....	687
18.4.1	Timer .....	687
18.4.2	Interrupt Interface .....	689
18.4.3	Hardware Trigger .....	689
18.5	Initialization .....	689
18.5.1	Startup .....	689
18.5.2	Shutdown .....	689
18.5.3	Flag Clearing .....	689
18.6	Application Information .....	690

## Chapter 19

### Pulse-Width Modulator (S12PWM8B8CV1)

19.1	Introduction .....	691
19.1.1	Features .....	691
19.1.2	Modes of Operation .....	691
19.1.3	Block Diagram .....	692
19.2	External Signal Description .....	692
19.2.1	PWM7 — PWM Channel 7 .....	692
19.2.2	PWM6 — PWM Channel 6 .....	693
19.2.3	PWM5 — PWM Channel 5 .....	693
19.2.4	PWM4 — PWM Channel 4 .....	693
19.2.5	PWM3 — PWM Channel 3 .....	693
19.2.6	PWM3 — PWM Channel 2 .....	693
19.2.7	PWM3 — PWM Channel 1 .....	693
19.2.8	PWM3 — PWM Channel 0 .....	693
19.3	Memory Map and Register Definition .....	693
19.3.1	Module Memory Map .....	693
19.3.2	Register Descriptions .....	694
19.4	Functional Description .....	709
19.4.1	PWM Clock Select .....	709
19.4.2	PWM Channel Timers .....	712
19.5	Resets .....	720
19.6	Interrupts .....	721

## Chapter 20

### Serial Communication Interface (S12SCIV5)

20.1	Introduction .....	723
20.1.1	Glossary .....	723
20.1.2	Features .....	724
20.1.3	Modes of Operation .....	724
20.1.4	Block Diagram .....	725
20.2	External Signal Description .....	726

20.2.1	TXD — Transmit Pin	726
20.2.2	RXD — Receive Pin	726
20.3	Memory Map and Register Definition	726
20.3.1	Module Memory Map and Register Definition	726
20.3.2	Register Descriptions	727
20.4	Functional Description	739
20.4.1	Infrared Interface Submodule	740
20.4.2	LIN Support	740
20.4.3	Data Format	741
20.4.4	Baud Rate Generation	742
20.4.5	Transmitter	743
20.4.6	Receiver	748
20.4.7	Single-Wire Operation	756
20.4.8	Loop Operation	757
20.5	Initialization/Application Information	757
20.5.1	Reset Initialization	757
20.5.2	Modes of Operation	757
20.5.3	Interrupt Operation	758
20.5.4	Recovery from Wait Mode	760
20.5.5	Recovery from Stop Mode	760

## Chapter 21

### Serial Peripheral Interface (S12SPIV5)

21.1	Introduction	761
21.1.1	Glossary of Terms	761
21.1.2	Features	761
21.1.3	Modes of Operation	761
21.1.4	Block Diagram	762
21.2	External Signal Description	763
21.2.1	MOSI — Master Out/Slave In Pin	763
21.2.2	MISO — Master In/Slave Out Pin	763
21.2.3	SS — Slave Select Pin	764
21.2.4	SCK — Serial Clock Pin	764
21.3	Memory Map and Register Definition	764
21.3.1	Module Memory Map	764
21.3.2	Register Descriptions	765
21.4	Functional Description	773
21.4.1	Master Mode	774
21.4.2	Slave Mode	775
21.4.3	Transmission Formats	776
21.4.4	SPI Baud Rate Generation	781
21.4.5	Special Features	782
21.4.6	Error Conditions	783
21.4.7	Low Power Mode Options	784

## Chapter 22

### Timer Module (TIM16B8CV2) Block Description

22.1	Introduction .....	787
22.1.1	Features .....	788
22.1.2	Modes of Operation .....	788
22.1.3	Block Diagrams .....	789
22.2	External Signal Description .....	791
22.2.1	IOC7 — Input Capture and Output Compare Channel 7 Pin .....	791
22.2.2	IOC6 — Input Capture and Output Compare Channel 6 Pin .....	791
22.2.3	IOC5 — Input Capture and Output Compare Channel 5 Pin .....	791
22.2.4	IOC4 — Input Capture and Output Compare Channel 4 Pin .....	791
22.2.5	IOC3 — Input Capture and Output Compare Channel 3 Pin .....	791
22.2.6	IOC2 — Input Capture and Output Compare Channel 2 Pin .....	791
22.2.7	IOC1 — Input Capture and Output Compare Channel 1 Pin .....	792
22.2.8	IOC0 — Input Capture and Output Compare Channel 0 Pin .....	792
22.3	Memory Map and Register Definition .....	792
22.3.1	Module Memory Map .....	792
22.3.2	Register Descriptions .....	792
22.4	Functional Description .....	809
22.4.1	Prescaler .....	810
22.4.2	Input Capture .....	811
22.4.3	Output Compare .....	811
22.4.4	Pulse Accumulator .....	812
22.4.5	Event Counter Mode .....	812
22.4.6	Gated Time Accumulation Mode .....	813
22.5	Resets .....	813
22.6	Interrupts .....	813
22.6.1	Channel [7:0] Interrupt (C[7:0]F) .....	814
22.6.2	Pulse Accumulator Input Interrupt (PAOVI) .....	814
22.6.3	Pulse Accumulator Overflow Interrupt (PAOVF) .....	814
22.6.4	Timer Overflow Interrupt (TOF) .....	814

## Chapter 23

### Voltage Regulator (S12VREGL3V3V1)

23.1	Introduction .....	815
23.1.1	Features .....	815
23.1.2	Modes of Operation .....	815
23.1.3	Block Diagram .....	816
23.2	External Signal Description .....	818
23.2.1	VDDR — Regulator Power Input Pins .....	818
23.2.2	VDDA, VSSA — Regulator Reference Supply Pins .....	818
23.2.3	VDD, VSS — Regulator Output1 (Core Logic) Pins .....	818
23.2.4	VDDF — Regulator Output2 (NVM Logic) Pins .....	819
23.2.5	VDDPLL, VSSPLL — Regulator Output3 (PLL) Pins .....	819

23.2.6	VDDX — Power Input Pin	819
23.2.7	V <sub>REGEN</sub> — Optional Regulator Enable Pin	819
23.2.8	V <sub>REG_API</sub> — Optional Autonomous Periodical Interrupt Output Pin	819
23.3	Memory Map and Register Definition	819
23.3.1	Module Memory Map	820
23.3.2	Register Descriptions	820
23.4	Functional Description	826
23.4.1	General	826
23.4.2	Regulator Core (REG)	826
23.4.3	Low-Voltage Detect (LVD)	826
23.4.4	Power-On Reset (POR)	827
23.4.5	Low-Voltage Reset (LVR)	827
23.4.6	HTD - High Temperature Detect	827
23.4.7	Regulator Control (CTRL)	827
23.4.8	Autonomous Periodical Interrupt (API)	827
23.4.9	Resets	828
23.4.10	Description of Reset Operation	828
23.4.11	Interrupts	828

## Chapter 24

### 128 KByte Flash Module (S12XFTM128K2V1)

24.1	Introduction	832
24.1.1	Glossary	832
24.1.2	Features	833
24.1.3	Block Diagram	834
24.2	External Signal Description	835
24.3	Memory Map and Registers	836
24.3.1	Module Memory Map	836
24.3.2	Register Descriptions	841
24.4	Functional Description	862
24.4.1	Flash Command Operations	862
24.4.2	Flash Command Description	867
24.4.3	Interrupts	887
24.4.4	Wait Mode	888
24.4.5	Stop Mode	888
24.5	Security	888
24.5.1	Unsecuring the MCU using Backdoor Key Access	889
24.5.2	Unsecuring the MCU in Special Single Chip Mode using BDM	890
24.5.3	Mode and Security Effects on Flash Command Availability	890
24.6	Initialization	890

## Chapter 25

### 256 KByte Flash Module (S12XFTM256K2V1)

25.1	Introduction	891
------	--------------	-----

25.1.1	Glossary	892
25.1.2	Features	893
25.1.3	Block Diagram	894
25.2	External Signal Description	895
25.3	Memory Map and Registers	896
25.3.1	Module Memory Map	896
25.3.2	Register Descriptions	901
25.4	Functional Description	922
25.4.1	Flash Command Operations	922
25.4.2	Flash Command Description	927
25.4.3	Interrupts	948
25.4.4	Wait Mode	949
25.4.5	Stop Mode	949
25.5	Security	949
25.5.1	Unsecuring the MCU using Backdoor Key Access	950
25.5.2	Unsecuring the MCU in Special Single Chip Mode using BDM	951
25.5.3	Mode and Security Effects on Flash Command Availability	951
25.6	Initialization	951

## Chapter 26

### 384 KByte Flash Module (S12XFTM384K2V1)

26.1	Introduction	953
26.1.1	Glossary	954
26.1.2	Features	955
26.1.3	Block Diagram	956
26.2	External Signal Description	957
26.3	Memory Map and Registers	958
26.3.1	Module Memory Map	958
26.3.2	Register Descriptions	963
26.4	Functional Description	984
26.4.1	Flash Command Operations	984
26.4.2	Flash Command Description	989
26.4.3	Interrupts	1011
26.4.4	Wait Mode	1012
26.4.5	Stop Mode	1012
26.5	Security	1012
26.5.1	Unsecuring the MCU using Backdoor Key Access	1013
26.5.2	Unsecuring the MCU in Special Single Chip Mode using BDM	1014
26.5.3	Mode and Security Effects on Flash Command Availability	1014
26.6	Initialization	1014

## Chapter 27

### 512 KByte Flash Module (S12XFTM512K3V1)

27.1	Introduction	1016
------	--------------	------

27.1.1	Glossary	1016
27.1.2	Features	1017
27.1.3	Block Diagram	1018
27.2	External Signal Description	1019
27.3	Memory Map and Registers	1020
27.3.1	Module Memory Map	1020
27.3.2	Register Descriptions	1025
27.4	Functional Description	1046
27.4.1	Flash Command Operations	1046
27.4.2	Flash Command Description	1051
27.4.3	Interrupts	1072
27.4.4	Wait Mode	1073
27.4.5	Stop Mode	1073
27.5	Security	1073
27.5.1	Unsecuring the MCU using Backdoor Key Access	1074
27.5.2	Unsecuring the MCU in Special Single Chip Mode using BDM	1075
27.5.3	Mode and Security Effects on Flash Command Availability	1075
27.6	Initialization	1075

## Chapter 28

### 768 KByte Flash Module (S12XFTM768K4V2)

28.1	Introduction	1077
28.1.1	Glossary	1078
28.1.2	Features	1079
28.1.3	Block Diagram	1080
28.2	External Signal Description	1081
28.3	Memory Map and Registers	1082
28.3.1	Module Memory Map	1082
28.3.2	Register Descriptions	1087
28.4	Functional Description	1108
28.4.1	Flash Command Operations	1108
28.4.2	Flash Command Description	1113
28.4.3	Interrupts	1135
28.4.4	Wait Mode	1136
28.4.5	Stop Mode	1136
28.5	Security	1136
28.5.1	Unsecuring the MCU using Backdoor Key Access	1137
28.5.2	Unsecuring the MCU in Special Single Chip Mode using BDM	1138
28.5.3	Mode and Security Effects on Flash Command Availability	1138
28.6	Initialization	1138

## Chapter 29

### 1024 KByte Flash Module (S12XFTM1024K5V2)

29.1	Introduction	1140
------	--------------	------



29.1.1	Glossary .....	1140
29.1.2	Features .....	1141
29.1.3	Block Diagram .....	1142
29.2	External Signal Description .....	1143
29.3	Memory Map and Registers .....	1144
29.3.1	Module Memory Map .....	1144
29.3.2	Register Descriptions .....	1150
29.4	Functional Description .....	1171
29.4.1	Flash Command Operations .....	1171
29.4.2	Flash Command Description .....	1176
29.4.3	Interrupts .....	1197
29.4.4	Wait Mode .....	1198
29.4.5	Stop Mode .....	1198
29.5	Security .....	1198
29.5.1	Unsecuring the MCU using Backdoor Key Access .....	1199
29.5.2	Unsecuring the MCU in Special Single Chip Mode using BDM .....	1200
29.5.3	Mode and Security Effects on Flash Command Availability .....	1200
29.6	Initialization .....	1200

## Appendix A

### Electrical Characteristics

A.1	General .....	1201
A.1.1	Parameter Classification .....	1201
A.1.2	Power Supply .....	1201
A.1.3	Pins .....	1202
A.1.4	Current Injection .....	1203
A.1.5	Absolute Maximum Ratings .....	1203
A.1.6	ESD Protection and Latch-up Immunity .....	1204
A.1.7	Operating Conditions .....	1206
A.1.8	Power Dissipation and Thermal Characteristics .....	1207
A.1.9	I/O Characteristics .....	1209
A.1.10	Supply Currents .....	1214
A.2	ATD Characteristics .....	1219
A.2.1	ATD Operating Characteristics .....	1219
A.2.2	Factors Influencing Accuracy .....	1219
A.2.3	ATD Accuracy .....	1221
A.3	NVM, Flash and Emulated EEPROM .....	1224
A.3.1	Timing Parameters .....	1224
A.3.2	NVM Reliability Parameters .....	1231
A.4	Voltage Regulator .....	1234
A.5	Output Loads .....	1235
A.5.1	Resistive Loads .....	1235
A.5.2	Capacitive Loads .....	1235
A.5.3	Chip Power-up and Voltage Drops .....	1235
A.6	Reset, Oscillator and PLL .....	1236

A.6.1	Startup .....	1236
A.6.2	Oscillator .....	1238
A.6.3	Phase Locked Loop .....	1239
A.7	External Interface Timing .....	1241
A.7.1	MSCAN .....	1241
A.7.2	SPI Timing .....	1241
A.7.3	External Bus Timing .....	1247

## Appendix B Package Information

B.1	208 MAPBGA .....	1259
B.2	144-Pin LQFP .....	1259
B.3	112-Pin LQFP Package .....	1261
B.4	80-Pin QFP Package .....	1262

## Appendix C PCB Layout Guidelines

## Appendix D Derivative Differences

D.1	Memory Sizes and Package Options S12XE - Family .....	1268
D.2	Pinout explanations: .....	1270

## Appendix E Detailed Register Address Map

## Appendix F Ordering Information